intel

Systems Data Catalog 1980

Intel Corporation, 1976, 1977, 1978, 1979

PRICE: $5.00

Intel was organized in 1968 to utilize the rapidly expanding technology of inegrated electronics. During its brief history, Intel has become the world's largest supplier of MOS circuits, and is in the top ten of the world's producers of all semiconductor devices.

This System Data Catalog provides complete specifications on most of Intel standard memory systems, single board computers, Intellec microcomputer development systems, software and peripherals. Margin tabs provide quick guides to major product categories; indexes located in Section 1 and at the beginning of each section allow location of specific products. Information on ordering and product flow may be found in Section 2. A listing of available technical literature may be found in Section 17.

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System Data Catalog

August 1979

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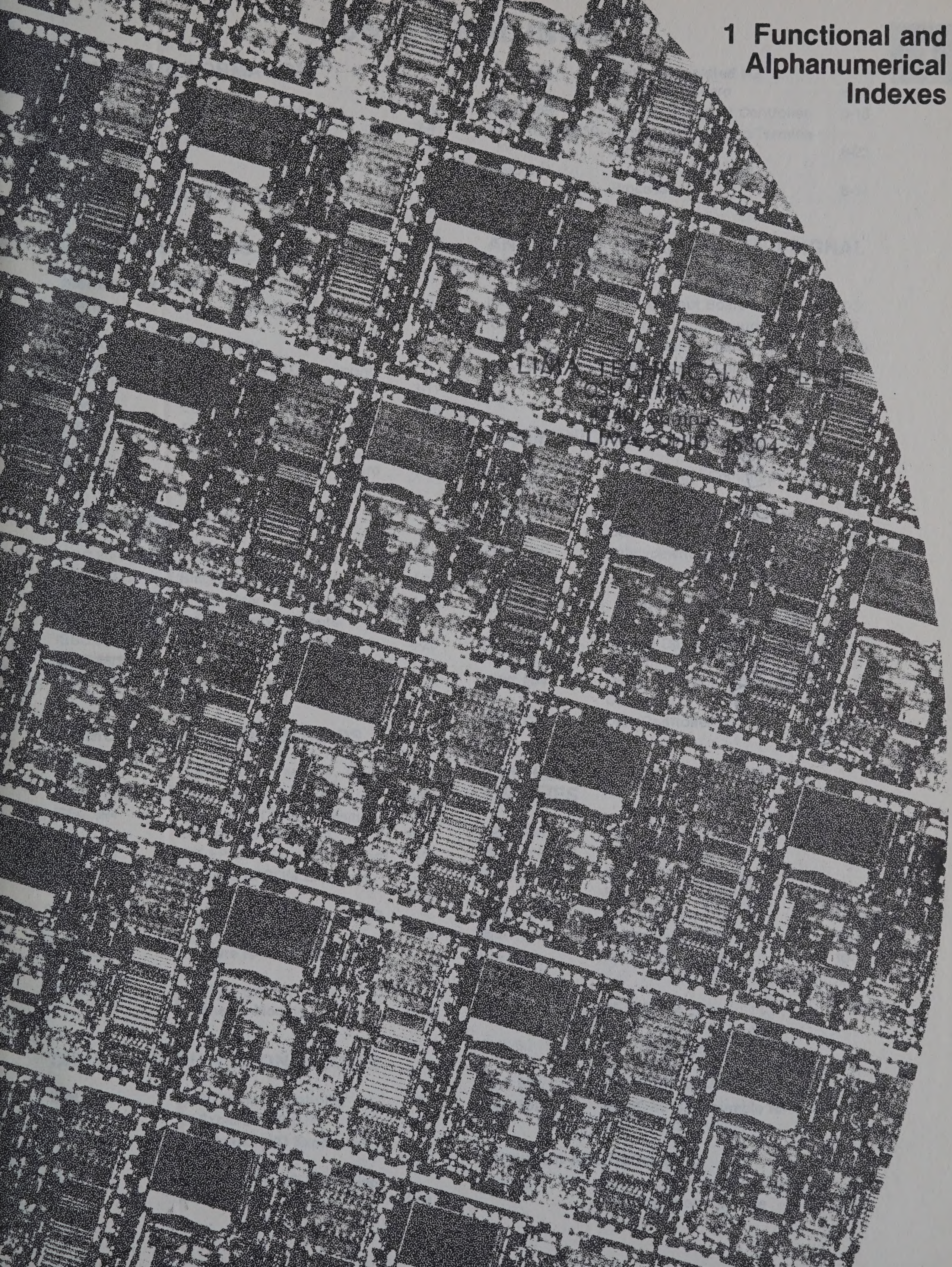
1 Functional and Alphanumerical Indexes



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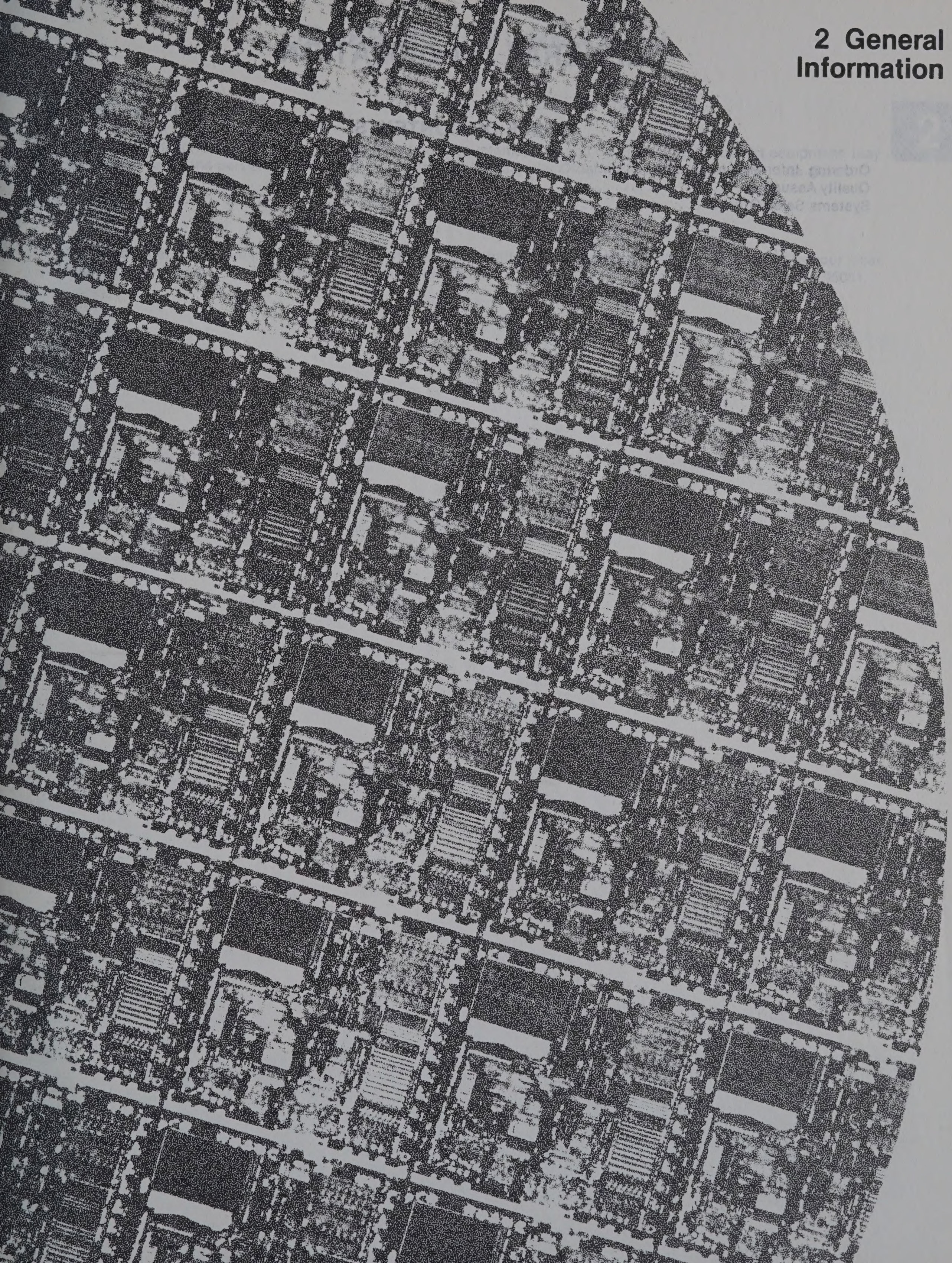

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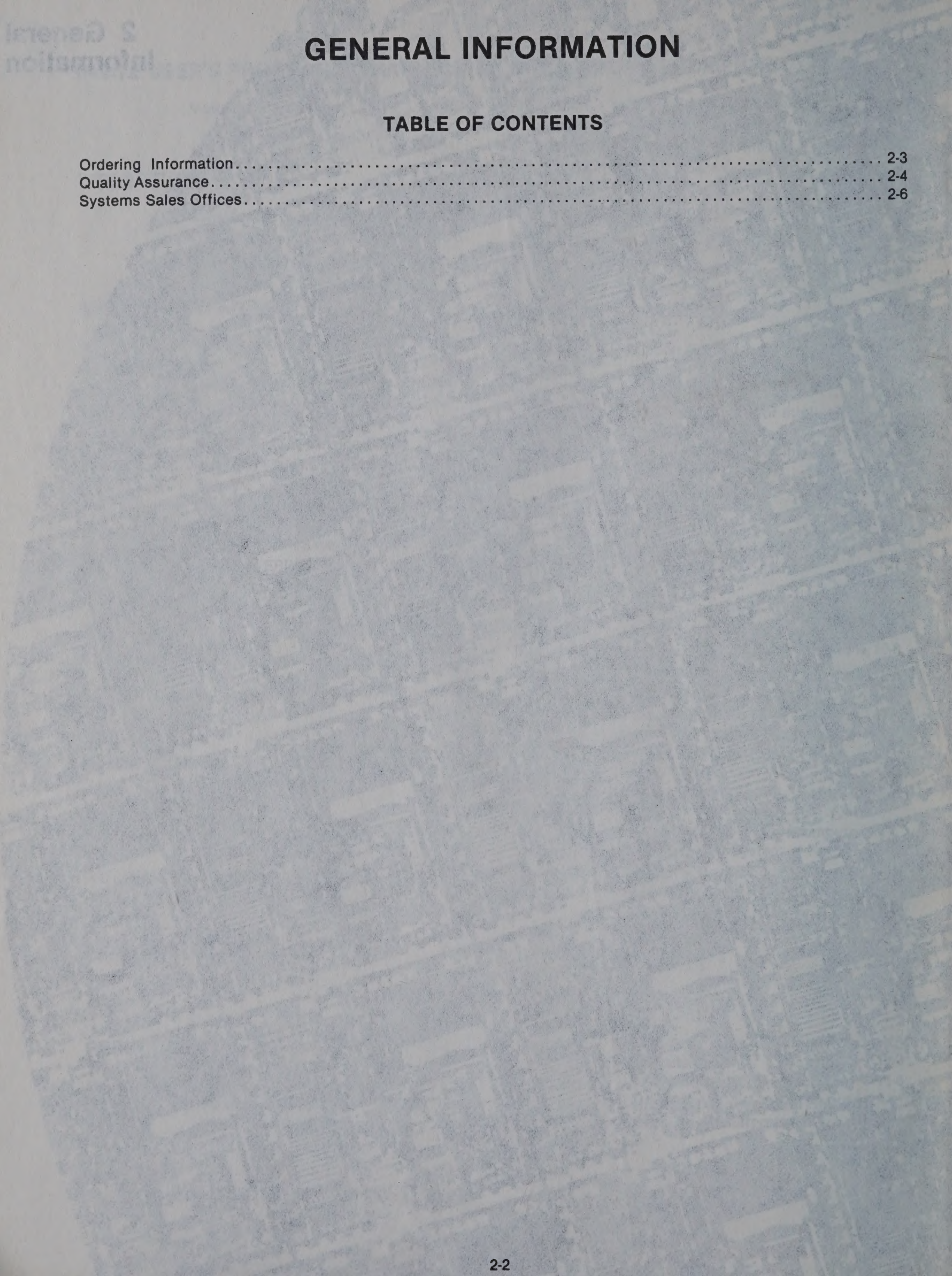


ORDERING INFORMATION

PART NUMBERS

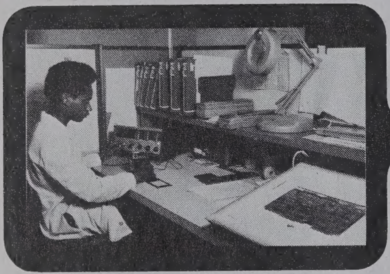
All products described in this catalog, including boards, systems, kits, and other peripheral support equipment, may be ordered using the part or model number designations listed under Ordering Information on each data sheet.

OPTIONS

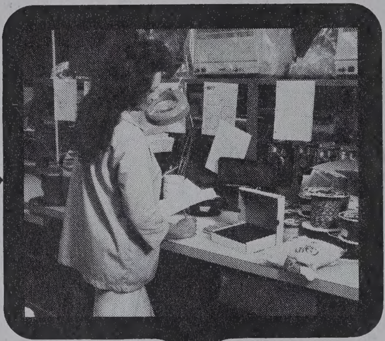
The latest Intel OEM price list should be consulted for availability of various options. It may be obtained by your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

QUALITY ASSURANCE

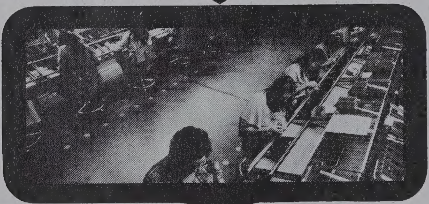
A typical product flow

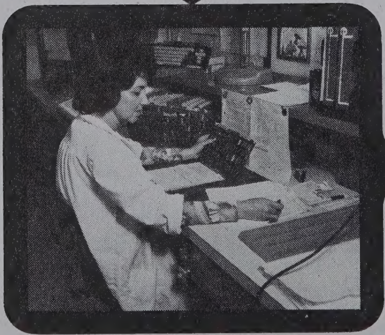


Gold Thickness Measurement on Raw Boards

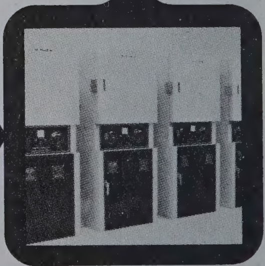


Kit Audit

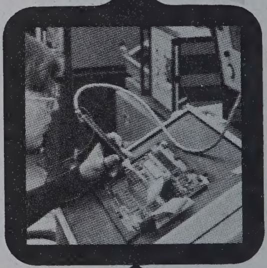




Visual Inspection of Printed Wire Assemblies

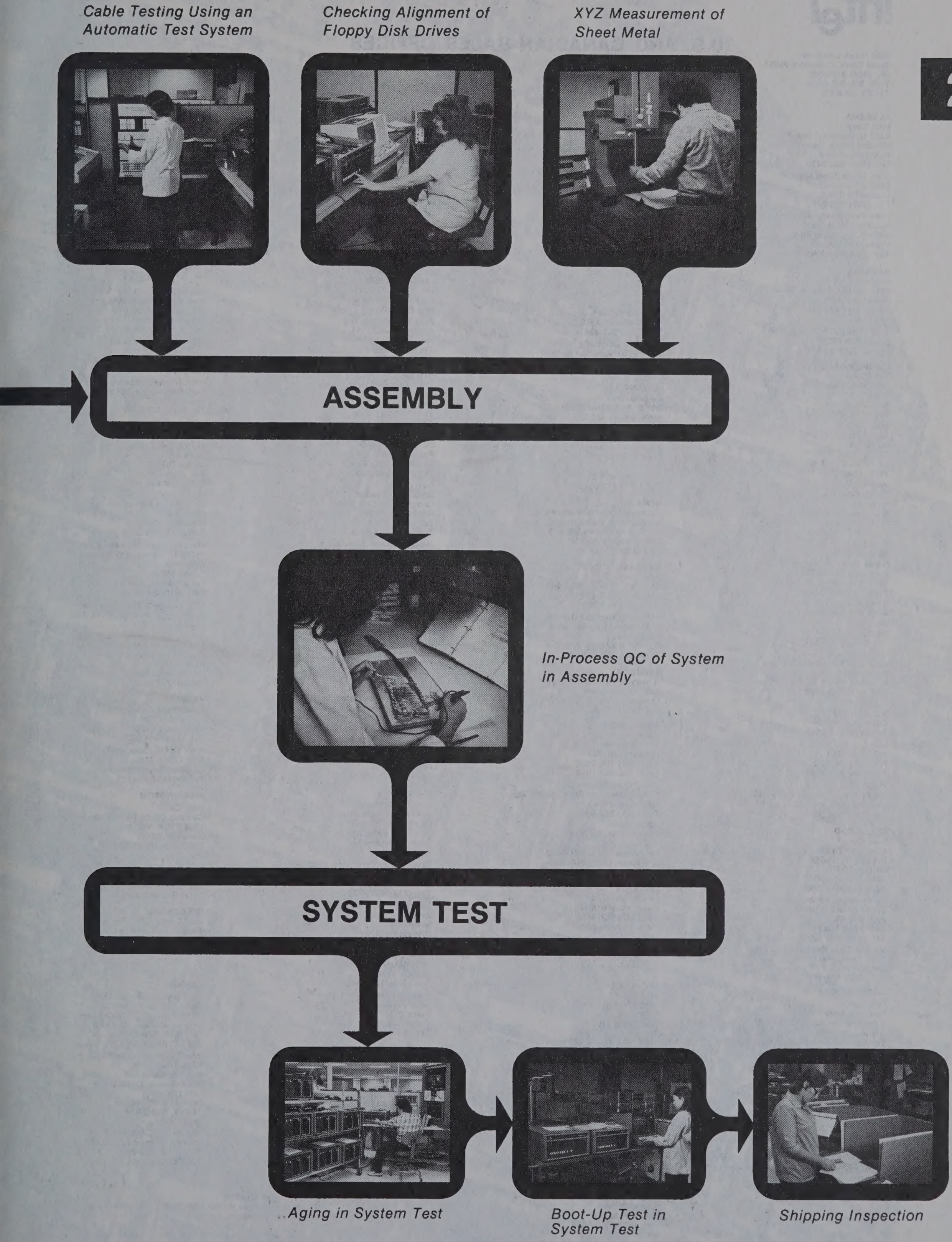


Ovens Utilized for Board Pre-Bake



Single Board Computer Test Fixture

Automatic Test Systems Utilized in Board Testing


Cable Testing Using an Automatic Test System
Checking Alignment of Floppy Disk Drives
XYZ Measurement of Sheet Metal
ASSEMBLY
In-Process QC of System in Assembly
SYSTEM TEST
Aging in System Test
Boot-Up Test in System Test
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*Field application location
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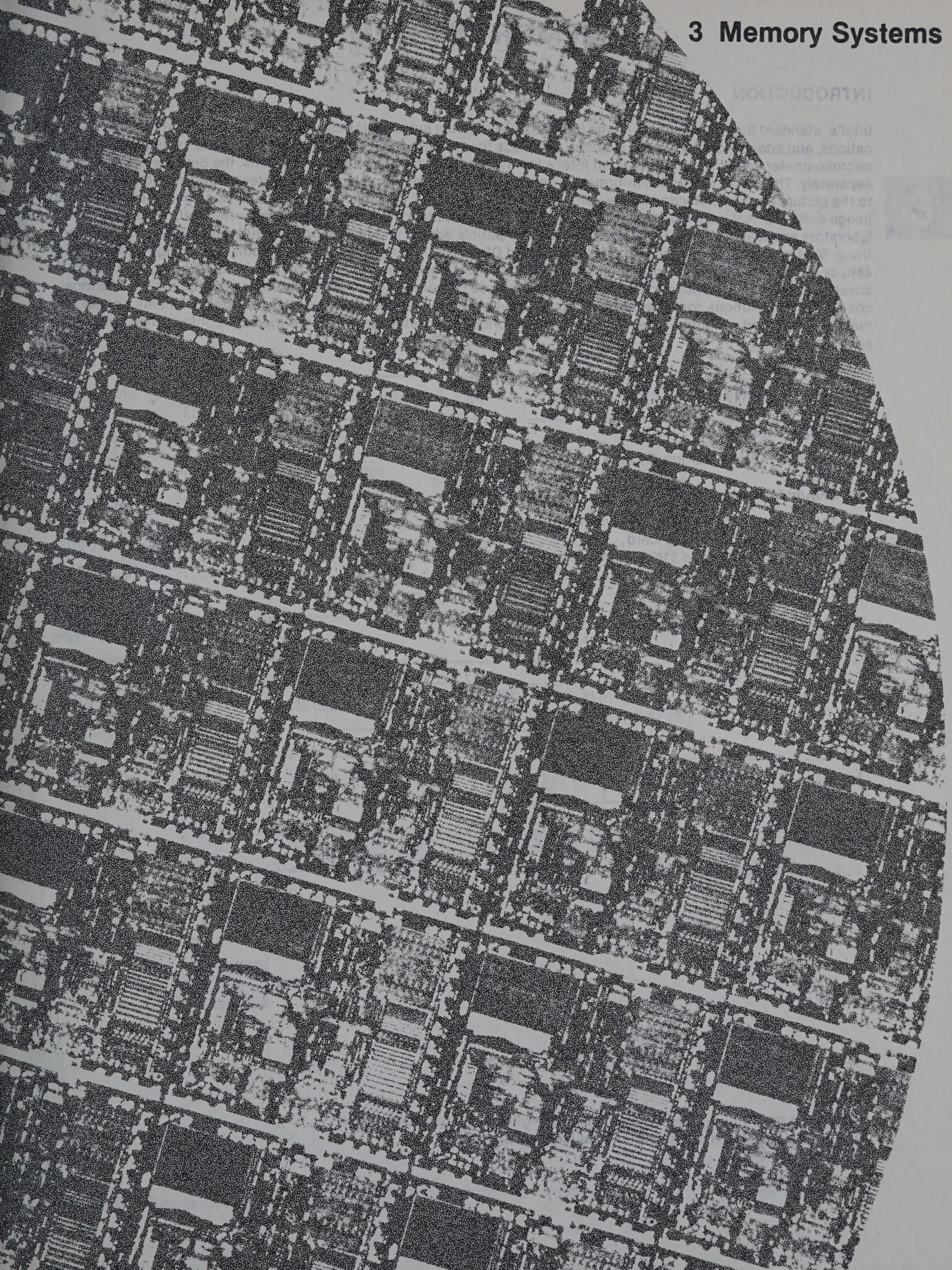
3 Memory Systems



MEMORY SYSTEMS

INTRODUCTION

Intel's standard line of memory systems include OEM memory systems for use in general and special purpose applications, and add-on/add-in memory systems and cards for use with DEC* and DG** minicomputer systems and DEC* microcomputer systems. Information on Intel's family of general purpose memory systems, the Series 90, is available separately. This section provides information on the in-5770, a video refresh memory system providing 4-bit resolution to the picture elements of video images projected onto raster-scan CRT display terminals, is designed specifically for image-enhancement applications in conjunction with sophisticated, computer-driven medical, scientific, and laboratory applications such as X-rays. The DEC-compatible add-on/add-in memories include the in-1670, in-5004, and the in-5034, a single hex height card offering users of DEC PDP* -11/04, 11-34 and 11/60 computers a high density 32K, 48K, or 64K x 18-bit memory with built-in reliability and low power consumption features. These standard products cover a wide range of applications, and because they use proven designs manufactured in volume, provide the most cost-effective solutions for most applications. However, in applications whose specialized requirements cannot be met with standard products, Intel designs and manufactures customized systems in exact conformance with user specifications.

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Memory Systems

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Add-On/Add-In Memories

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in-5004 LSI-11 Add-In Memory Card 3-15
in-5034 PP-11/04, 11/34, and 11/60 Add-In Memory Card 3-17
in-5160 Nova 3 Add-In Memory Card 3-21

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**Nova is a registered trademark of Data General Corporation.

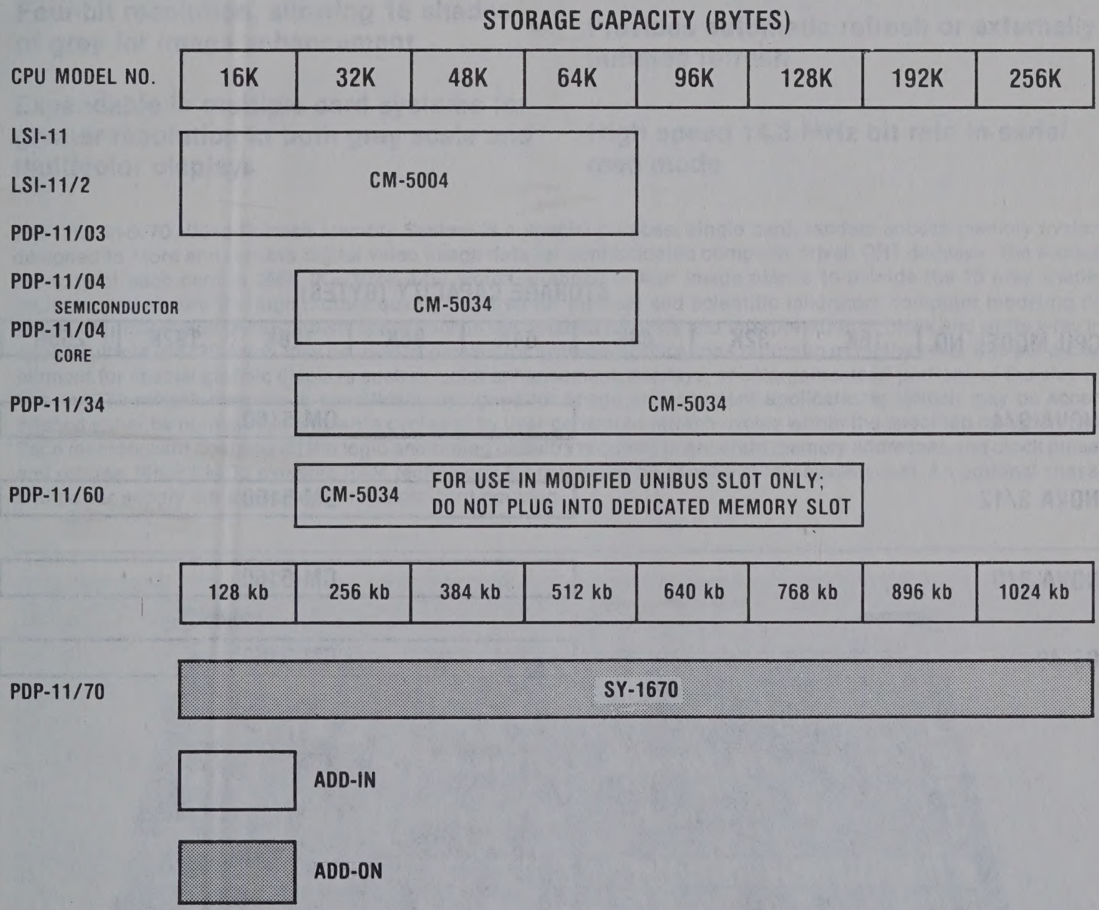

STORAGE CAPACITY (BYTES)
CPU MODEL NO.
16K
32K
48K
64K
96K
128K
192K
256K
LSI-11
LSI-11/2
PDP-11/03
CM-5004
PDP-11/04
SEMICONDUCTOR
PDP-11/04
CORE
CM-5034
PDP-11/34
CM-5034
PDP-11/60
CM-5034
FOR USE IN MODIFIED UNIBUS SLOT ONLY;
DO NOT PLUG INTO DEDICATED MEMORY SLOT
128 kb
256 kb
384 kb
512 kb
640 kb
768 kb
896 kb
1024 kb
PDP-11/70
SY-1670
ADD-IN
ADD-ON

Figure 1. DEC-Compatible Product Selection Guide

<table>
<tr><th></th><th colspan="8">STORAGE CAPACITY (BYTES)</th></tr>
<tr><th>CPU MODEL NO.</th><th>16K</th><th>32K</th><th>48K</th><th>64K</th><th>96K</th><th>128K</th><th>192K</th><th>256K</th></tr>
<tr><td>NOVA 3/4</td><td></td><td></td><td></td><td colspan="5">CM-5160</td></tr>
<tr><td>NOVA 3/12</td><td></td><td></td><td></td><td colspan="5">CM-5160</td></tr>
<tr><td>NOVA 3/D</td><td></td><td></td><td></td><td colspan="5">CM-5160</td></tr>
<tr><td>CS-40</td><td></td><td></td><td></td><td colspan="5">CM-5160</td></tr>
</table>

Figure 2. DG-Compatible Product Selection Guide.

in-5770
VIDEO REFRESH MEMORY SYSTEM

Single card memory system complete with addressing and timing logic

256K-word × 4-bit capacity in four image planes, each 256K × 1 bit wide

Four-bit resolution, allowing 16 shades of grey for image enhancement

Expandable in multiple card systems for greater resolution in both grey scale and multicolor displays

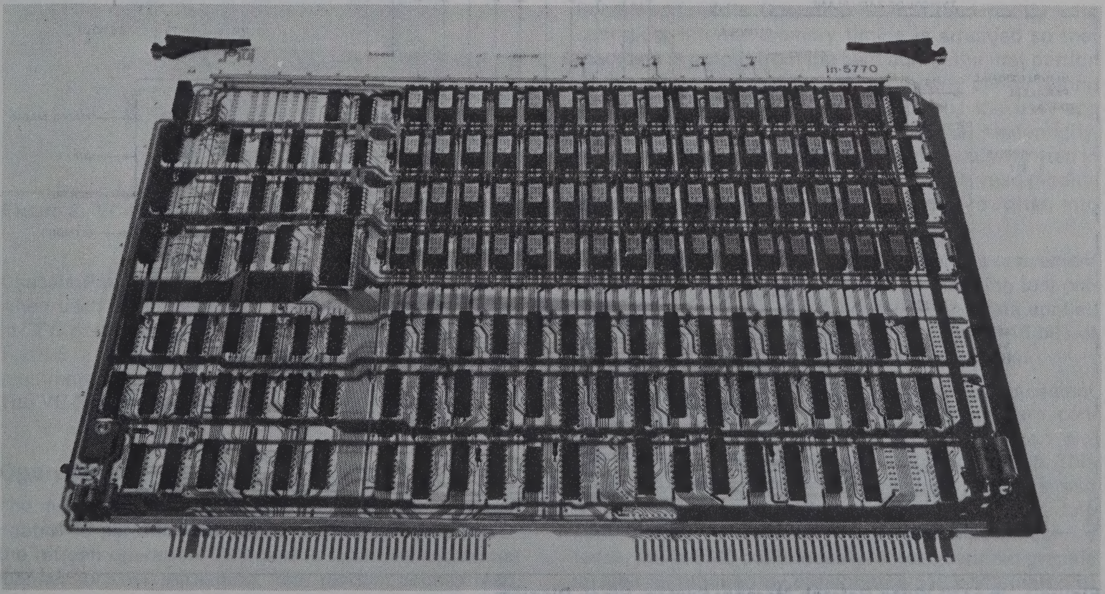
Utilizes MOS dynamic RAMs for maximum bit density at low system cost

Operates in both parallel and single bit mode control

Provides automatic refresh or externally initiated refresh

High speed 14.3 MHz bit rate in serial read mode

The Intel in-5770 Video Refresh Memory System is a special purpose, single card, random access memory system designed to store and retrieve digital video image data for sophisticated computer driven CRT displays. The storage capacity of each card is 256K (K = 1024) 4-bit words arranged in four image planes to provide the 16 grey shades necessary to ensure the high picture quality required for medical and scientific laboratory computer modeling displays; a typical image enhancement application is the detailed analysis and interpretation of black and white x-ray images. Multiple in-5770 cards may be used in parallel for systems applications requiring more than four bits per picture element for special graphic displays such as color enhancement, overlays, or enlargements of portions of the display. The in-5770 refresh memory is specifically designed for image enhancement applications; refresh may be accomplished either by normal read and write cycles or by user generated refresh cycles within the specified retention time. Each memory card contains all the logic and timing circuitry required to generate memory addresses and clock pulses, and utilizes 16K × 1 MOS dynamic RAM technology for maximum bit density at low system cost. An optional chassis and power supply are available for multiple card housing.



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FUNCTIONAL DESCRIPTION

The in-5770 is a video refresh random access memory card system designed specifically for storing and retrieving digital video image data with high resolution, but also used for conventional storage applications. The complete system consists of one 16 × 11.25-inch edge connector type printed circuit card containing the semiconductor storage area and all the required address and data latches and control logic needed to operate the memory. The two standard configurations are 512 × 512 using Intel's 16K × 1 dynamic MOS RAM and 512 × 256 using the 8K × 1 dynamic MOS RAM. The memory is arranged in four planes either 16K × 16 or 8K × 16. A block diagram of the in-5770 memory system is shown in Figure 1.

Capacity

Each CM-5770 memory card has the capacity to store a 512 × 512 display with four bits per picture element. The two standard configurations are 512 × 512 × 4 (CM-5770-512) and 512 × 256 × 4 (CM-5770-256). The memory storage area in the 512 × 512 version consists of 64 Intel 16K × 1 dynamic N-channel MOS RAM silicon gate memory chips. The 16,384 storage cells on each chip are arranged in a 128 × 128 array requiring seven row and seven column addresses to select one cell. Each cell holds one bit of information. The memory chips are arranged in four rows of 16 chips each, with each 4 × 4 block of chips representing one 16K × 16 plane of data. The memory storage area in the 512 × 256 version uses 64 Intel 8K × 1 dynamic N-channel MOS RAM memory chips with 8192 storage cells arranged as a 64 × 128 array. The 8K RAMs are partial 16K devices with only one half of the array operational. The in-5770 memory capacity may be expanded using up to a maximum of 24 CM-5770 cards per system.

Chassis Option

To accommodate a wide range of memory capacities, Intel offers a number of chassis options, available as standard equipment. The in-5770 system, whose outer dimensions and card outline are shown in Figure 2, may be mounted in the optional VC-5770 vertical chassis.

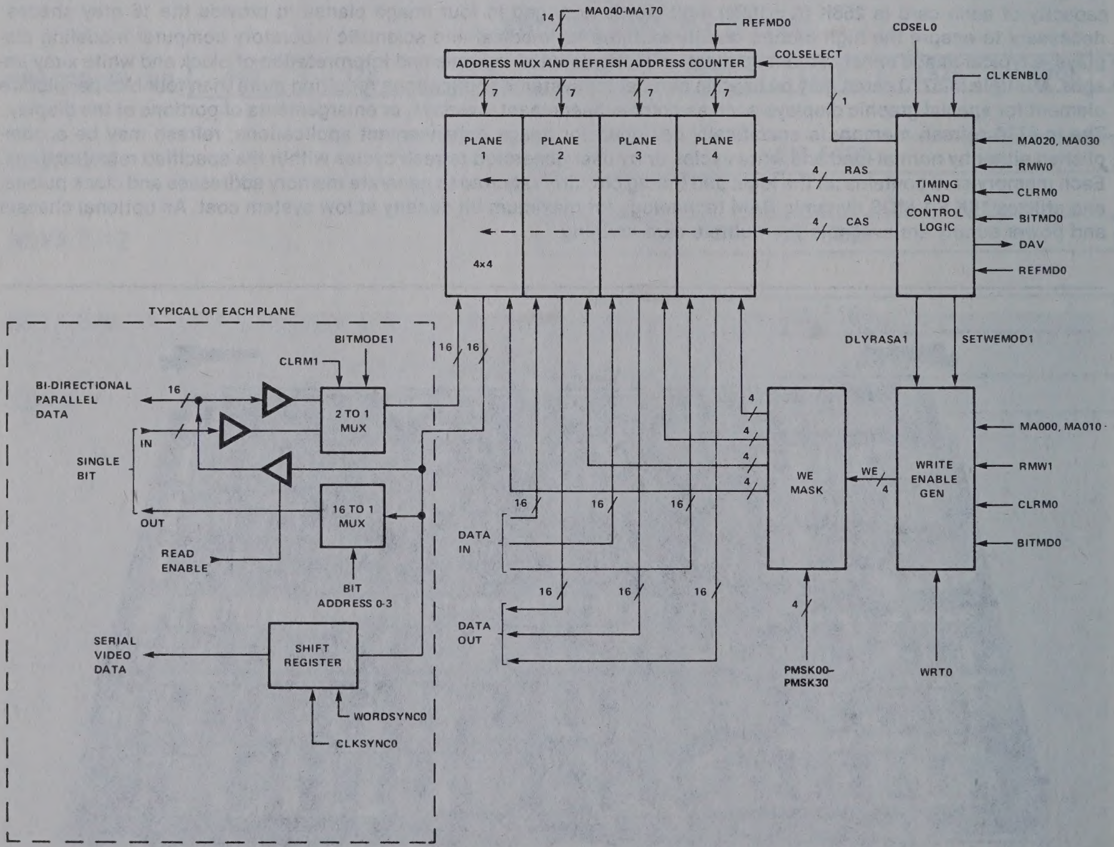

14
MA040-MA170
REFMDO
CDSELO
ADDRESS MUX AND REFRESH ADDRESS COUNTER
COLSELECT
CLKENBLO
7
7
7
7
1
PLANE 1
PLANE 2
PLANE 3
PLANE 4
4x4
4
RAS
4
CAS
TIMING AND CONTROL LOGIC
MA020, MA030
RMWO
CLRMO
BITMDO
DAV
REFMDO
TYPICAL OF EACH PLANE
BITMODE1
CLRM1
16
16
BI-DIRECTIONAL PARALLEL DATA
16
2 TO 1 MUX
IN
SINGLE BIT
OUT
16 TO 1 MUX
READ ENABLE
BIT ADDRESS 0-3
SERIAL VIDEO DATA
SHIFT REGISTER
WORDSYNCO
CLKSYNCO
DLYRASA1
SETWEMOD1
4
4
4
4
WE MASK
WE
4
WRITE ENABLE GEN
MA000, MA010
RMW1
CLRMO
BITMDO
16
16
16
DATA IN
16
16
16
DATA OUT
4
PMSK00-PMSK30
WRTO

Figure 1. in-5770 Video Refresh Memory System Block Diagram

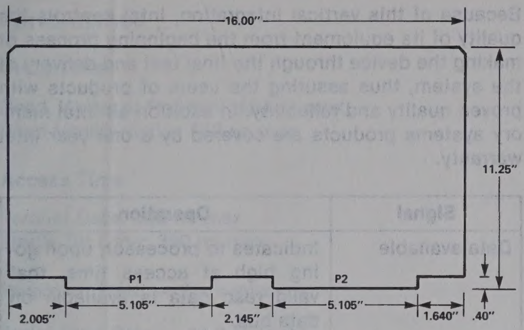


Figure 2. in-5770 Card Dimensions

Vertical CRT Chassis — The VC-5770 (as shown in Figure 3) is a 24-slot chassis used for a combination of in-5770 CRT refresh memories and custom control interface card mounted vertically. The UT-5770 utility card may also be used with the in-5770 to provide custom logic. Power supplies and cooling fans are not included. Power is supplied by the in-CPS series of power supplies.

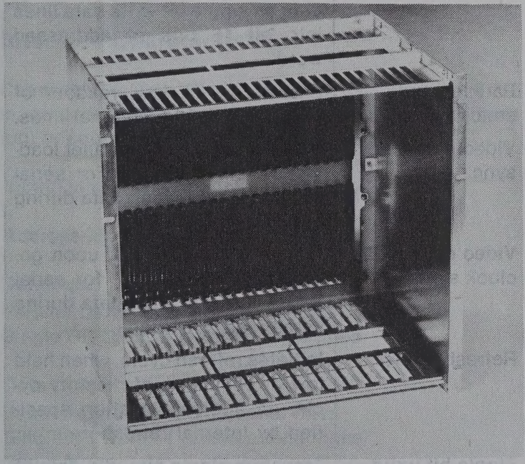


Figure 3. VC-5770 Vertical CRT Chassis Unit

Chassis Power Supply — For the VCRT chassis option when used with the in-5770 CRT refresh memory card, in-CPS power supplies are recommended, as shown in Table 5. Four models are available to satisfy the power requirements of a range of memory cards from 1 to 24. The VC-5770 has space for up to 24 in-5770 cards.

VC-5770 (qty)	Power Supply Model	Power Supply Drawers
1-4	in-CPS-1	1
5-8	in-CPS-2	1
9-16	in-CPS-3	1
17-24	in-CPS-4	1

Note
Power must be specified if other than 110V AC, 50/60 Hz.

Table 1. in-CPS Power Supplies

Operation

The in-5770 provides both parallel and single bit mode control to perform four basic memory operations plus the refresh operation. The card is read in a sequential manner for CRT refreshing, with random access read, write, or read-modify-write operations performed in between the CRT refresh reads. During a CRT refresh read, 16 bits of data from each plane are read on the memory card and are internally converted to serial bit lines, clocked at 70-nanosecond or longer intervals.

Read Operation — In all read modes, a full 16-bit data word is read out from the addressed location in each memory plane. During parallel read operations, a 16-bit data word is read from each plane of the memory array and placed on the output lines, 64 lines in all, resulting in 64 bits being simultaneously available at the interface. During serial read operations, 16 bits from each memory plane are loaded into shift registers and transferred out serially on four output lines. During single bit read operations, a 16-bit word is read from each of the four memory planes, but only one bit from each plane is transferred to the single bit output lines.

Write Operation — In write modes, 64 bits of data are stored in the location specified by the address inputs. During parallel write operations, 64 bits are received at the interface, and stored as four 16-bit words, one in each memory plane. The parallel write mode writes a 16-bit data word selectively in any or all of the planes, under control of a plane select mask. During single-bit write operations, four bits (one pixel) are received at the interface and stored with one bit in each memory plane.

Read-Modify-Write Operation — In a read-modify-write operation, internal memory timing is arranged so that read data is output from the card during the first portion of the cycle, followed by a 90 ns modify period during which a new data word is generated by the user and stored in the memory. During a parallel read-modify-write operation, a full 16-bit word is read and rewritten in each memory plane. During a single bit read-modify-write operation, a single bit is read and rewritten into each memory plane.

Clear Operation — A clear mode provides a convenient way for clearing the screen and for generating test patterns. During a clear mode operation, the data applied on the single bit input lines is written into all 16 bits of the selected address in all four memory planes.

Video Refresh Operation — In image enhancement applications, photographic or video images are converted to a matrix of picture elements with binary elements designating the intensity assigned to each. This information is sent from the computer to the refresh memory and stored for later CRT display. Since data sent directly to a screen from the computer quickly fades, the in-5770 continuously recreates stored graphic images as required by projecting a 512 × 512 matrix of shaded picture elements onto the CRT screen.

Memory Refresh Options — All rows of memory devices within the in-5770 must be refreshed once every 2 milliseconds to prevent loss of data. The refresh operation takes place automatically during serial read for video refresh. However, if normal read operations do not use all 128 chip rows within the memory, refresh cycles must be externally initiated. Data refreshing in N-Channel MOS RAMs is normally achieved by sequentially scanning the memory at the rate of 128 times each 2 milliseconds.

Interface

Input/Output — All in-5770 input/output signals are compatible with TTL integrated circuits. The input and output signal operations for the in-5770 are summarized in Tables 2 and 3, respectively.

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring the users of products with proven quality and reliability. In addition all Intel memory systems products are covered by a one year Intel warranty.

Signal	Operation
Data available	Indicates to processor, upon going high at access time, that valid read data is available on data bus.
Single bit data (0–3)	Transfer single bit read data out of memory on four unidirectional lines.
Serial video data (0–3)	Transfers serial video data out of memory on four unidirectional lines.

Table 3. in-5770 Output Signal Operations

Signal	Operation
Addresses (0–17)	Controls address selection of both single bit data and parallel data on 18 bidirectional lines.
Card select	Enables memory activity on card when low.
Memory cycle start	Initiates memory cycle upon going from high to low.
Bit mode	Indicates to memory, when low, that single bit write cycle or read-modify-write cycle is to be performed. Enables parallel operation when high.
Write	Initiates write operation when held low at beginning of memory cycle.
Read-modify-write	Initiates read operation when held low at beginning of memory cycle. Initiates write operation after 90 ns delay. Writes user supplied data into location initially read out.
Plane select write mask	Inhibits writing operation, when driven low during write or read-modify-write operation on data within given planes, on all data within that plane.
Clear mode	Initiates write operation, when held low at beginning of cycle, of data on single bit write data lines into all 16 bits of addressed word.
Parallel read enable	Enables, when low, readout of data onto 64 bidirectional lines.
Video data load sync	Enables, when low, parallel loading of shift registers for serial transfer out of video data during serial read operations.
Video data serial clock sync	Clocks shift registers, upon going from low to high, for serial transfer out of video data during serial read operations.
Refresh mode	Initiates refresh cycle, when held low at beginning of memory cycle, on address location specified by internal refresh counter.
Single bit write data (0–3)	Transfers single bit write data to memory on four bidirectional lines, 16 for each plane.
Parallel memory data (0–15)	Transfers parallel data to and from memory on 64 bidirectional lines, 16 for each plane.

Table 2. in-5770 Input Signal Operations

SPECIFICATIONS

Storage Capacity

256K × 4 bits, addressable as 64-bit words (16 bits per image plane), or as 4-bit words (1 bit per image plane)

Word Length

16 bits on the parallel bus per image plane
1 bit on the single bit bus per image plane
1 bit on the serial data bus per image plane

Performance

Cycle Time

Read, Write, or Refresh: 450 ns max
Read-Modify-Write: 780 ns max

Access Time

Parallel Data: 380 ns max
Single Bit Data: 390 ns max

Retention Time — 2 ms max

Serial Data Rate — 14.3 MHz max

Operational Modes

Parallel write (16 bits)
Parallel read-modify-write (16 bits)
Single bit write
Single bit read-modify-write
Parallel read (16 bits)
Single bit read
Serial read
Clear mode write
Memory refresh

Interface Characteristics

Connector — Two 80-pin double-sided PC edge, 0.125 in. centers, type SAE 8100 (Stanford Applied Engineering) or equivalent

Input/Output — TTL compatible (single ended)

Address Input — 18 binary lines

Data Input

Parallel Data: 64 bidirectional lines
Single Bit Data: 4 unidirectional lines

Data Output

Parallel Data: 64 bidirectional lines
Single Bit Data: 4 unidirectional lines
Serial Mode Data: 4 unidirectional lines

Control Input — 17 lines: memory cycle start, write, single bit mode, read-modify-write, card select, refresh, plane select write masks 0 through 3, clear mode, parallel read enable 0 through 3, serial data clock, serial data load enable, video data load sync

Control Output — Data available

Interface Signals

Input

Low: −1.0V to +0.8V @ 2 mA
High: +2.2V to +5.5V @ 100 μA

Output

Low: −0.5V to +0.5V @ 15 mA
High: +2.4V to +5.2V @ 200 μA

Physical Characteristics

Card

Width: 11.25 in. (28.58 cm)
Length: 16 in. (40.64 cm)
Weight: 2 lb (1 kg)
Mounting Centers: 0.625 in. (1.59 cm)

Chassis

Width: 19 in. (48.26 cm)
Height: 17.5 in. (44.45 cm)
Depth: 11.5 in. (29.21 cm)

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Current (max)
+12V	2.5A
+5V	2.75A
−5V	100 mA

Environmental Requirements

Temperature — 0°C to 55°C operating ambient, −40°C to 125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 40,000 ft max, non-operating

Cooling — 200 linear ft per minute

Optional Accessories

IC-10 — 96-pin interface connector

EX-5770 — Extender card

UT-5770 — Utility card

IN-BA — Blower assembly (for VC-5770 only)

VC-5770 — Vertical mount chassis/cardcage with unwired backplane to accommodate up to 24 CM-5770 cards.

Reference Manuals

TM-5770-000 — in-5770 Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5770-512	256K × 4	512 × 512 × 4 video refresh memory system card
CM-5770-256	128K × 4	256 × 512 × 4 video refresh memory system card
VC-5770	—	Chassis with universal backplane to accommodate up to 24 CM-5770 cards
UT-5770	—	Utility card
EX-5770	—	Extender card

in-1670
PDP*-11/70 ADD-ON MEMORY SYSTEM

Total hardware and software compatibility with PDP-11/70

128K-bytes storage capacity expandable to 1024K bytes in 128K-byte increments

User access to full PDP-11/70 address space at 3,932,160 bytes

MOS RAMs provide high density memory with low system cost

Two-way memory system interleaving

ECC and error coding for single bit error correction and double bit error detection

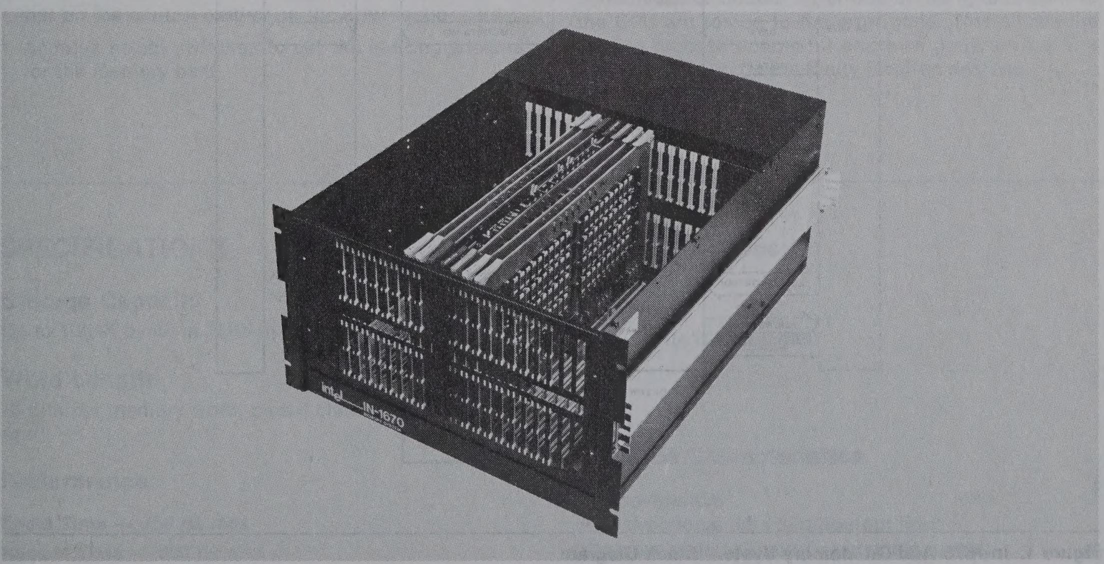
High speed CPU data transfer rate

- **— cycle time: 750 ns**
- **— access time: 555 ns**

Installation and maintenance available from Intel

UL recognition

The Intel in-1670 PDP-11/70 Add-On Memory System is a monolithic memory system offering up to one megabyte of add-on memory for PDP-11/70 users, thus improving PDP-11/70 system performance with increased capacity, increased data transfer-speed, improved functional and component reliability, and reduced cost. The complete in-1670 system utilizes four types of printed circuit cards: memory unit cards, control unit cards, data cards, and error logging cards. All components are fully hardware and software compatible with the DEC* central processing unit (CPU) and are engineered to meet or exceed the specifications of similar DEC components. The Intel in-1670 is used in PDP-11/70 computer systems as a direct replacement for the memory module (MK-11) supplied by DEC, and uses cables and interface signals identical to those used in DEC memory modules. The unit may be installed without change or modification to the DEC software, CPU, memory bus, or I/O structure. High density memory is provided by dynamic MOS RAM devices, and is expandable in 128K-byte increments to 1024K bytes. High speed 750-nanosecond read and write cycle times allow the maximum utilization of Unibus data throughput. The in-1670 system includes error coding and correction (ECC), error monitoring, and error logging.



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FUNCTIONAL DESCRIPTION

The in-1670 semiconductor memory system is specifically designed as an add-on memory for the DEC PDP-11/70 processor. The basic memory device is a monolithic integrated circuit using N-channel MOS transistors. The complete system uses four types of printed circuit cards: 1) control cards containing address and control circuitry; 2) data cards to provide interfacing and parity checking for read and write data; 3) error logger cards to monitor and log data error conditions; and 4) memory cards (MU-167As) for storage. Each memory module contains its own power supply and cooling. All on-line operating sequences are controlled by processor supplied controller signals and by internally generated response signals sent to the processor from the memory, and all system components are engineered to meet or exceed the specifications of similar DEC components. A simplified block diagram of the in-1670 memory system is shown in Figure 1.

Compatibility

The in-1670 is specifically designed for use in PDP-11/70 computer systems as a direct replacement for the DEC-supplied memory module (MK-11), and uses cables and address, data, and interface control signals identical to those in DEC memory modules. The unit may be installed in the DEC central processing unit (CPU) memory cabinet without change or modification to the DEC software, CPU, memory bus, or I/O structure. All system voltages, currents, timing, and I/O signal requirements are compatible with the PDP-11/70.

Capacity

Card Capacity — Each memory card in the in-1670 memory system has a capacity of 64K bytes. Two memory cards make up the basic 128K-byte storage in increments of the in-1670 memory system. A fully expanded memory system contains 1024K bytes. Interleaving is possible between two memory systems with the same capacity.

System Capacity — The storage area of the in-1670 system consists of 16 Intel MU-167A memory system units. Each MU-167A contains 80 Intel 2109 8K dynamic MOS RAMs to rpovide a capacity of 32K words by 20 bits per card. The 16 MU-167A's in the system are configured to provide 256K words of storage with a double-word 40-bit interface. Thirty-two of the bits are assigned to data and eight of the bits to error correction and coding (ECC). These systems are housed in a chassis along with power supplies and fan assemblies. Up to four such chassis may be mounted in one equipment rack and interfaced in daisy-chain fashion with the processor.

Expandability — Each unit is easily field upgradable to larger capacities with the addition of memory cards or a memory rack containing cards. A diagram showing CPU and memory cabinet dimensions is shown in Figure 2.

System Components

The in-1670 consists of four basic printed circuit cards for memory storage, control, data transfer, and error logging, all housed in a system chassis with power sup-

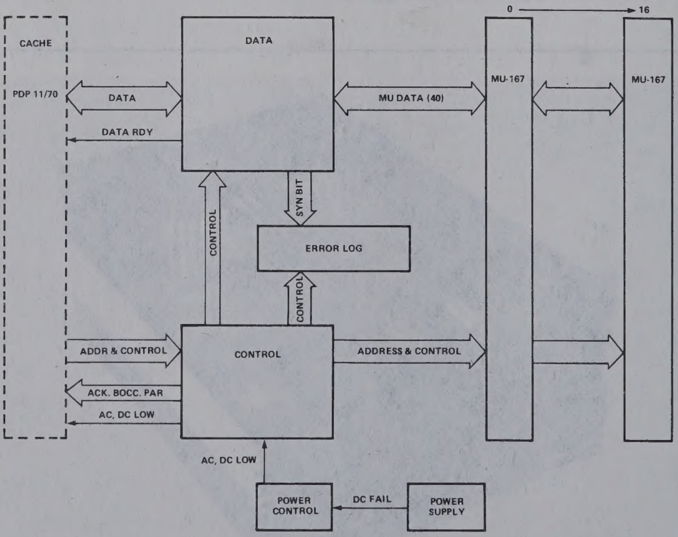


Figure 1. in-1670 Add-On Memory System Block Diagram

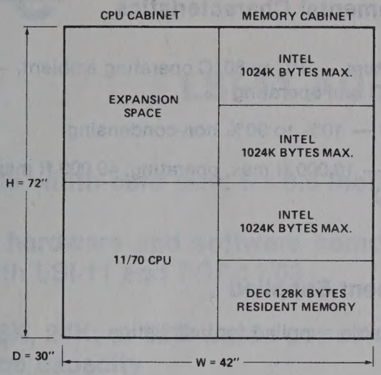


Figure 2. PDP-11/70 CPU Cabinet and in-1670 Add-On Memory Cabinet Dimensions

plies and fan assemblies. Up to four chassis may be mounted in one equipment rack and interfaced in daisy-chain fashion with the processor.

Maintainability

The in-1670 memory system provides convenient controls, reconfiguration switches, and status indicators as standard maintainability features, all located to provide easy maintenance access to the user.

Rear Panel Controls — The following controls are located on the rear panel of the memory module:

- AC circuit breaker
- Three power supply output voltage adjustments

Card Controls — The following controls are located either on the control card or on the error logger card:

- Address select switches to set the starting address for the memory bank
- Memory on-line/off-line switch to disconnect the in-1670 from the PDP-11/70 memory bus
- Reset logic switch
- Error logger on/off switch
- Lamp test
- ECC on/off switch
- Error logger scan switch

Card Indicators — The following indicators are provided either on the control card or on the error logger card:

- Address parity error indicator
- Mismatch error indicator
- Write data parity error indicator
- Address display
- Syndrome bits display
- Single bit mode or double bit mode indicator
- On-line/off-line mode indicator

Reliability

Error Correction Coding — The Intel in-1670 memory system includes error correction coding (ECC) as a standard feature. The ECC logic detects single bit memory errors and automatically corrects a single bit failure prior to read operation. Since most memory errors are due to single bit failures, ECC provides a 10 to 25 times improvement in memory system reliability over systems with parity checking only. During write operations, ECC logic removes parity bits from the input data word and generates error correction code bits to be stored with the data word. When write data is received from the processor, it is checked for correct parity before being written into memory. During a read operation, the word is checked for correct status. The ECC circuitry automatically corrects the incorrect bit should a single bit be detected. A double bit error in the read word is not corrected. For double bit errors, all parity bits sent to the CPU are forced to the error state. This allows the CPU to process double bit errors as parity errors. The ECC logger records the faulty location address.

SPECIFICATIONS

Storage Capacity

Up to 1024K bytes in 128K-byte increments

Word Length

16 bits per memory word, plus 8 check bits per double word

Performance

Cycle Time — 750 ns max
Access Time — 555 ns max

Operational Modes

Read
Write
Partial write (1 or 2 bytes)

Interface Characteristics

TTL compatible
36 bidirectional data input/output lines
23 binary address input lines (single ended)

Installation Requirements

All cables and connectors supplied by Intel
1 DEC memory cabinet (21"W × 30"D × 72"H)
1 in-1670 memory card

Notes

1. Installation can be done by the customer or purchased from Intel.
2. Maintenance contracts are available from Intel.

Physical Characteristics

Width — 10.5 in. (26.3 cm)
Height — 10.5 in. (26.3 cm)
Depth — 25.0 in. (77.5 cm)
Weight — Less than 70 lb (54 kg)

Electrical Characteristics

AC Power Requirements

Requirement	115V AC (max)	230V AC (max)
Voltage	90V AC to 140V AC	170V AC to 260V AC
Frequency	45 to 440 Hz single phase	45 to 440 Hz single phase
Input current	6.5A max	3.3A max

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, −40°C to +85°C non-operating

Humidity — 10% to 90% non-condensing

Altitude — 10,000 ft max, operating; 40,000 ft max, non-operating

Equipment Supplied

Ribbon cable supplied for installation

Reference Manuals

TM-1670-000 — in-1670 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
SY-1670-128	128K bytes (64K words)	Add-on memory system for PDP-11/70
SY-1670-256	256K bytes (128K words)	Same as above except capacity
SY-1670-384	384K bytes (192K words)	Same as above except capacity
SY-1670-512	512K bytes (256K words)	Same as above except capacity
SY-1670-640	640K bytes (320K words)	Same as above except capacity
SY-1670-768	768K bytes (384 words)	Same as above except capacity
SY-1670-896	896K bytes (448K words)	Same as above except capacity
SY-1670-1MB	1024K bytes (512K words)	Same as above except capacity
XF-1670-128	128K bytes	Expansion for in-1670 PDP-11 Add-On Memory System
EX-1670	—	Card extender
XX-1670-001	—	Memory card
XX-1670-002	—	Data interface card
XX-1670-003	—	Control card
XX-1670-004	—	Error logger card
XX-1670-005	—	Terminator board
XX-1670-006	—	Power control card
XX-1670-007	—	I/O cable assembly
XX-1670-008	—	Power supply
XX-1670-009	—	Diagnostic memory test. Includes magnetic tape.
XX-1670-010	—	Branch spare kit containing one each EX-1670 and XX-1670-001 through XX-1670-009

in-5004
LSI-11 ADD-IN MEMORY CARD

Double width card size: 5 × 8.5 inches

Total hardware and software compatibility with LSI-11 and PDP-11/03

8K, 16K, 24K, or 32K words per card storage capacity

Optional 18-bit word length for byte parity

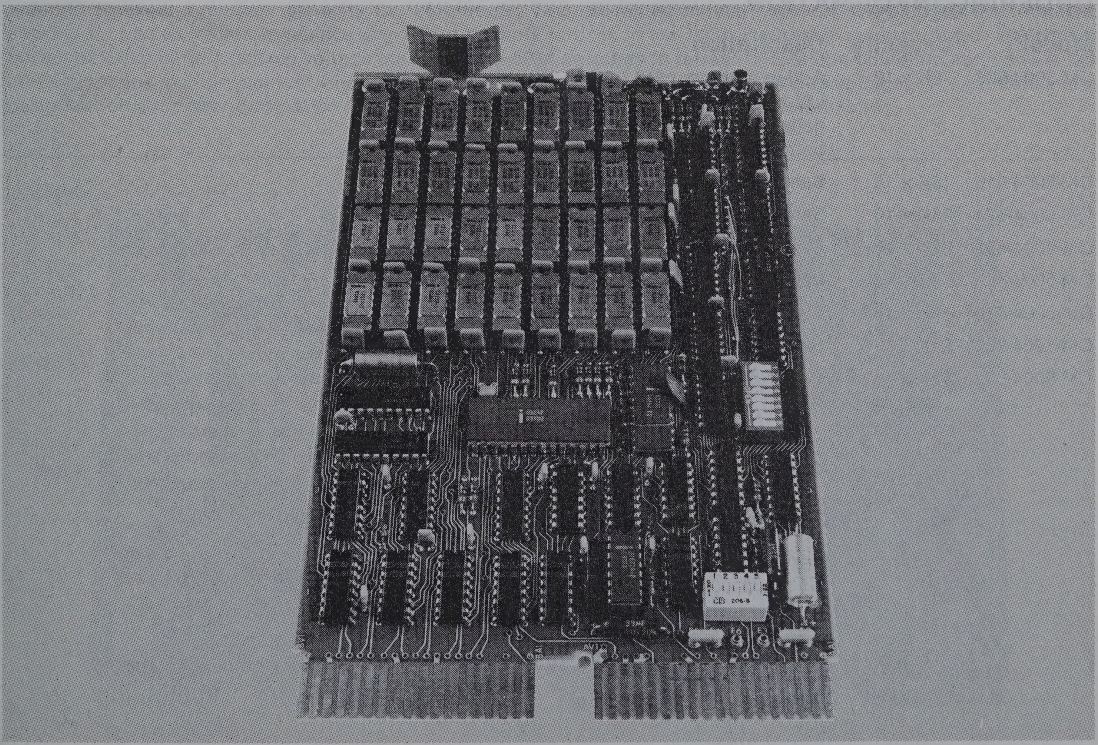
Dynamic MOS RAMs provide high density memory with low system cost

On-board switch selectable addressing

Selectable on-board or external refresh

Battery backup capability

The Intel in-5004 LSI-11 Add-In Memory Card is a plug-compatible memory module designed for use with DEC* LSI-11, LSI-11/2, and PDP*-11/03 microcomputer systems. Utilizing dynamic MOS RAM devices, the in-5004 is available in 8K, 16K, 24K, and 32K-word × 16-bit capacities. An optional 18-bit word length is available for byte parity. The in-5004's on-board refresh circuitry may be user disabled in applications requiring an optional external refresh operation. Repositioning the appropriate jumpers will also reconfigure the in-5004 to accept external battery backup voltage inputs. Address segments of the in-5004 are switch selectable from 0 to 32K, in 4K increments. For simplified installation, each 4K segment is enabled by a single switch. A 28K, 30K, 31K, or 32K upper address limit may also be selected for maximum memory utilization.



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SPECIFICATIONS

Storage Capacity

8K, 16K, 24K, or 32K words

Word Length

16 bits per word with optional 18-bit word length available for byte parity

Performance

Cycle Time — 550 ns max

Access Time

Read: 250 ns typ, 325 ns max (BSYNCL to BRPLY)

Write: 150 ns typ, 200 ns max (BDOUTL to BRPLY)

Operational Modes

Read
Write
Read-modify-write

Physical Characteristics

Width — 8.5 in. (21.3 cm)
Length — 5 in. (12.7 cm)

Electrical Characteristics

DC Power Requirements

Power (±5%)	Operating (max)	Standby (max)
System Power		
+5V ±5% +12V ±5%	0.9A typ (1.4A) 0.35A 11W	0.9A typ (1.4A) 0.075A 8W
Battery Backup Power		
+5V ±5% +12V ±5%	0.3A typ (0.50A) 0.075A	

Environmental Characteristics

Temperature — 0°C to +50°C operating ambient, −40°C to +125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-5004-000 — in-5004 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5004-608	8K × 16	Add-in memory card for LSI-11, LSI-11/2, and PDP-11/03. User selectable on-board refresh and battery backup modes
CM-5004-616	16K × 16	Same as above except capacity
CM-5004-624	24K × 16	Same as above except capacity
CM-5004-632	32K × 16	Same as above except capacity
CM-5004-808	8K × 18	Same as above except capacity
CM-5004-816	16K × 18	Same as above except capacity
CM-5004-824	24K × 18	Same as above except capacity
CM-5004-832	32K × 18	Same as above except capacity

in-5034

PDP*-11/04, 11/34 ADD-IN MEMORY CARD

Total hardware and software compatibility with PDP-11/04 and PDP-11/34

16K, 32K, 48K, or 64K words × 18 bits per board storage capacity

Single hex height card contains all address and control circuitry

8K and 16K MOS RAMs provide high density memory with low system cost

On-board switch selectable addressing

On-board parity checking and generation

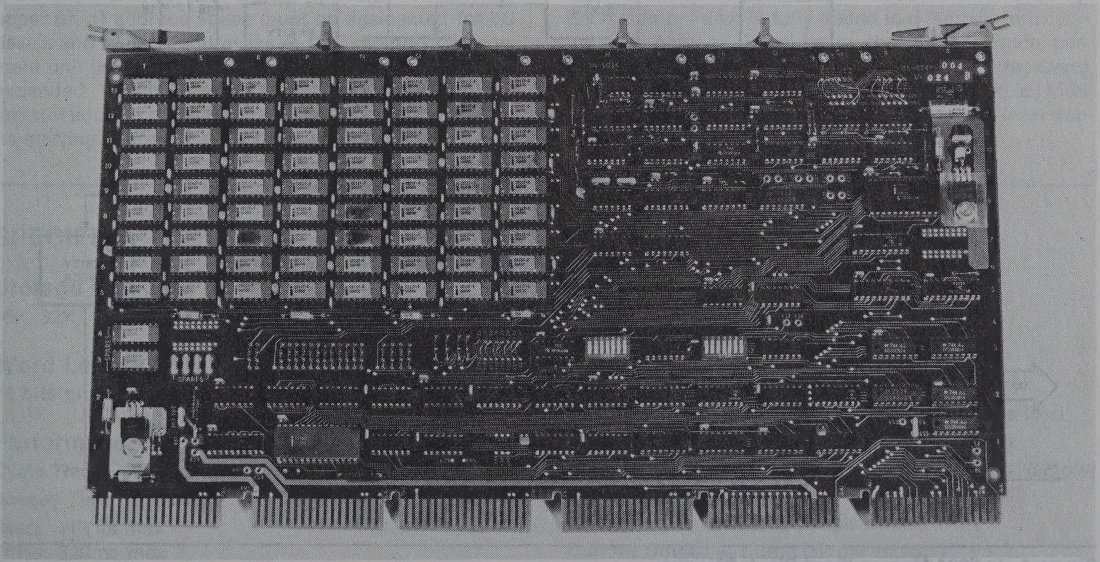
On-board control status register (CSR)

Battery backup capability

Low power dissipation for higher system reliability

Spare on-board memory chips

The Intel in-5034 PDP-11/04, 11/34 Add-In Memory Card is a plug-compatible memory module designed for use with any DEC* PDP-11/04 or PDP-11/34 modified unibus* slot. The complete in-5034 memory system, with all address and control circuitry, is contained on a single hex height printed circuit card requiring only one modified Unibus* slot. All system components are fully hardware and software compatible with PDP-11 systems and may be installed, without change or modification to the DEC software, CPU, memory bus, or input/output structure. High density memory is provided by 16K dynamic MOS RAM components, and is expandable in 16K-word increments to 64K words. High speed 600-nanosecond read and write cycle times allow maximum utilization of modified Unibus throughput. The system provides on-board parity checking and generation and an on-board control status register (CSR). The parity check and the CSR function perform for the in-5034 memory the equivalent of DEC's parity controller module function. Dual-in-line package (DIP) switches on the module select the desired Unibus address ranges and provide the addressing inputs required to expand memory capacity to 128K words. Two pre-tested memory devices are plugged into on-board sockets for use as spares to replace any failing memory devices in the field. Provisions are included on the card to accept external battery backup voltage inputs. The in-5034 switches to refresh cycles upon detection of a power failure, and retains memory content when provided +5V, +15V, and −15V battery backup voltages. The system is also designed for low power dissipation and consumption, resulting in improved system reliability.



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FUNCTIONAL DESCRIPTION

The in-5034 semiconductor memory module consists of a single hex-height printed circuit card specifically designed to plug into a modified Unibus slot, and containing all circuitry required for memory operation, including data circuitry, address circuitry, mode enable and byte control logic, timing logic, control logic, refresh control circuitry, a control status register, a memory storage area, and a parity generator and checker. All operating sequences are controlled by processor supplied signals and by internally generated response signals sent to the processor from the memory. All system components are engineered to meet or exceed the specifications of similar DEC components. A simplified block diagram of the in-5034 memory card is shown in Figure 1.

Compatibility

The in-5034 is specifically designed for use with the DEC PDP-11 family of computer systems, and is fully compatible with all PDP-11/04 and PDP-11/34 computers. The in-5034 memory module consists of one modified Unibus compatible printed circuit card assembly that plugs directly into a single system unit card slot. The system unit slot may be any of slots 2 through 8 of PDP-11/34 or either of slots 2 or 3 of PDP-11/04, as shown in Figure 2. The in-5034 uses cables and interface control, address, and data signals identical to those used in DEC memory modules. The unit may be installed in the DEC central processing unit (CPU) memory cabinet without change or modification to the DEC software, CPU, memory bus, or I/O structure. Jumper options are provided to select compatibility with either the core or semiconductor memory, to select or deselect the battery backup capability, and to enable or disable the control status register. All other system voltages, currents, timing, and I/O signal requirements are compatible with both the PDP-11/04 and PDP-11/34.

Capacity

Each memory card has a basic maximum capacity of 64K words by 18 bits, with one word consisting of two 8-bit data bytes (upper and lower) plus one parity bit per byte, i.e., 16 bits plus two parity bits per card. The card may be depopulated to provide 16K, 32K or 48K words of storage, as required. The storage area in the memory consists of 72 8K or 16K dynamic N-channel MOS RAM silicon gate memory chips. The 8K memory chip has a capacity of 8K words by one bit; the 16K, a capacity of 16K words by one bit. The in-5034 memory capacity may be expanded in 16K-word increments to a total of

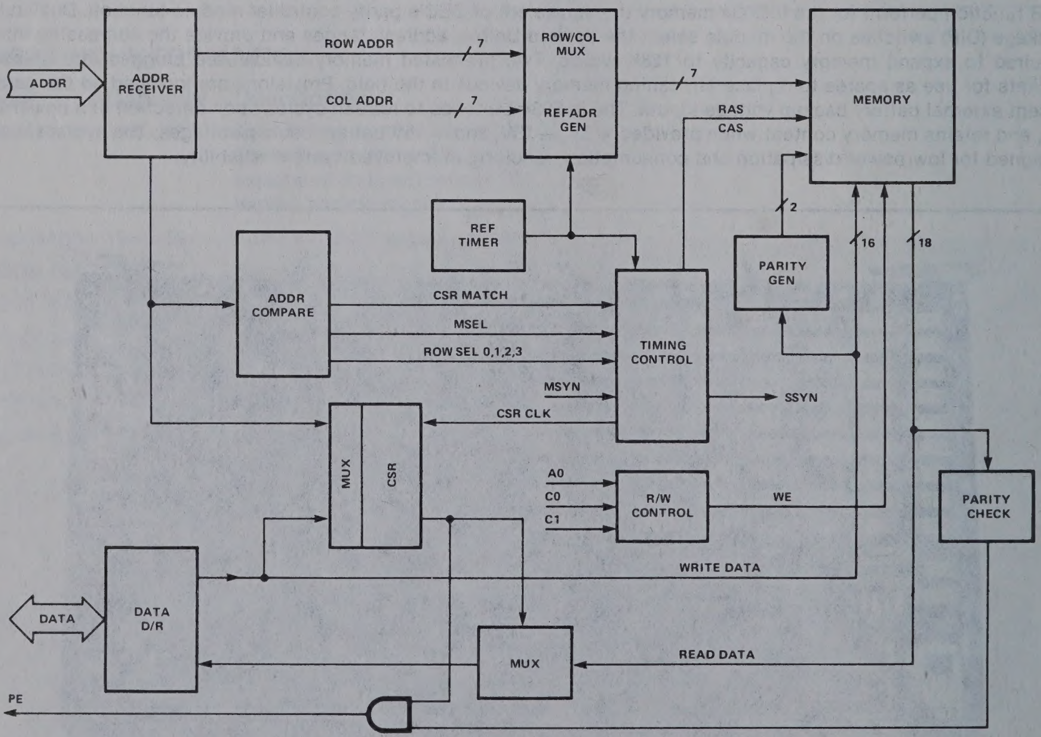


Figure 1. in-5034 Memory/Card Block Diagram

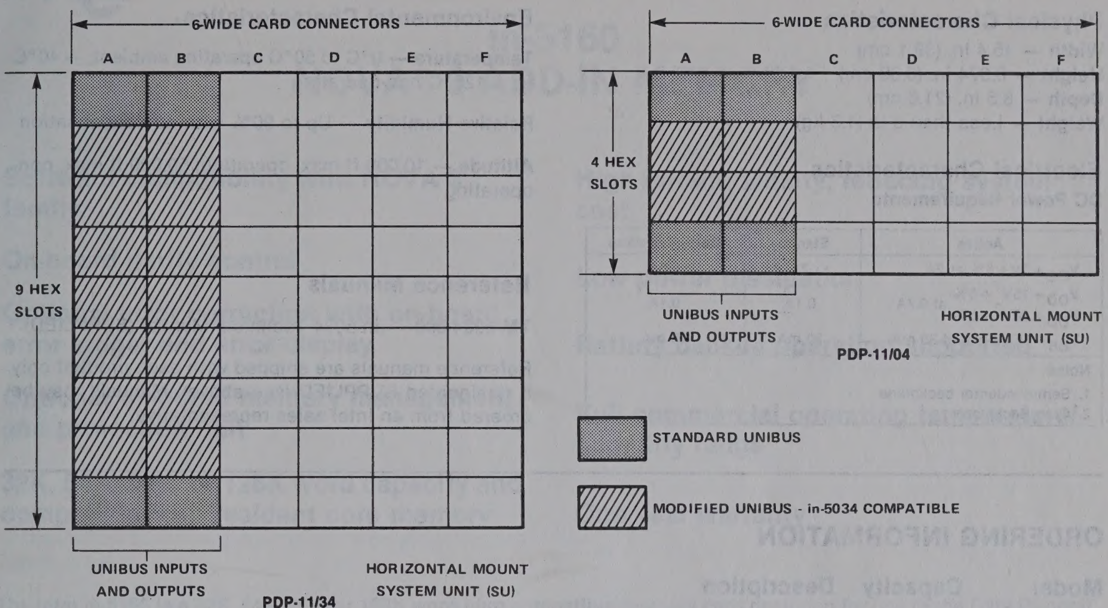

6-WIDE CARD CONNECTORS
A
B
C
D
E
F
9 HEX SLOTS
UNIBUS INPUTS AND OUTPUTS
HORIZONTAL MOUNT SYSTEM UNIT (SU)
PDP-11/34
6-WIDE CARD CONNECTORS
A
B
C
D
E
F
4 HEX SLOTS
UNIBUS INPUTS AND OUTPUTS
HORIZONTAL MOUNT SYSTEM UNIT (SU)
PDP-11/04
STANDARD UNIBUS
MODIFIED UNIBUS - in-5034 COMPATIBLE

Figure 2. in-5034 Installation in PDP-11/34 and PDP-11/04 System Unit Card Slots

64K words. However, use of a total memory capacity exceeding 28K words requires the use of a DEC-supplied memory management unit.

Addressability

The address range for each module is set by on-board dual-in-line package (DIP) switches. The memory module starting address is selectable to any 8K boundary and the ending address is selectable to any 4K boundary. Each memory module provides addressing inputs to allow expansion to 128K words, although normally the upper 8K of address space must be deselected for I/O device and register addresses. A DEC memory management unit is required when the total system memory is expanded beyond 28K words. The control status register address of each memory board is determined by its starting address (set by DIP switches).

Reliability

The in-5034 is designed for low power dissipation. When operating at full speed in a PDP-11/04 or PDP-11/34, the 64K in-5034 dissipates 87 BTUs/hour, in standby 43 BTUs/hour, and in the battery backup mode 17 BTUs/hour, resulting in a cooler running system, an increased margin for power supply operation, and improved system reliability. Since the in-5034 dissipates less power than the equivalent DEC core or semiconductor memory, no special provisions are necessary for cooling. Each memory card is fully tested in a temperature cycling environment. Because of the 100% burn-in performed on each card, the user is assured of receiving Intel's proven quality and reliability. In addition, all Intel compatible products are covered by a one-year Intel warranty.

SPECIFICATIONS

Storage Capacity

16K, 32K, 48K, or 64K words per card

Word Length

16 bits plus 2 parity bits

Performance

Cycle Time — 600 ns max

Access Time

Read: 410 ns max
Write: 320 ns max

Operational Modes

Read
Write
Read byte
Write byte

Interface Characteristics

Interface — Modified Unibus compatible, 1 bus load

Address Input — 18 binary lines (single ended)

Data Input/Output — 18 bidirectional lines (single ended)

Control Input — 3 lines (single ended)

Control Output — 1 line (single ended)

Physical Characteristics

Width — 15.4 in. (39.1 cm)
Height — 0.374 in. (0.09 cm)
Depth — 8.5 in. (21.6 cm)
Weight — Less than 3 lb (1.3 kg)

Electrical Characteristics

DC Power Requirements

Active	Standby	Battery Backup
V_{CC} + 5V ± 5% at 2A	2A	0.5A
V_{DD} + 15V[1] + 5% at 0.7A V_{DD} + 20V[2] + 5%	0.1A	0.1A
V_{BB} − 15V ± 5% at 30 mA	20 mA	20 mA

Notes
1. Semiconductor backplane
2. Core Backplane

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, −40°C to +125°C non-operating

Relative Humidity — Up to 90% with no condensation

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-5034-000 — in-5034 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from an Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5034-816	16K × 18	Add-in memory card for PDP-11/04 and PDP-11/34
CM-5034-832	32K × 18	Same as above except capacity
CM-5034-848	48K × 18	Same as above except capacity
CM-5034-864	64K × 18	Same as above except capacity

in-5160
NOVA* 3 ADD-IN MEMORY

Software compatibility with NOVA 3 family

On-board parity control

Optional error correction with on-board error logger and error display

Optional on-board memory management and protection unit

32K, 64K, 96K, or 128K word capacity and compatible with resident core memory

High circuit density, reducing system cost

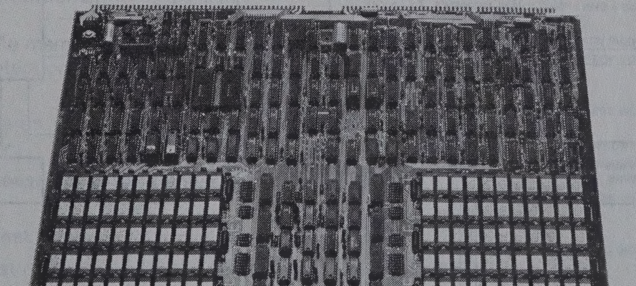
Low power dissipation

Battery backup operation supported

Full commercial operating temperature/ humidity range

One year warranty

The Intel in-5160 is a 32K, 64K, 96K, or 128K word plug compatible memory card designed for use in the Data General NOVA 3 computer. It is totally hardware and software compatible with the NOVA 3, and configures easily with resident Data General memory boards. All in-5160 control memory, address, parity, bus driving, and voltage regulator circuitry, as well as all options, are contained on one 15-inch × 15-inch printed circuit card, which occupies only one card slot. This high circuit density allows a NOVA 3/4 to be configured with the maximum addressable memory, a memory management unit, the memory protect option, and the parity generate/check option, with two slots left for a disk controller and a serial controller or any other two cards. The in-5160 is designed for low power dissipation and uses a maximum of 50 watts (40 watts typical). In case of power failure the contents of the memory will be retained if a battery backup is provided. With this low power dissipation, no additional cooling fans are required. The parity feature and the optional memory management and protection unit (MMPU) are functionally identical to the corresponding units available from Data General and both features are fully compatible with the NOVA 3 software. The parity feature generates and checks parity on a 16-bit data word and will work not only for the in-5160, but for any other 17-bit memory in the same system. The optional MMPU allows memory addressing and allocation up to 128K words and provides several system protect functions under software control. The optional ECC error check and correction provides error correction facilities on the board along with an error logger. All single bit errors will be corrected; all double bit errors and a significant portion of multiple bit errors are detected.



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FUNCTIONAL DESCRIPTION

The in-5160 NOVA 3 Add-In Memory is a semiconductor memory system specifically designed as a single card add-in containing the maximum amount of memory addressable by existing software. Also on the board are all memory associated system functions previously available only on a separate card, or not available at all: parity generation and checking, memory management, memory protection, error detection/correction, and error logging with error location display. All normal memory functions are also contained on the card: address buffers and decoding logic, data transceivers, control logic, timing, mode enable logic, and refresh control logic. On-line operating sequences are controlled by processor supplied control signals, signals received from data channel devices and by internal control signals. Response signals sent to the central processing unit (CPU) are generated by the parity logic, MMPU, and other control logic circuitry. All system components are engineered to meet or exceed the specifications of similar Data General components.

Compatibility

The in-5160 can be inserted into any NOVA 3 series computer and will work with any 17-bit memory already in the system. If the previous memory has a capacity of 32K words, or a multiple of 32K words, the in-5160 starting address is set to follow the ending address of the existing memory. If the previous memory capacity is not a multiple of 32K words, the in-5160 is set to occupy the address range from zero up to the in-5160 card capacity. The previously installed memory is then set to follow the ending address of the in-5160. For example, a 64K word in-5160 could be used as shown in Table 1.

Condition	Address Range for in-5160	Address Range for Resident NOVA Memory
No previous memory	0-64KW	—
16K resident memory	0-64KW	64KW-80KW
32K resident memory	32KW-96KW	0-32KW
64K resident memory	64KW-128KW	0-64KW

Table 1. in-5160 Memory Address Range

Capacity

The in-5160 is manufactured with two types of memory devices: a 16K × 1-bit dynamic RAM and an 8K × 1-bit dynamic RAM. Both chips are manufactured with NMOS technology and are tested to the same specifications.

Addressability

Card select for the in-5160 is determined by the decode of the three extended address inputs and the settings of the address select switches on the card. These switches enable the card's starting and ending addresses to be set on any 32K word boundaries within the 128K word address field available with memory management. For cards with memory capacity greater than 32K words, the address range must be selected so that the memory occupies contiguous 32K address blocks.

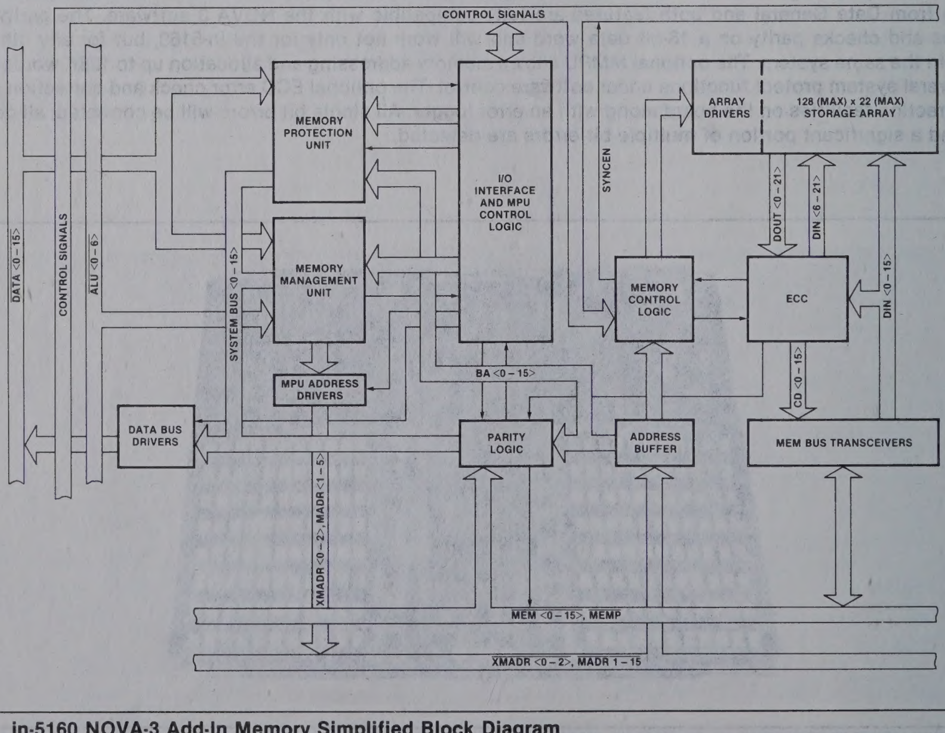

CONTROL SIGNALS
MEMORY PROTECTION UNIT
I/O INTERFACE AND MPU CONTROL LOGIC
ARRAY DRIVERS
128 (MAX) x 22 (MAX) STORAGE ARRAY
SYNCEN
DOUT <0 – 21>
DIN <6 – 21>
DATA <0 – 15>
CONTROL SIGNALS
ALU <0 – 6>
SYSTEM BUS <0 – 15>
MEMORY MANAGEMENT UNIT
MEMORY CONTROL LOGIC
ECC
DIN <0 – 15>
BA <0 – 15>
CD <0 – 15>
MPU ADDRESS DRIVERS
DATA BUS DRIVERS
PARITY LOGIC
ADDRESS BUFFER
MEM BUS TRANSCEIVERS
XMADR <0 – 2>, MADR <1 – 5>
MEM <0 – 15>, MEMP
XMADR <0 – 2>, MADR 1 – 15

Figure 1. in-5160 NOVA-3 Add-In Memory Simplified Block Diagram

Operating Modes

The in-5160 emulates all of the operating modes supported by Data General on the NOVA 3 series computers. In normal operation, the in-5160 performs read, read-hold, write, and read-modify-write processor controlled cycles. Refresh cycles are timed out internally and use chip row addresses generated by a counter on the board. The in-5160 offers the largest storage capacity that can be handled by existing software and has a higher effective speed than the NOVA 3 semiconductor memories. Read or write operations required 500 nanoseconds and the read-modify-write operation is completed in 1100 nanoseconds, whether initiated when the memory is idle or immediately following a preceding cycle. On consecutive memory cycles, the Data General NOVA 3 memory requires 500 nanoseconds for read cycles, 1200 nanoseconds for write cycles and 2200 nanoseconds for read-modify-write. Since consecutive memory cycles occur frequently, the Intel memory can provide significantly faster throughput. The data valid time is extended during the read-hold cycle by the processor pulling the hold input low. The longer data valid time is required during defer cycles, console initiated read cycles (the examine switch), or during data channel read cycles. For data channel memory cycles, the memory operates in either write or read-hold modes. All read, write, or read-modify-write cycles can be performed with or without single bit error correction, map, memory protection, or parity error reset or interrupt.

Memory Management and Protection Unit (MMPU)

Memory expansion — The MMPU provides the capability to use a memory of up to 128K words and supplies the hardware necessary to make use of the NOVA 3 software protection features. The expansion of memory capacity is accomplished by replacing the five highest order address bits (the logical address) with seven bits from a location in the translation memory (the physical address). Each logical address is 'mapped' (or translated) to one, and only one, physical address, which may be anywhere within the 128K physical address field. The contents of the translation memory (the map) may be set up using ordinary I/O instructions.

Memory protection — The memory protection function of the MMPU provides detection capability for five types of software violations:

- **Write protect** — prevents writing into a write protected 1K page
- **Validity** — prevents accessing, in any manner, a page declared invalid
- **Defer** — protects against runaway defer cycles
- **I/O** — enables I/O violation detection in the CPU
- **Auto Index** — Prevents auto-indexing operations.

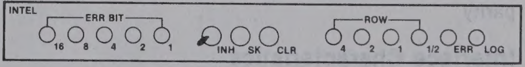
When a violation is detected, the MMPU initiates an interrupt routine in the processor.

Parity

The parity feature is standard on all in-5160 memory boards. During write operations, the parity logic generates a parity bit for the 16-bit data word. Data and parity bit are then stored in the memory. During read operations, 16 bits of data and one parity bit are read out from the memory and checked for a parity error. If a parity error is detected, the address and parity bit are latched in the parity error address register, and either a reset or interrupt signal (jumper selectable) is returned to the processor. The CPU reads the contents of the parity error address register by using standard I/O instructions. The parity feature services not only the in-5160, but all 17-bit memories in the same system. On boards with the ECC option, the parity logic still functions for other 17-bit memories in the system and reports multiple bit errors detected by the ECC logic to the CPU as parity errors.

Error Correction and Error Logger

The in-5160 error correction circuitry (ECC) provides on-board capability to correct any single bit error and detect any double bit error in the read data. Many errors of more than 2 bits will also be detected. ECC greatly increases memory reliability and minimizes non-recoverable system failures. The multiple bit errors are flagged to the processor as parity errors. All errors are logged as they occur and are simultaneously displayed on the in-5160's control panel. The error correction function can be disabled by a switch on the control panel; however, the error logger will continue to monitor and store error information. The chip location of single bit errors and row location of double bit and multiple bit errors are stored in the error logger memory and displayed on LEDs on the control panel as they occur. The error logger controls and indicators are shown in Figure 2.



ERR BIT — THESE INDICATORS SHOW FAULTY DATA BIT (BINARY CODED).
16,8,4,2,1 *EXAMPLE:* INDICATORS 1 AND 4 ON, INDICATES BIT 5 IN ERROR.

SK (SEEK) — PUSHBUTTON SWITCH. WHEN PUSHED AND HELD, PERFORMS LED TEST. WHEN RELEASED, ERROR LOGGING MEMORY IS SEARCHED FOR ERROR INFORMATION.

CLR (CLEAR) — PUSHBUTTON SWITCH. CLEARS ERROR LOGGING MEMORY.

INH (INHIBIT) — TOGGLE SWITCH. IN ON POSITION INHIBITS ERROR CORRECTION FUNCTION. DOES NOT INHIBIT ERROR LOGGER.

ROW — THESE INDICATORS SHOW ROW LOCATION OF FAULTY RAM
4,2,1,½ (BINARY CODED).

LOG — THIS INDICATOR COMES ON TO INDICATE ERROR LOGGING IN PROGRESS.

ERR — INDICATES ERROR IS DETECTED; SINGLE BIT OR DOUBLE BIT/MULTIPLE BIT

Figure 2. Error Logger Control Panel and Indicators

INSTALLATION

The installation of the in-5160 on a NOVA 3 system is covered in detail by the technical manual which accompanies the product. The main points of consideration during installation are address selection and parity error action (RESET or interrupt). The location of these switches and jumpers are illustrated in the manual for easy location.

RELIABILITY

The in-5160 is designed for low power dissipation. When operating with all options, and at full speed in a NOVA 3, the 128K in-5160 dissipates 170 Btu/hr; in battery backup (standby) mode, it dissipates 55 Btu/hr. This results in a cooler running system, an increased margin for power supply operation, and improved system reliability. Every card is fully tested in a temperature cycling environment for eight hours and in a NOVA 3 computer to test all options with the NOVA software. Because of the 100% burn-in performed on each card, the user is assured of receiving Intel's proven quality and reliability. In addition, all Data General compatible products manufactured by Intel are covered by a on year warranty.

SPECIFICATIONS

Storage Capacity

32K, 64K, 96K, or 128K words

Word Length

Standard — 16 data bits and one parity bit
With ECC — 16 data bits and six ECC check bits

Cycle Time

Read or Write Cycle — 500 ns
RMW — 1100 ns

Access Time

300 ns (access and cycle times are extended 100 ns if error correction takes place)

Operating Modes for Memory

Processor — Read, read-hold, write, read-modify-write
Data Channel — Read-hold, write
MMPU — Translation enabled/disabled
Parity — Disabled/generate even parity, generate odd parity

Interface Characteristics

Interface — NOVA-3 backplane compatible, one card slot required

Note: If the in-5160 is equipped with MMPU option, backplane slot 2 is required. If slot 2 is occupied, jumper plugs will be supplied to carry the required signals to any other slot.

Address Input — MADR 1-15: 15 lines; ALU 0-6: 7 lines; DS 0-5: 6 lines
Address Input/Output — MADR 1-15
(Generated in MMPU) X MADR 0-2
Memory Data Input/Output — 16 bidirectional lines
I/O Data Input/Output — 16 bidirectional lines
Control Inputs — 36 lines
Control Outputs — 14 lines

Physical Characteristics

Width — 15 in. (38.1 cm)
Length — 15 in. (38.1 cm)
Height — 0.4 in. (1.02 cm)
Weight — Less than 3 lb (1.36 kg)

Electrical Characteristics

DC Power Requirements (128K, all options)

Voltage (±5%)	Active	Current Battery Backup
+5V	6.1A	1.6A
+15V	890 mA	200 mA
−5V	15 mA	10 mA

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient; −40°C to 120°C non-operating ambient
Relative Humidity — Up to 90% with no condensation
Altitude — 10,000 ft max operating; 50,000 ft max non-operating

Reference Manuals

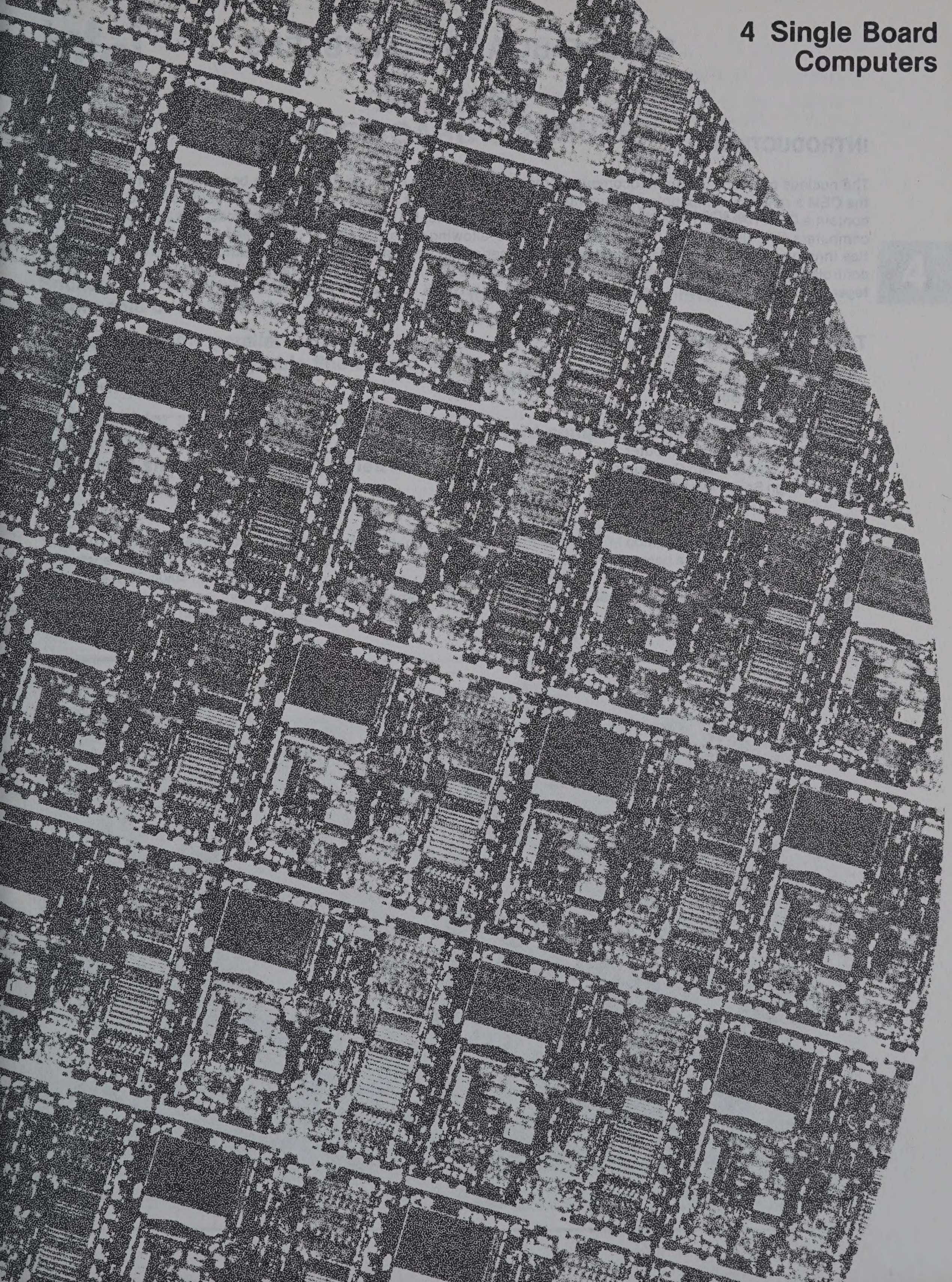
TM-5160-000 — in-5160 Technical Manual, Number 19-1432-000 (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5160A-032	32K × 17-bit	32K memory with parity
CM-5160A-064	64K × 17-bit	64K memory with parity
CM-5160A-096	96K × 17-bit	96K memory with parity
CM-5160A-128	128K × 17-bit	128K memory with parity
CM-5160B-032	32K × 22-bit	32K memory with ECC
CM-5160B-064	64K × 22-bit	64K memory with ECC
CM-5160B-096	96K × 22-bit	96K memory with ECC
CM-5160B-128	128K × 22-bit	128K memory with ECC
CM-5160C-032	32K × 22-bit	32K memory with MMPU
CM-5160C-064	64K × 22-bit	64K memory with MMPU
CM-5160C-096	96K × 22-bit	32K memory with MMPU
CM-5160C-128	128K × 22-bit	128K memory with MMPU
CM-5160D-032	32K × 22-bit	32K memory with ECC and MMPU
CM-5160D-364	64K × 22-bit	64K memory with ECC and MMPU
CM-5160D-096	96K × 22-bit	96K memory with ECC and MMPU
CM-5160D-128	128K × 22-bit	128K memory with ECC and MMPU

4 Single Board Computers



SINGLE BOARD COMPUTERS

INTRODUCTION

The nucleus of Intel's OEM microcomputer product family is the 8-bit and 16-bit single board computers. They offer the OEM a range of compatible microcomputers with a consistent set of capabilities, i.e., all single board computers contain a CPU, RAM, EPROM/ROM capacity, serial and parallel I/O (with stand-alone applications). Intel single board computers offer the MULTIBUS system interface bus, allowing the expansion of the single board computers capabilities through a family of boards, including memory, serial and parallel I/O, analog I/O, communications and peripheral controllers. For increased computational performance, the iSBC 310 High Speed Math Unit offers high speed, fixed integer and floating point arithmetic for the family of MULTIBUS compatible single board computers.

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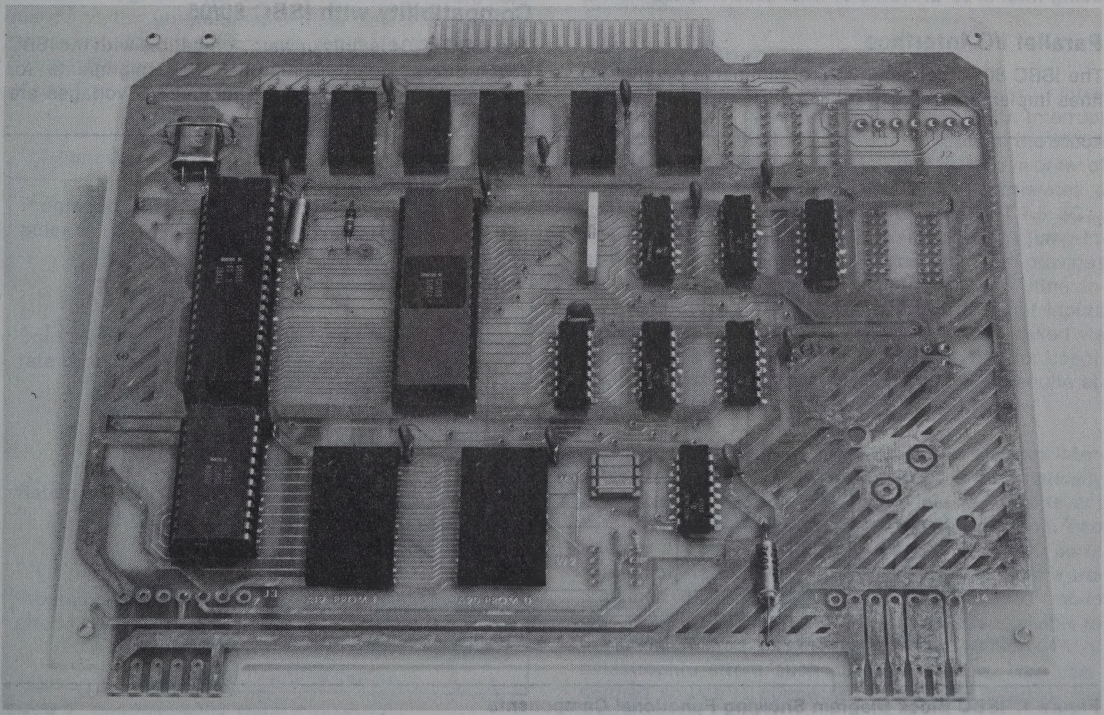
iSBC 80/04
SINGLE BOARD COMPUTER

- **8085A CPU used as central processor**
- **256 bytes of static read/write memory**
- **Sockets for 4K bytes of erasable reprogrammable or masked read only memory**
- **22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators**
- **Optimized for stand-alone applications with provisions for on-board +5V regulator, heat sink, and mounting holes for attachment to user's equipment**
- **Programmable 14-bit binary timer**
- **TTL serial I/O interface with hole patterns for RS232C line drivers and receivers**
- **Four-level vectored interrupt**
- **Upward compatibility with iSBC 80/05**
- **Single +5V power supply**

The iSBC 80/04 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/04 is a complete computer system on a single 6.75 × 7.85-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, and programmable timer all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/04. The 8085A CPU is directly software compatible with the popular intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of iSBC 80/04 functional components is shown in Figure 1.

Memory Addressing

The 8085A CPU has a 16-bit program counter which allows addressing of up to 65,536 bytes of memory. An external stack, located within any portion of iSBC 80/04 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/04 contains 256 bytes of read/write memory using the Intel 8155 RAM/IO/Timer. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2316E masked ROMs. Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 2708 EPROMs or Intel 2608 masked ROMs.

Parallel I/O Interface

The iSBC 80/04 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Stand-Alone Applications

The iSBC 80/04 is designed to be a cost-effective solution for applications requiring a self-contained computer on a single board without the need for external memory or I/O options. In order to help minimize power supply cost in small systems, the iSBC 80/04 includes provision for an on-board + 5V regulator allowing unregulated voltage to be connected directly on the board. Regulated DC voltages are applied to the board through two 12-pin edge connectors which mate with flat, woven, or round cables. The iSBC 80/04 also includes pins that will accept MOLEX-type connectors for connection of regulated DC voltages. Mounting holes are provided in the corners of the iSBC 80/04 board which permit direct attachment to the user's equipment, thereby eliminating the need for cardcage and backplane.

Compatibility with iSBC 80/05

The iSBC 80/04 is fully upward compatible with the iSBC 80/05 Single Board Computer. Pin assignments for parallel I/O, serial I/O, and regulated DC voltages are

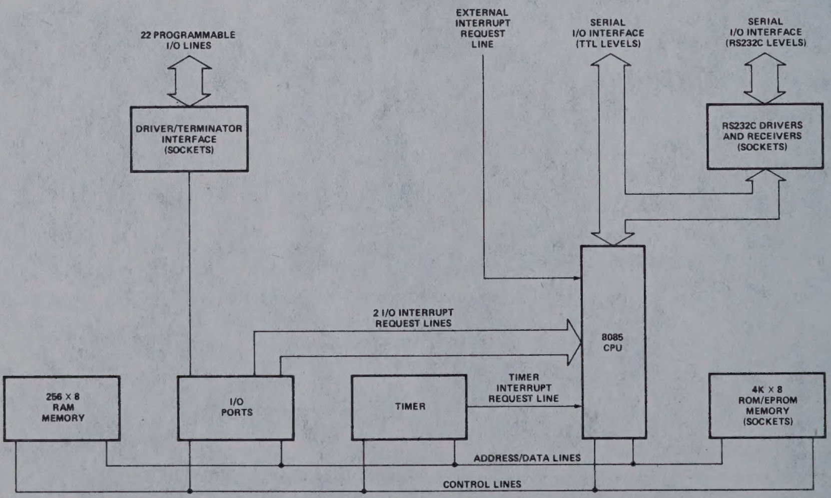

22 PROGRAMMABLE I/O LINES
EXTERNAL INTERRUPT REQUEST LINE
SERIAL I/O INTERFACE (TTL LEVELS)
SERIAL I/O INTERFACE (RS232C LEVELS)
DRIVER/TERMINATOR INTERFACE (SOCKETS)
RS232C DRIVERS AND RECEIVERS (SOCKETS)
2 I/O INTERRUPT REQUEST LINES
8085 CPU
256 X 8 RAM MEMORY
I/O PORTS
TIMER
TIMER INTERRUPT REQUEST LINE
4K X 8 ROM/EPROM MEMORY (SOCKETS)
ADDRESS/DATA LINES
CONTROL LINES

Figure 1. iSBC Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation				
		Unidirectional				Control
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X1
4	3	X		X		X2

Notes

1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.

Table 1. Input/Output Port Modes of Operation

indentical to those of the iSBC 80/05. Additionally, software developed for the iSBC 80/04 will execute directly in the iSBC 80/05. In addition to the iSBC 80/04 features, the iSBC 80/05 contains a total of 512 bytes of read/write memory, allows for expansion of memory and I/O capacity, and provides full MULTIBUS arbitration control for multimaster applications.

Programmable Timer

The iSBC 80/04 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO/Timer. The systems designer simply configures the time via software to meet system requirements. Whenever a given timer delay is needed, software commands to the programmable timer select the desired functions. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out remains high until one-half the count has been completed, and goes low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Table 2. Programmable Timer Functions

Serial I/O Interface

The iSBC 80/04 prvides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085A CPU. These functions are controlled exclusively by software through execution of the 8085A RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the iSBC 80/04 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible, and hole patterns are provided on the board for optional installation of RS232C line drivers and receivers.

Interrupt Capability

The iSBC 80/04 takes advantage of the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed to four interrupt inputs of the 8085A CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 26_{16}, RST 7.5: $3C_{16}$, RST 6.5: 34_{16}, RST 5.5: $2C_{16}$). A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require attention by the 8085A CPU.

Interrupt Generation — The iSBC 80/04 accepts interrupts from four sources. An interrupt is automatically generated by the programmable interval timer/event counter upon completion of the selected function. Two interrupts are automatically generated by the I/O ports section of the 8155 when ports 1 or 2 of the 8155 are programmed to operate in the "latched and strobed" mode (see Table 1). The fourth interrupt source is available to the user and should be used to inform the 8085A CPU of catastrophic errors such as power failure. This user-defined source is connected to the trap input of the 8085A CPU.

Systems Development Capability

The development cycle of the iSBC 80/04-based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/04 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/04.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intellec system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 2.03 μs, ±0.1%

Note
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — 0-0FFF$_H$
RAM — 3F00$_H$

Memory Capacity

ROM/EPROM — 4K bytes (sockets only)
RAM — 256 bytes

I/O Addressing

On-Board Programming I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 3 & 4	8155 Ports	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Serial Communications Characteristics

SID and SOD functions of the 8085 CPU are used for serial I/O. Controlled by software through RIM and SIM instructions of the 8085A CPU. Baud rate determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085 CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Condition	Interrupt Input	Memory Address	Priority	Type
User-defined	TRAP	24_{16}	Highest	Non-maskable
Timer	RST 7.5	$3C_{16}$	↕	Maskable
I/O Port 2	RST 6.5	34_{16}		Maskable
I/O Port 1	RST 5.5	$2C_{16}$	Lowest	Maskable

Timer

Input Frequency Reference — 122.88 kHz ±0.1% (8.14 μs period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter	
	Min	Max
Programmable pulse	8.14 μs	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μs	133.33 ms

Interfaces

Parallel I/O — All signals TTL compatible
Interrupt Request — All TTL compatible (active-low)
Serial I/O — TTL; hole patterns available for user installation of RS232C line drivers and receivers

System Clock (8085 CPU)

1.966 MHz ±0.1%

Connectors

Interface		Pins (no.)	Center (in.)	Mating Connectors[1]
Voltages	+5V, +12V, −5V[2]	12 double-sided	0.156	CDC VPB01E06D00A1
		7 single-sided	0.156	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 09-50-0106 Pin Molex 15-04-0219 Key
				AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key
	+5V, −12V[3]	12 double-sided	0.156	CDC VPB01E06D00A1
		7 single-sided	0.156	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key
				AMP 87149-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key
	Unregulated +5V	2 single-sided	0.156	Molex 09-65-1021 Connector Molex 09-50-7021 Connector Molex 08-50-0106 Pin
				AMP 87194-1 Connector AMP 2-87025-5 Connector AMP 87023-1 Pin
Parallel I/O		50 double-sided	0.1	3M 3416-000 (flat cable) or TI H312125 (round cable)
Serial I/O		7 single-sided	0.156	Molex 09-65-1021 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key
				AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key

Notes

1. Connectors and pins from a given vendor may only be used with connectors and pins from the same vendor.
2. A single 86-contact edge-on connector (CDC VPB01E43A00A1) may be used to connect the two groups of regulated voltages (i.e., +5V, +12V, −5V, and +5V, −12V).
3. Required only when RS232C line drivers and receivers are used.

Line Drivers and Terminators

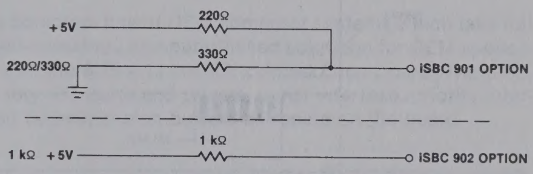
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/04:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220Ω/330Ω divider and 1 kΩ pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the iSBC 80/04:

RS232C Driver — National DS1488 or TI SN75188

RS232C Receiver — National DS1490 or TI SN75189

Sockets

Sockets may be installed in the hole patterns provided for the RS232C drivers and receivers. The following sockets are compatible with the iSBC 80/04: TI C93-14-02 and SCANBE US-2-14-160-N-B.

Compatible Voltage Regulator

National LM 323 — 3A, 5V Positive Regulator

Fairchild μA7805 KM — 1A, 5V Positive Regulator

Compatible Heat Sink

IERC — LA Series or

AAVID Engineering, Inc. — Series 5051

Physical Characteristics

Width — 7.85 in. (19.94 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 6.0 oz (169.9 gm)

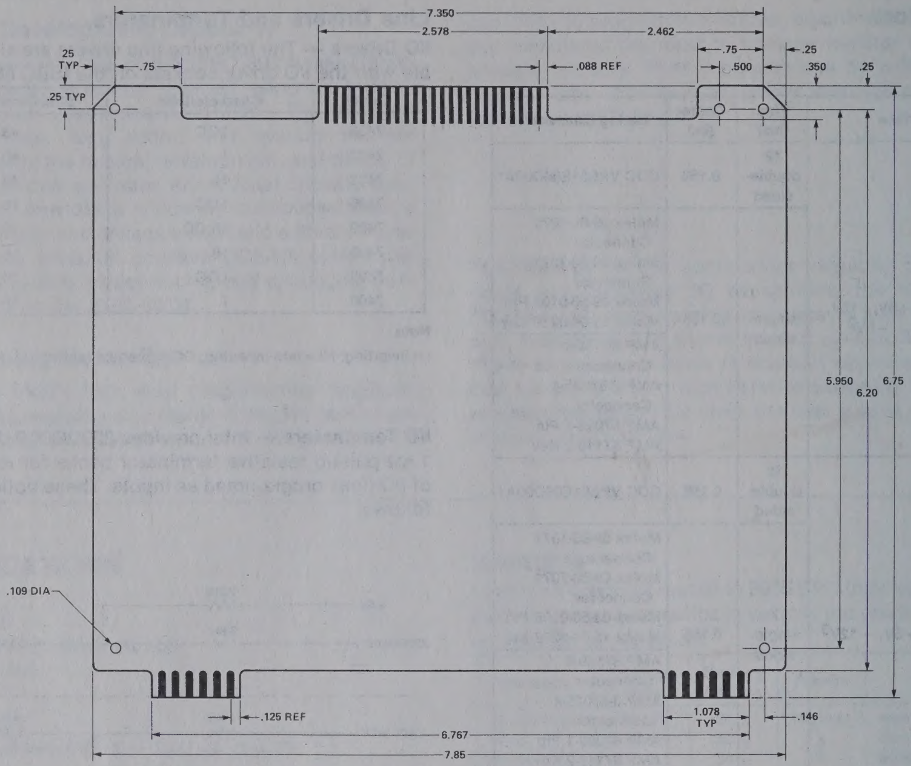


Figure 2. iSBC 80/04 Dimensions

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without PROM[1] (max)	With 2716 EPROM[2] (max)	With 2708 EPROM[3] (max)
$V_{CC} = +5V$	$I_{CC} = 600$ mA	1.45A	1.25A
$V_{DD} = +12V$ [4]	$I_{DD} = 0$	7 mA[5]	137 mA
$V_{BB} = -5V$ [4]	$I_{BB} = 0$	0	90 mA
$V_{AA} = -12V$ [5]	$I_{AA} = 0$	23 mA[5]	23 mA[5]

Notes

1. Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
2. With two Intel 2716 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
3. With two Intel 2708 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
4. Required for 2708 EPROMs.
5. Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800482-02 - iSBC 80/04 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/04	Single Board Computer

iSBC 80/05
SINGLE BOARD COMPUTER

8085A CPU used as central processor

512 bytes of static read/write memory

Sockets for 4K bytes of erasable reprogrammable or masked read only memory

22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Full MULTIBUS control logic allowing up to 16 masters to share system bus

Programmable 14-bit binary timer

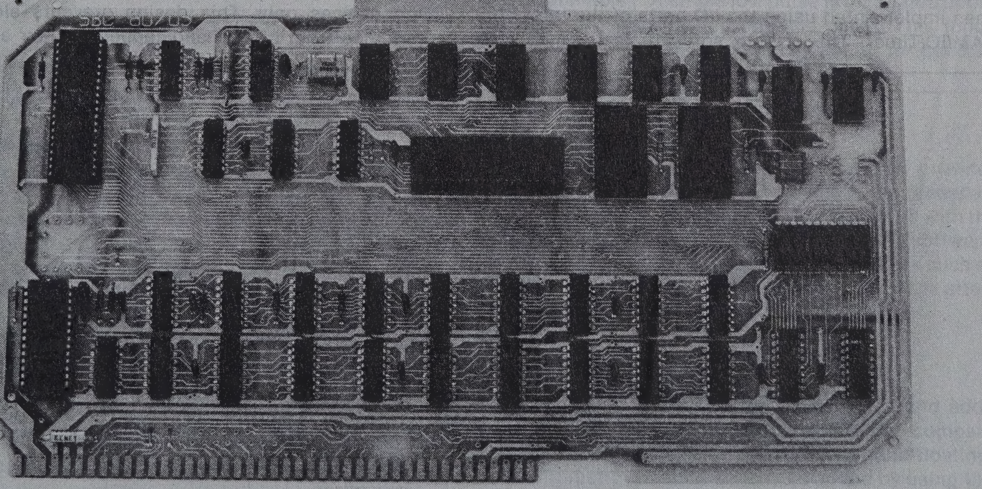
TTL serial I/O interface with sockets for RS232C line drivers and receivers

Four-level vectored interrupt

Fully compatible with optional iSBC expansion boards and peripherals

Single +5V power supply

The iSBC 80/05 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/05 is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, programmable timer, MULTIBUS control logic, and bus expansion buffers all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085 CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/05. The 8085A CPU is directly software compatible with the popular Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of iSBC 80/05 functional components is shown in Figure 1.

Memory Addressing

The 8085A CPU has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

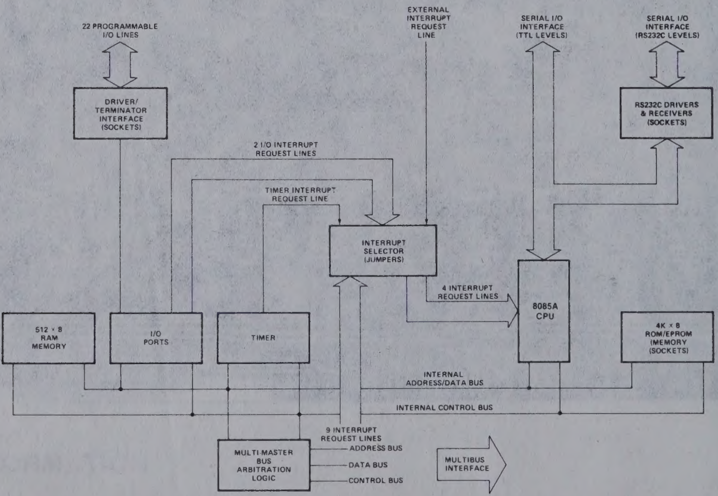
The iSBC 80/05 contains 512 bytes of read/write memory using Intel's low power static RAMs. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2316E masked ROMs. Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 2708 EPROMs or Intel 2608 masked ROMs.

Parallel I/O Interface

The iSBC 80/05 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 40-pin edge connector that mates with flat, woven, or round cable.

Multimaster Capability

The iSBC 8085A is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share systems tasks with communication over the system bus), the iSBC 80/05 provides full MULTIBUS arbitration control logic. This control logic allows up to three bus masters (i.e., any combination of iSBC 80/05, iSBC 80/20-4, DMA controller, diskette controller, etc.) to share the system bus in serial (daisy-chain) priority fashion, and up to 16 masters may share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/05 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and for transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to



22 PROGRAMMABLE I/O LINES
EXTERNAL INTERRUPT REQUEST LINE
SERIAL I/O INTERFACE (TTL LEVELS)
SERIAL I/O INTERFACE (RS232C LEVELS)
DRIVER/ TERMINATOR INTERFACE (SOCKETS)
RS232C DRIVERS & RECEIVERS (SOCKETS)
2 I/O INTERRUPT REQUEST LINES
TIMER INTERRUPT REQUEST LINE
INTERRUPT SELECTOR (JUMPERS)
4 INTERRUPT REQUEST LINES
8085A CPU
512 × 8 RAM MEMORY
I/O PORTS
TIMER
4K × 8 ROM/EPROM (MEMORY (SOCKETS)
INTERNAL ADDRESS/DATA BUS
INTERNAL CONTROL BUS
9 INTERRUPT REQUEST LINES
MULTI-MASTER BUS ARBITRATION LOGIC
ADDRESS BUS
DATA BUS
CONTROL BUS
MULTIBUS INTERFACE

Figure 1. iSBC 80/05 Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation Unidirectional				
		Input		Output		Control
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X[1]
4	3	X		X		X[2]

Notes

1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.

Table 1. Input/Output Port Modes of Operation

gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timer

The iSBC 80/05 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO/Timer. The system designer simply configures the timer via software to meet system requirements. Whenever a given time delay is needed, software commands to the programmable timer select the desired function. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Serial I/O Interface

The iSBC 80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085A CPU. These functions are controlled exculsively by software through execution of the 8085A RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the iSBC 80/05 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible and sockets are provided on the board for optional connection of RS232C line drivers and receivers.

Interrupt Capability

The iSBC 80/05 takes advantage of the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed to the four interrupt inputs of the 8085A CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 24$_{16}$, RST 7.5: 3C$_{16}$, RST 6.5: 34$_{16}$, RST 5.5: 2C$_{16}$). A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU.

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out will remain high until one-half the count has been completed, and go low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Table 2. Programmable Timer Functions

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combinations boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are avialable to support multiboard systems.

Systems Development Capability

The development cycle of iSBC 80/05-based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/05 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editior, and a library manager.

A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/05.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 2.03 μs, ±0.1%

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — 0-0FFF$_H$

RAM — 3E00$_H$

Memory Capacity

On-Board ROM/EPROM — 4K bytes (with Intel 2716) or 2K bytes (with Intel 2708)

On-Board RAM — 512 bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combination of RAM, ROM, and PROM

I/O Addressing

On-Board Programmable I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 Ports 3 & 4	8155 Port	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Note

The iSBC 80/05 may be expanded to 1102 programmable input/output lines by using optional iSBC 80 I/O boards.

Serial Communications Characteristics

SID and SOD functions of the 8085A CPU are used for serial I/O. They are controlled by software through RIM and SIM instructions of the 8085A CPU. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085A CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Interrupt Input	Memory Address	Priority	Type
TRAP	24_{16}	Highest	Non-maskable
RST 7.5	$3C_{16}$	↕	Maskable
RST 6.5	34_{16}		Maskable
RST 5.5	$2C_{16}$	Lowest	Maskable

Timer

Input Frequency Reference — 122.88 kHz ±0.1% (8.14 μs period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter Min	Timer/Counter Max
Programmable pulse	8.14 μs	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μs	133.33 ms

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Request — All TTL compatible (active-low)

Serial I/O — TTL; sockets available for RS232C line drivers and receivers

System Clock (8085A CPU)

1.966 MHz ± 0.1%

Interface	Lines (qty)	Centers (in.)	Mating Connector
Bus	50 double-sided	0.156	Viking 3KH43/9AMK12
Parallel I/O	50 double-sided	0.1	3M 3415-000 or TI H312125
Serial I/O[1]	7 single-sided	0.1	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key
			AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 878023-1 Pin AMP 87116-2 Key

Note

1. Connectors and pins from one vendor may only be used with connectors and pins from the same vendor.

Line Drivers and Terminators

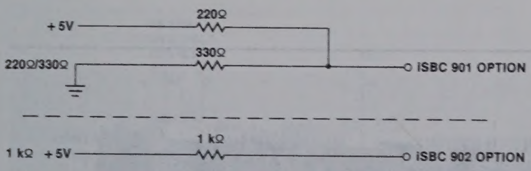
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/05:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220Ω/330Ω divider and 1 kΩ pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the iSBC 80/05:

RS232C Driver — National DS1488 or TI SN75188

RS232C Receiver — National DS1490 or TI SN75189

Physical Characteristics

Width — 12.00 in. (30.49 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12.0 oz (339.8 gm)

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without PROM[1] (max)	With 2716 EPROM[2] (max)	With 8708 EPROM[3] (max)
$V_{CC} = +5V$	$I_{CC} = 1.80$ mA	2.65A	2.45A
$V_{DD} = +12V$ [4]	$I_{DD} = 0$	7 mA[5]	137 mA
$V_{BB} = -5V$ [4]	$I_{BB} = 0$	0	90 mA
$V_{AA} = -12V$ [5]	$I_{AA} = 0$	23 mA[5]	23 mA[5]

Notes

1. Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
2. With two Intel 2716 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
3. With two Intel 2708 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
4. Required for 2708 EPROMs.
5. Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C.

Reference Manual

9800483D — iSBC 80/05 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/05	Single Board Computer

iSBC 80/10A SINGLE BOARD COMPUTER

8080A CPU used as central processor

1K bytes of read/write memory

Sockets for 8K bytes of programmable or masked read only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

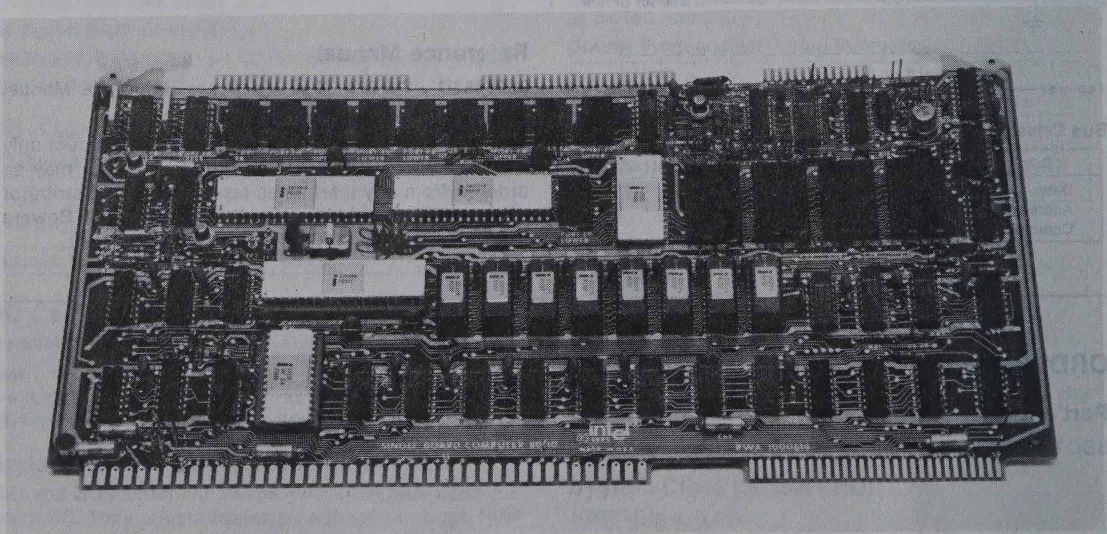
Programmable synchronous/asynchronous communications interface with selectable teletypewriter or RS232C compatibility

Six interrupt request lines

Compatible with optional memory and I/O expansion boards

Bus drivers for memory and I/O expansion

The iSBC 80/10A is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/10A is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, bus control logic, and drivers all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/10A. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. A block diagram of iSBC 80/10A functional components is shown in Figure 1.

Memory Addressing

The 8080A has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

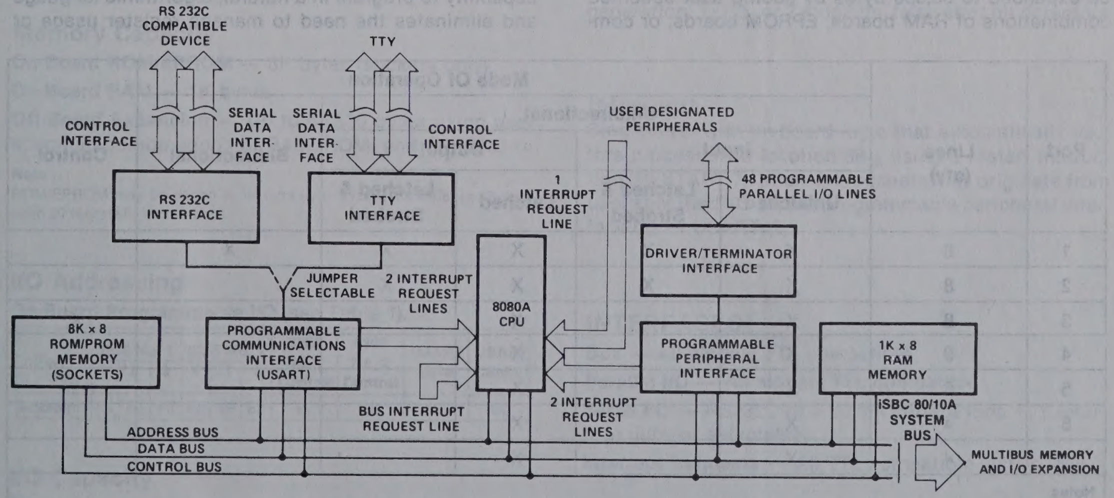
The iSBC 80/10A contains 1K bytes of read/write memory using Intel low power static RAMs. All on-board RAM read and write operations are performed at maximum processor speed. Sockets for up to 8K bytes of nonvolatile read-only-memory are provided on the board. Read-only-memory may be added in 1K byte increments using Intel 2708 or 2758 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2608 ROMs. Optionally, if more than 4K bytes are required, read only memory may be added in 2K-byte increments using Intel 2716 EPROMs or Intel 2316E masked ROMs. All on-board ROM or EPROM read operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/10A contains 48 programmable parallel I/O lines implemented using two Intel 8255A programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provide for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable or round cable.

Serial I/O Interface

A programmable communications interface using the Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper selectable TTY or


RS 232C COMPATIBLE DEVICE
TTY
CONTROL INTERFACE
SERIAL DATA INTERFACE
SERIAL DATA INTERFACE
CONTROL INTERFACE
USER DESIGNATED PERIPHERALS
RS 232C INTERFACE
TTY INTERFACE
1 INTERRUPT REQUEST LINE
48 PROGRAMMABLE PARALLEL I/O LINES
DRIVER/TERMINATOR INTERFACE
JUMPER SELECTABLE
2 INTERRUPT REQUEST LINES
8080A CPU
8K x 8 ROM/PROM MEMORY (SOCKETS)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)
PROGRAMMABLE PERIPHERAL INTERFACE
1K x 8 RAM MEMORY
BUS INTERRUPT REQUEST LINE
2 INTERRUPT REQUEST LINES
iSBC 80/10A SYSTEM BUS
ADDRESS BUS
DATA BUS
CONTROL BUS
MULTIBUS MEMORY AND I/O EXPANSION

Note

1. Interrupts originating from the programmable communications interface and programmable peripheral interface are jumper selectable.

Figure 1. iSBC 80/10A Block Diagram Showing Functional Components

RS232C compatible interfaces on the board, in conjunction with the USART, provides a direct interface to teletypes, CRTs, RS232 compatible cassettes, and asynchronous and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 25-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt Capability

Interrupt requests may originate from six sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38_{16}.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Real-Time Software

Intel's RMX/80 Real Time Multi-Tasking Executive software, specifically designed for Intel iSBC 80 single board computers, provides the capability to monitor and control multiple asynchronous external events. The RMX/80 executive, which synchronizes and controls the execution of multiple tasks, resides in 2K bytes of on-board EPROM or ROM. Optional linkable and relocatable modules for teletypewriter and CRT control, a diskette file system, a high sped math unit, and analog subsystems are also available.

System Development Capability

The development cycle of iSBC 80/10A-based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/10A system software. An optional diskette operating system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-80) option provides the capability of developing and debugging software directly on the iSBC 80/10A.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or

Port	Lines (qty)	Mode Of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X[1]
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

Notes
Port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intellec system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user flexibility in developing software.

BASIC-80 — A high level language interpreter with extended disk capabilities which operates under the RMX/80 Real-Time Multitasking Executive and translates BASIC-80 source programs into an internally executable form. This language interpreter provided as a set of linkable object modules is ideally suited to the OEM who requires a pass through programming language. The BASIC-80 programs may be created, stored and interpreted on the iSBC 80 based system. The BASIC-80 language has a rich complement of statements, functions, and commands to program applications requiring a full range of 1) string manipulation and disk I/O for data processing, 2) single and double precision floating point and array handling for numeric analysis, or 3) port I/O with mask operations controlled through bit-wise Boolean logical operators.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.95 μs

Note
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0—IFFF (using 2716 EPROMs or 2316E ROMs); 0—OFFF (using 2708 or 2758 EPROMs, or 2608 ROMs)

On-Board RAM — 3C00—3FFF

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 1K bytes

Off-Board Expansion — Up to 65,536 bytes using user specified combinations of RAM, ROM, and EPROM.

Note
ROM/EPROM may be added in 1K-byte (with 2708/2758/2608) or 2K-byte (with 2716/2316E) increments.

I/O Addressing

On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note
Expansion to 1128 programmable I/O lines can be accomplished using optional boards.

Serial Baud Rates

Freqency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
6.98	6980	—	110
4.8	4800	300	75

Serial Communication Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5—8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Single-level with on-board logic that automatically vectors processor to location 38_{16} using a restart instruction (RESTART 7). Interrupt requests may originate from user specified I/O (2), the programmable peripheral interface (2), or USART (2).

INTERFACES

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C or a 20 mil current loop TTY interface (jumper selectable)

Interrupt Requests — All TTL compatible (active-low)

System Clock

2.048 MHz ± 0.1%

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors	
Bus	86	0.156	Viking 3KH43/9AMK12	Wire-wrap
Parallel I/O (2)	50	0.1	3M 3415-000 or TI H312125	Flat Pins
Serial I/O	26	0.1	3M 3462-0001 or AMP 88106-1	Flat Flat

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (484.4 gm)

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without EPROM[1] (max)	8708 EPROM[2] (max)	With 2758 or 2716 EPROM[3] (max)
V_{CC} = +5V	I_{CC} = 2.9A	4.0A	4.4A
V_{DD} = +12V	I_{DD} = 150 mA	400 mA	150 mA
V_{BB} = −5V	I_{BB} = 2 mA	200 mA	2 mA
V_{AA} = −12V	I_{AA} = 175 mA[4]	175 mA[4]	175 mA[4]

Notes

1. Does not include power required for optional ROM/EPROM, I/O drivers, and I/O Terminators
2. With four Intel 2708 EPROMs and 220Ω/330Ω terminators installed for 48 input lines; all terminator inputs low.
3. With four Intel 2758 or four 2716 EPROMs and 220Ω/330Ω terminators installed for 48 input ports; all terminator inputs low.
4. Required for RS232C drivers only.

Line Drivers and Terminators

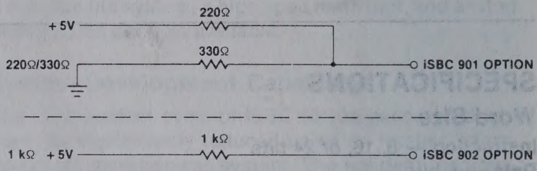
I/O Drivers — The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 80/10A:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note
I = inverting; NI = non-inverting; OC = open collector.

Port 1 has 25 nA totem pole drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pull up



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	25
Address	Tri-state	25
Commands	Tri-state	25

Environmental Characteristics

Operating Temperature — 0°C to 5°C

Equipment Supplied

iSBC 80/10A Single Board Computer
iSBC 80/10A Schematics

Reference Manual

9800230F — iSBC 80/10 and iSBC 80/10A Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/10A	Single Board Computer

iSBC 80/20-4 SINGLE BOARD COMPUTER

8080A CPU used as central processor

4K bytes of static read/write memory

Sockets for up to 8K bytes of erasable reprogrammable or masked read only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable synchronous/asynchronous RS232C compatibel serial interface with fully software selectable baud rate generation

Full MULTIBUS control logic allowing up to 16 masters to share system bus

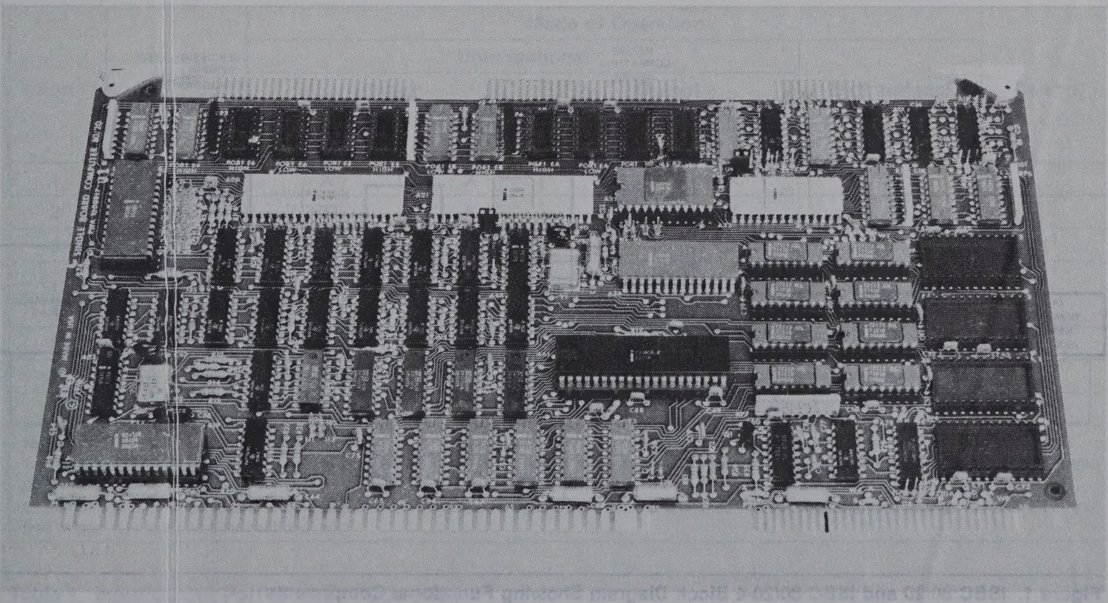
Two programmable 16-bit BCD and binary timers

Eight-level programmable interrupt control

Compatible with optionalmemory and I/O expansion boards

Auxiliary power bus, memory protect, and power-fail interrupt control logic provided for battery backup RAM requirements

The iSBC 80/20-4 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. Each iSBC 80/20-4 is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic, two programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on each board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/20-4. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum instruction execution time is 1.86 microseconds. A block diagram of iSBC 80/20-4 functional components is shown in Figure 1.

Memory Addressing

The 8080A has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/20-4 contains 4K bytes of static read/write memory using Intel low power static RAMs. All on-board RAM read and write operations are performed at maximum processor speed. Power for on-board RAM memory is provided on an auxiliary power bus, and memory protect logic is included for battery backup RAM requirements. Sockets for up to 8K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 1K-byte increments using Intel 2708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2608 ROMs, or read only memory may be added in 2K-byte increments using Intel 2716 EPROMs or Intel 2316E masked ROMs. All on-board ROM read operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/20-4 contains 48 programmable parallel I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of the unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round cable.

Serial I/O Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC

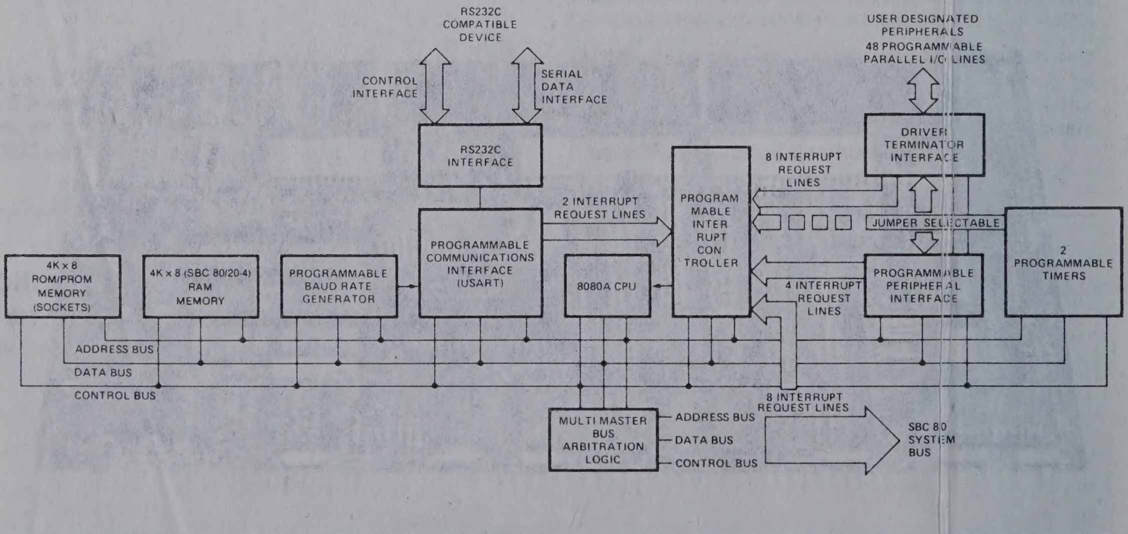

RS232C COMPATIBLE DEVICE
CONTROL INTERFACE
SERIAL DATA INTERFACE
RS232C INTERFACE
USER DESIGNATED PERIPHERALS
48 PROGRAMMABLE PARALLEL I/O LINES
DRIVER TERMINATOR INTERFACE
8 INTERRUPT REQUEST LINES
2 INTERRUPT REQUEST LINES
PROGRAMMABLE INTERRUPT CONTROLLER
JUMPER SELECTABLE
4K x 8 ROM/PROM MEMORY (SOCKETS)
4K x 8 (SBC 80/20-4) RAM MEMORY
PROGRAMMABLE BAUD RATE GENERATOR
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)
8080A CPU
4 INTERRUPT REQUEST LINES
PROGRAMMABLE PERIPHERAL INTERFACE
2 PROGRAMMABLE TIMERS
ADDRESS BUS
DATA BUS
CONTROL BUS
8 INTERRUPT REQUEST LINES
MULTI MASTER BUS ARBITRATION LOGIC
ADDRESS BUS
DATA BUS
CONTROL BUS
SBC 80 SYSTEM BUS

Figure 1. iSBC 80/20 and iSBC 80/20-4 Block Diagram Showing Functional Components

80/20-4 board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character parity, and baud rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 80/20-4 to teletypewriters or other 20 mA current loop equipment.

Multimaster Capability

The iSBC 80/20-4 is a full computer on a single board with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the iSBC 80/20-4 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/20-4 or high speed controllers to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters may share the system bus with the addition of an external priority network. Once bus control is attained, a bus bandwidth of up to 5M bytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data words per second. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/20-4 board provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or outputs from the 8255 programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X^1
	4	X		X			X^1
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X^2
	4	X		X			X^2

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

rate generator for the iSBC 80/20-4 RS232C USART serial port. In utilizing the iSBC 80/20-4, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly".

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 2. Programmable Timer Functions

Interrupt Capability

Operation and Priority Assignments — An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the interrupt register of the PIC.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Addressing — The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8080 jump instruction at each of these addressed then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation — Interrupt requests may originate from 26 sources. Four jumper selectable interrupt requets can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transfer to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and eight interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Power-Fail Control — Control logic is also included for generation of a power-fail interrupt which works in conjunction with the AC-low signal from iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Real-Time Software

The iSBC 80/20-4 is totally compatible with Intel's RMX/80 Real-Time Multi-Tasking Executive. iSBC 80/20-4 based user programs (tasks) can take advantage of the RMX/80 executive to do all necessary scheduling, intertask ccommunication, and memory space allocation. RMX/80 also provides standard I/O support software such as disk file handling, Intel analog board handling, and terminal handling.

System Development Capability

The development cycle of iSBC 80/20-4 based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/20-4 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-80) option provides the capability of developing and debugging software directly on the iSBC 80/20-4 single board computer.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly langauge programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intellec system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

BASIC-80 — A high level language interpreter with extended disk capabilities which operates under the RMX/80 Real-Time Multi-Tasking Executive and translates BASIC-80 source programs into an internally executable form. This language interpreter, provided as a set of linkable object modules, is ideally suited to the OEM who requires a pass through programming language. The BASIC-80 programs may be created, stored and interpreted on the iSBC 80 based system. The BASIC-80 language has a rich complement of statements, functions, and commands to program applications requiring a full range of 1) string manipulation and disk I/O for data processing, 2) single and double precision floating point and array handling for numeric analysis, or 3) port I/O with mask operations controlled through bit-wise Boolean logical operators.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.86 μs

Note
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-0FFF (2708) or 0–1FFF (2716)

On-Board RAM — 4K bytes ending on a 16K boundary (e.g., $3FFF_H$, $7FFF_H$, $BFFF_H$, . . . $FFFF_H$)

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 4K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified RAM, ROM, and EPROM

Note
ROM/EPROM may be added in 1K or 2K-byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1)

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note
Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

Serial Communications Characteristics

Synchronous — 5–8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Note
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

Note
Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE$_H$).

Interrupts

Register Addresses (hex notation, I/O address space)

DA Interrupt request register
DA In-service register
DB Mask register
DA Command register
DB Block address register
DA Status (polling register)

Note
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Timers

Register Addresses (hex notation, I/O address space)

DF Control register
DC Timer 1
DD Timer 2

Note
Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference	Event Rate
1.0752 MHz ± 10% (0.930 μs period, nominal)	1.1 MHz max

Note
Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Programmable one-shot	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-wave rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.31 kHz
Software triggered strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Hardware triggered strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hr

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Interrupt Requests — All TTL compatible
Timer — All signals TTL compatible
Serial I/O — RS232C compatible, data set configuration

System Clock (8080A CPU)

2.1504 MHz ±0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

Line Drivers and Terminators

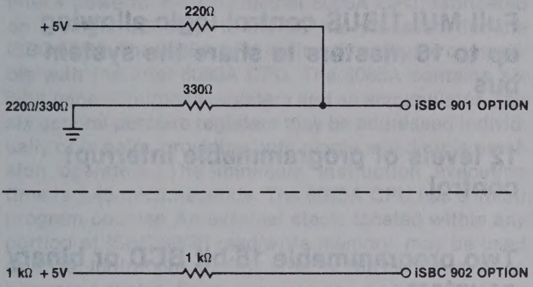
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/20-4.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note
I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pull-up



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.26 cm)
Weight — 14 oz (397.6 gm)

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without PROM[1] (max)	With 4K PROM[2] (max)	With iSBC 530[3] (max)	RAM Only[4] (max)	With 8K PROM[5] (max)
V_{CC} = +5V	I_{CC} = 4.0A	4.9A	4.9A	1.1A	5.2A
V_{DD} = +12V	I_{DD} = 90 mA	350 mA	450 mA	—	90 mA
V_{BB} = −5V	I_{BB} = 2 mA	180 mA	180 mA	—	2 mA
V_{AA} = −12V	I_{AA} = 20 mA	20 mA	120 mA	—	20 mA

Notes

1. Does not include power required for optional PROM, I/O drivers, and I/O terminators.
2. With four 2708 EPROMs and 220Ω/330Ω input terminators installed for 32 I/O lines, all terminator inputs low.
3. With four 2708 EPROMs, 220Ω/330Ω input terminators installed for 32 I/O lines, all terminator inputs low, and iSBC 530 Teletypewriter Adapter drawing power from serial port connector.
4. RAM chips powered via auxiliary power bus.
5. With four 8716 EPROMs and eight 220Ω/330Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°CC

Reference Manual

9800317D — iSBC 80/20-5 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/20-4	Single Board Computer with 4K bytes RAM

intel®

iSBC 80/30
SINGLE BOARD COMPUTER

8085A CPU used as central processing unit

16K bytes of dual port dynamic read/write memory with on-board refresh

Sockets for up to 8K bytes of read only memory

Sockets for 8041A/8741A Universal Peripheral Interface and interchangeable line drivers and line terminators

24 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable synchronous/asynchronous RS232C compatible serial interface with fully software selectable baud rate generation

Full MULTIBUS control logic allowing up to 16 masters to share the system bus

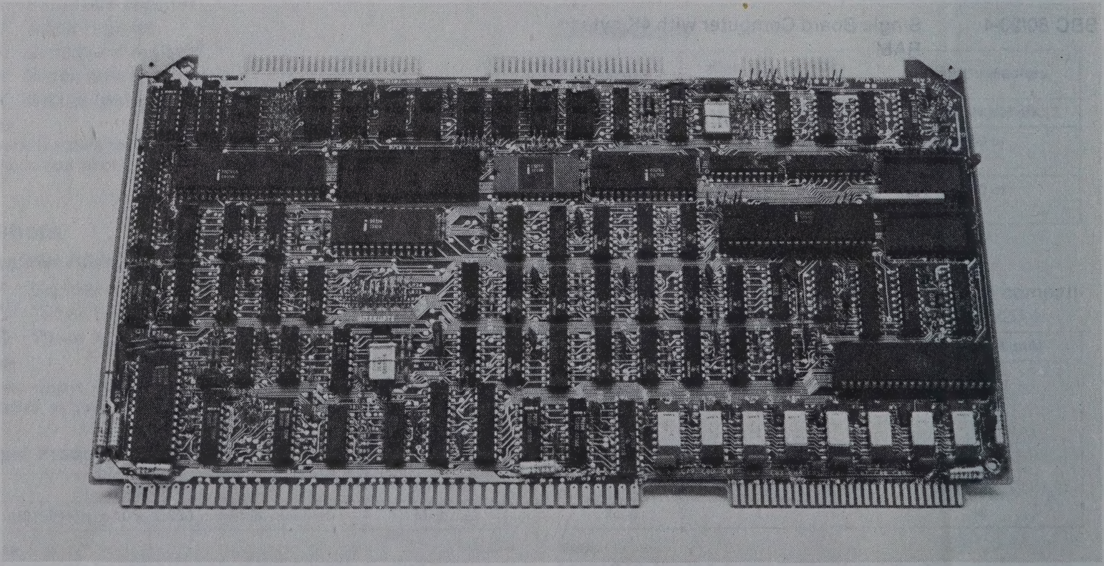
12 levels of programmable interrupt control

Two programmable 16-bit BCD or binary counters

Auxiliary power bus, memory protect, and power-fail interrupt control logic for RAM battery backup

Compatible with optional iSBC 80 CPU, memory, and I/O expansion boards

The iSBC 80/30 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical self-contained computer-based solutions for OEM applications. The iSBC 80/30 is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, universal peripheral interface capability, I/O ports and drivers, serial communications interface, priority interrupt logic, programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on the board.



FUNCTIONAL DESCRIPTION

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/30. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of iSBC 80/30 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Bus Structure

The iSBC 80/30 has an internal bus for all on-board memory and I/O operations and a system bus (i.e., the MULTIBUS) for all external memory and I/O operations. Hence, local (on-board) operations do not tie up the system bus, and allow true parallel processing when several bus masters (i.e., DMA devices, other single board computers) are used in a multimaster scheme. A block diagram of the iSBC 80/30 functional components is shown in Figure 1.

RAM Capacity

The iSBC 80/30 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 80/30 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the iSBC 80/30 or from any other bus master interfaced via the

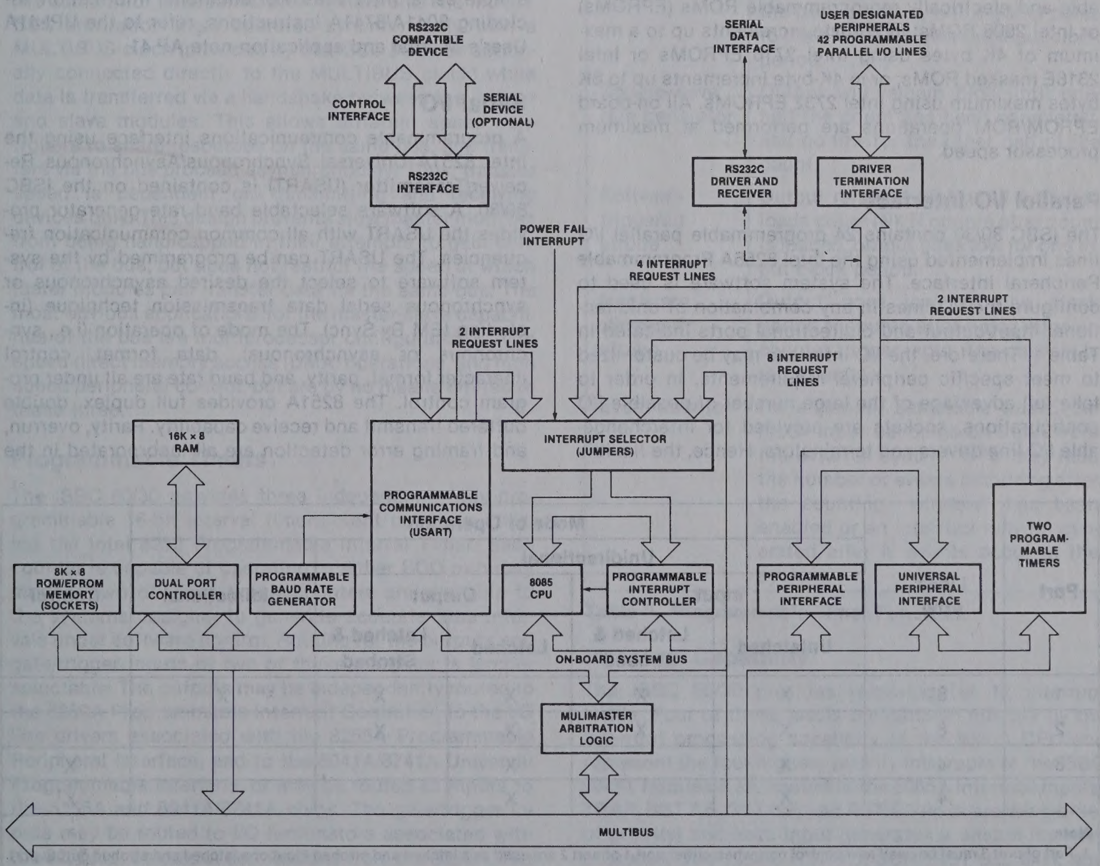

RS232C COMPATIBLE DEVICE
CONTROL INTERFACE
SERIAL DEVICE (OPTIONAL)
RS232C INTERFACE
SERIAL DATA INTERFACE
USER DESIGNATED PERIPHERALS 42 PROGRAMMABLE PARALLEL I/O LINES
RS232C DRIVER AND RECEIVER
DRIVER TERMINATION INTERFACE
POWER FAIL INTERRUPT
4 INTERRUPT REQUEST LINES
2 INTERRUPT REQUEST LINES
2 INTERRUPT REQUEST LINES
8 INTERRUPT REQUEST LINES
16K × 8 RAM
INTERRUPT SELECTOR (JUMPERS)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)
TWO PROGRAMMABLE TIMERS
8K × 8 ROM/EPROM MEMORY (SOCKETS)
DUAL PORT CONTROLLER
PROGRAMMABLE BAUD RATE GENERATOR
8085 CPU
PROGRAMMABLE INTERRUPT CONTROLLER
PROGRAMMABLE PERIPHERAL INTERFACE
UNIVERSAL PERIPHERAL INTERFACE
ON-BOARD SYSTEM BUS
MULIMASTER ARBITRATION LOGIC
MULTIBUS

Figure 1. iSBC 80/30 Single Board Computer Block Diagram

MULTIBUS. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for any other concurrent operations (e.g., DMA data transfers) requiring the use of the MULTIBUS. Dynamic RAM refresh is accomplished automatically by the iSBC 80/30 for accesses originating from either the CPU or via the MULTIBUS. Memory space assignment can be selected independently for on-board and MULTIBUS RAM accesses. The on-board RAM, as seen by the 8085A CPU, may be placed anywhere within the 0- to 64K-address space. The iSBC 80/30 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to reserve 8K- and 16K-byte segments of on-board RAM for use by the 8085A CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory are provided on the iSBC 80/30 board. Read only memory may be added in 1K-byte increments up to a maximum of 2K bytes using Intel 2708 or 2758 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2608 ROMs; in 2K-byte increments up to a maximum of 4K bytes using Intel 2716 EPROMs or Intel 2316E masked ROMs; or in 4K-byte increments up to 8K bytes maximum using Intel 2732 EPROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/30 contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Universal Peripheral Interface (UPI)

The iSBC 80/30 provides sockets for a user supplied Intel 8041A/8741A Universal Peripheral Interface (UPI) chip and the associated line drivers and terminators for the UPI's I/O ports. The 8041A/8741A is a single chip microcomputer containing a CPU, 1K bytes of ROM (8041A) or EPROM (8741A), 64 bytes of RAM, 18 programmable I/O lines, and an 8-bit timer. Special interface registers included in the chip allow the 8041A to function as a slave processor to the iSBC 80/30's 8085A CPU. The UPI allows the user to specify algorithms for controlling user peripherals directly in the chip, thereby relieving the 8085A for other system functions. The iSBC 80/30 provides an RS232C driver and an RS232C receiver for optional connection to the 8041A/8741A in applications where the UPI is programmed to handle simple serial interfaces. For additional information, including 8041A/8741A instructions, refer to the UPI-41A User's Manual and application note AP-41.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 80/30. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM By-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X^1
	4	X		X			X^1

Note
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 80/30 to teletypewriters or other 20 mA current loop equipment.

Multimaster Capability

The iSBC 80/30 is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 80/30 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/30's or other bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/30 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/30 provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, and to the 8041A/8741A Universal Programmable Interface, or may be routed as inputs to the 8255A and 8041A/8741A chips. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 80/30 RS232C USART serial port. In utilizing the iSBC 80/30, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 2. Programmable Timer Functions

Interrupt Capability

The iSBC 80/30 provides vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A CPU and represent the four highest priority interrupts of the iSBC 80/30. Requests are routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority) and each input generates a unique memory address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A jump instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Request Generation — Interrupt requests may originate from 18 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers and by the universal peripheral interface, eight additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and two interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating point arithmetic capabilities may be added by using the iSBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Real-Time Software

Intel's RMX/80 Real-Time Multi-Tasking Executive software, specifically designed for Intel iSBC 80 single board computers, provides the capability to monitor and control multiple asynchronous external events. The RMX/80 executive, which synchronizes and controls the execution of multiple tasks, is provided as a linkable and relocatable module requiring only 2K bytes of memory space. Optional linkable and relocatable modules for teletypewriter and CRT control, diskette file system, high speed math unit, and analog subsystems are also available.

System Development Capability

The development cycle of iSBC 80/30-based products may be significantly reduced using the Intellec series microcomputer development systems. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/30 system software. An optional diskette operating system provides a relocating macroassembler, relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/30.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the intellec system. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 subset language specification. The FORTRAN-80 compiler produces relocatable object code that may be easily linked with other FORTRAN-80, PL/M, or assembly language program modules. This gives the user wide flexibility in developing software by using the best software tool for a particular functional module within the user's application.

BASIC-80 — A high level language interpreter with extended disk capabilities which operates under the RMX/80 Real-Time Multitasking Executive and translates BASIC-80 source programs into an internally executable form. This language interpreter provided as a set of linkable object modules is ideally suited to the OEM who requires a pass thru programming language. The Basic-80 programs may be created, stored and interpreted on the iSBC 80 based system. The BASIC-80 language has a rich complement of statements, functions, and commands to program applications requiring a full range of 1) string manipulation and disk I/O for data processing, 2) single and double precision floating point and array handling for numeric analysis, or 3) port I/O with mask operations controlled through bit-wise Boolean logical operators.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.45 μs

Note
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-07FF (using 2708 or 2758 EPROMs or 2608 ROMs); 0-0FFF (using 2716 EPROMs or 2316E ROMs); 0-1FFF (using 2732 ROMs)

On-Board RAM — 16K bytes of dual port RAM starting on a 16K boundary. One or two 8K-byte segments may be reserved for CPU use only.

Memory Capacity

On-Board Read Only Memory — 8K bytes (sockets only)

On-Board RAM — 16K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM

Note
Read only memory may be added in 1K, 2K, or 4K-byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1)

Port	8255A				8041A/8741A		USART	
	1	2	3	Control	Data	Control	Data	Control
Address	E8	E9	EA	EB	E4 or E6	E5 or E7	EC	ED

I/O Capacity

Parallel — 42 programmable lines using one 8255A (24 I/O lines) and an optional 8041A/8741A (18 I/O lines)
Serial — 2 programmable lines using one 8251A and an optional 8041A/8741A programmed for serial operation

Note:
For additional information on the 8041A/8741A refer to the UPI-41 User's Manual (Publication 9800504).

Serial Communications Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5—8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Note
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Interrupts

Addresses for 8259A Registers (Hex notation, I/O address space)

DA	Interrupt request register
DA	In-service register
DB	Mask register
DA	Command register
DB	Block address register
DA	Status (polling register)

Note
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels routed to 8085A CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C	↕	Maskable
RST 6.5	34		Maskable
RST 5.5	2C	Lowest	Maskable

Timers

Register Addresses (Hex notation, I/O address space)

DF Control register
DC Timer 0
DD Timer 1
DE Timer 2

Note
Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 μs period, nominal); 1.23 MHz±0.1%(0.81 μs period, nominal); or 153.60 kHz ±0.1%(6.51 μs period nominal).

Note
Above frequencies are user selectable

Event Rate: 2.46 MHz max

Note
Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.63 μs	427.1 ms	3.26 μs	466.50 min
Programmable one-shot	1.63 μs	427.1 ms	3.26 μs	466.50 min
Rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-wave rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software triggered strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min
Hardware triggered strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min

Interfaces

MULTIBUS — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Interrupt Requests — All TTL compatible
Timer — All signals TTL compatible
Serial I/O — RS232C compatible, data set configuration

System Clock (8085A CPU)

2.76 MHz ±0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

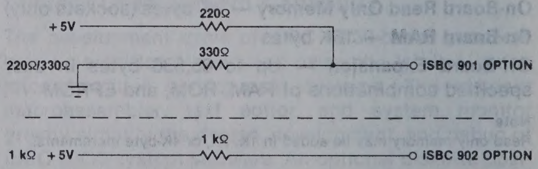
I/O Drivers— The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/30.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 18 oz. (509.6 gm)

Electrical Characteristics

DC Power Requirements

Configuration	Current Requirements			
	V_{CC} = +5V ± 5%(max)	V_{DD} = +12V ± 5%(max)	V_{BB} = −5V ± 5%(max)	V_{AA} = −12V ± 5%(max)
Without EPROM[1]	I_{CC} = 3.5A	I_{DD} = 220 mA	I_{BB} = —	I_{AA} = 50 mA
With 8041/8741[2]	3.6A	220 mA	—	50 mA
RAM only[3]	350 mA	20 mA	2.5 mA	—
With iSBC 530[4]	3.5A	320 mA	—	150 mA
With 2K EPROM[5] (using 8708)	4.4A	350 mA	95 mA	40 mA
With 2K EPROM[5] (using 2758)	4.6A	220 mA	—	50 mA
With 4K EPROM[5] (using 2716)	4.6A	220 mA	—	50 mA
With 8K EPROM[5] (using 2332)	4.6A	220 mA	—	50 mA

Notes

1. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators.
2. Does not include power required for optional EPROM/ROM, I/O drivers and I/O terminators.
3. RAM chips powered via auxiliary power bus
4. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators. Power for iSBC 530 is supplied through the serial port connector.
5. Includes power required for two EPROM/ROM chips, 8041A/8741A and 220Ω/330Ω input terminators installed for 34 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manual

9800611B — iSBC 80/30 Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/30	Single Board Computer with 16K bytes RAM

iSBC 86/12A
SINGLE BOARD COMPUTER

8086 16 bit HMOS microprocessor central processor unit

32K-bytes of dual-port read/write memory expandable on-board to 64K-bytes with on-board refresh

Sockets for up to 16K-bytes of read only memory expandable on-board to 32K-bytes

System memory expandable to 1 megabyte

24 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable synchronous/ asynchronous RS232C compatible serial interface with software selectable baud rates

Two programmable 16-bit BCD or binary timers/event counters

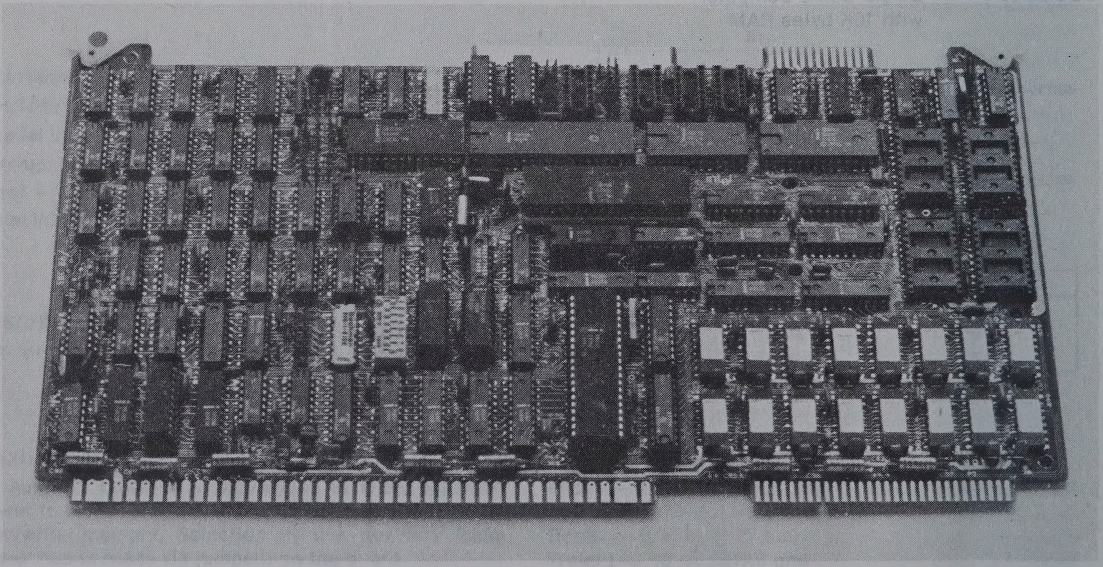
9 levels of vectored interrupt control, expandable to 65 levels

Auxiliary power bus and power fail interrupt control logic for read/write memory battery backup

MULTIBUS interface for multimaster configurations and system expansion

Compatible with iSBC 80 family single board computers, memory, digital and analog I/O, and peripheral controller boards

The iSBC 86/12A Single Board Computer is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's LSI technology to provide economical self-contained computer based solutions for OEM applications. The iSBC 86/12A board is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. Full MULTIBUS interface logic is included to offer compatibility with the Intel OEM Microcomputer Systems family of Single Board Computers, expansion memory options, digital and analog I/O expansion boards and peripheral controllers.



FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 86/12A board is Intel's 8086, a powerful 16-bit HMOS device. The 225 sq. mil chip contains 29,000 transistors and has a clock rate of 5MHz. The architecture includes four (4) 16-bit byte addressable data registers, two (2) 16-bit memory base pointer registers and two (2) 16-bit index registers, all accessed by a total of 24 operand addressing modes for complex data handling and very flexible memory addressing.

Instruction Set — The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. The instruction set of the 8086 is a superset of the 8080A/8085A family and with available software tools, programs written for the 8080A/8085A can be easily converted and run on the 8086 processor.

Architectural Features — A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 1.2μsec minimum instruction cycle to 400 nsec for queued instructions. The stack oriented architecture facilitates nested subroutines and co-routines, reentrant code and powerful interrupt handling. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K-bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

Bus Structure

The iSBC 86/12A microcomputer has three buses: an internal bus for communicating with on-board memory and I/O options, the MULTIBUS system bus for referencing additional memory and I/O options, and the dual-port bus which allows access to RAM from the on-board CPU and the MULTIBUS system bus. Local (on-board) accesses do not require MULTIBUS communication, making the system bus available for use by other MULTIBUS masters (i.e. DMA devices and other single board computers transferring to additional system memory). This feature allows true parallel processing in a multiprocessor environment. In addition, the MULTIBUS interface can be used for system expansion through the use of other 8- and 16-bit iSBC computers, memory and I/O expansion boards.

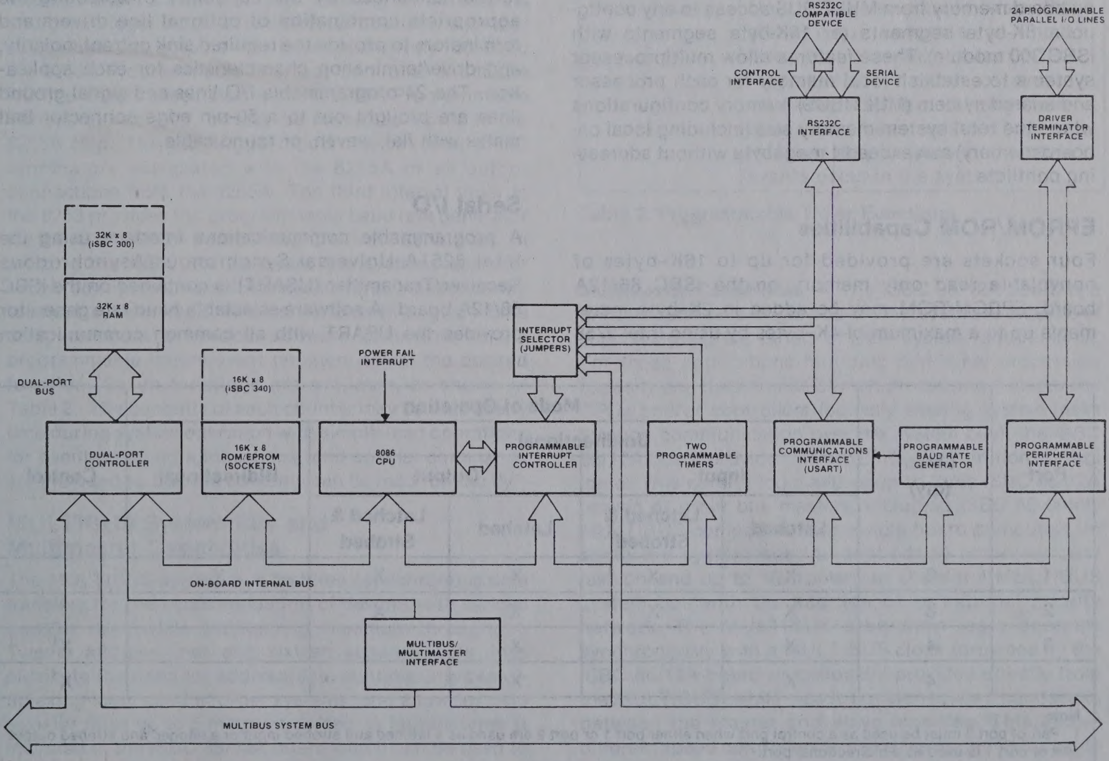

RS232C COMPATIBLE DEVICE
24 PROGRAMMABLE PARALLEL I/O LINES
CONTROL INTERFACE
SERIAL DEVICE
RS232C INTERFACE
DRIVER TERMINATOR INTERFACE
32K x 8 (iSBC 300)
32K x 8 RAM
INTERRUPT SELECTOR (JUMPERS)
POWER FAIL INTERRUPT
DUAL-PORT BUS
16K x 8 (iSBC 340)
DUAL-PORT CONTROLLER
16K x 8 ROM/EPROM (SOCKETS)
8086 CPU
PROGRAMMABLE INTERRUPT CONTROLLER
TWO PROGRAMMABLE TIMERS
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)
PROGRAMMABLE BAUD RATE GENERATOR
PROGRAMMABLE PERIPHERAL INTERFACE
ON-BOARD INTERNAL BUS
MULTIBUS/ MULTIMASTER INTERFACE
MULTIBUS SYSTEM BUS

Figure 1. iSBC 86/12A Single Board Computer Block Diagram

RAM Capabilities

The iSBC 86/12A microcomputer contains 32K bytes of dynamic read/write memory using 16K-bit 2117 RAMs. In addition, the on-board RAM complement may be expanded to 64K bytes with the iSBC 300 32K-byte RAM expansion module. Power for the on-board RAM and refresh circuitry may be optionally provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 86/12A board contains a dual port controller which allows access to the on-board RAM (32K bytes or 64K bytes when the iSBC 300 module is included with the iSBC 86/12A board) from the iSBC 86/12A CPU and from any other MULTIBUS master via the system bus. The dual port controller allows 8- and 16-bit accesses from the MULTIBUS system bus, and the on-board CPU transfers data to RAM over a 16-bit data path. Priorities have been established such that memory refresh is guaranteed by the on-board refresh logic and that the on-board CPU has priority over MULTIBUS system bus requests for access to RAM. The dual port controller includes independent addressing logic for RAM access from the on-board CPU and from the MULTIBUS system bus. The on-board CPU will always access RAM starting at location 00000_H. Address jumpers allow on-board RAM to be located starting on any 8K-byte boundary within a 1 megabyte address range for accesses from the MULTIBUS system bus. In conjunction with this feature, the iSBC 86/12A microcomputer has the ability to protect on-board memory from MULTIBUS access to any contiguous 8K-byte segments (or 16K-byte segments with iSBC 300 module). These features allow multiprocessor systems to establish local memory for each processor and shared system (MULTIBUS) memory configurations where the total system memory size (including local on-board memory) can exceed 1 megabyte without addressing conflicts.

EPROM/ROM Capabilities

Four sockets are provided for up to 16K-bytes of nonvolatile read only memory on the iSBC 86/12A board. EPROM/ROM may be added in 2K-byte increments up to a maximum of 4K-bytes by using Intel 2758 electrically programmable ROMs (EPROMs); in 4K-byte increments up to 8K bytes by using Intel 2716 EPROMs or Intel 2316E masked ROMs; or in 8K-byte increments up to 16K bytes by using Intel 2732 EPROMs or 2332A ROMs. On-board EPROM/ROM is accessed via 16-bit data paths. On-board EPROM/ROM capacity may be expanded to 32K bytes with the addition of the iSBC 340 16K-byte EPROM expansion module. It provides an additional four sockets for Intel 2732 EPROMs or Intel 2332A ROMs. With user modification of the iSBC 86/12A's on-board memory and MULTIBUS address decode, Intel 2758 and 2716 EPROMs or 2316E ROMs may be optionally supported. System memory size is easily expanded by the addition of MULTIBUS system bus compatible memory boards available in the iSBC product family.

Parallel I/O Interface

The iSBC 86/12A single board computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/12A board. A software selectable baud rate generator provides the USART with all common communication

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

Note
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26 pin edge connector that mates with RS232C compatible flat or round cable. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 unit may be used to interface the iSBC 86/12A board to teletypewriters or other 20 mA current loop equipment.

Programmable Timers

The iSBC 86/12A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A chip. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 86/12A board RS232C USART serial port. In utilizing the iSBC 86/12A board the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents can be read "on the fly".

MULTIBUS System Bus and Multimaster Capabilities

The MULTIBUS system bus features asynchronous data transfers for the accommodation of devices with various transfer rates while maintaining maximum throughput. Twenty address lines and sixteen separate data lines eliminate the need for address/data multiplexing/demultiplexing logic used in other systems, and allow for data transfer rates up to 5 megawords/sec. A failsafe timer is included in the iSBC 86/12A board which can be used to generate an interrupt if an addressed device does not respond within 6 msec.

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 2. Programmable Timer Functions

Multimaster Capabilities — The iSBC 86/12A board is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 86/12A board provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 86/12A boards or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers, to share the system bus in serial (daisy chain) priority fashion and up to 16 masters to share the MULTIBUS system bus with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 86/12A board or optionally provided directly from the MULTIBUS) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed peripheral control, but are by no means limited to these three.

Interrupt Capablity

The iSBC 86/12A board provides 9 vectored interrupt levels. The highest level is the NMI (Non-maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt cannot be inhibited by software and is typically used for signalling catastrophic events (i.e., power failure). On servicing this interrupt, program control will be implicitly transferred through location 00008_H. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at 4 byte intervals. This 32-byte block may begin at any 32-byte boundary in the lowest 1K-bytes of memory,* and contains unique instruction pointers and code segment offset values (for expanded memory operation) for each interrupt level. After acknowledging an interrupt and obtaining a device identifier byte from the 8259A PIC, the CPU will store its status flags on the stack and execute an indirect CALL instruction through the vector location (derived from the device identifier) to the interrupt service routine. In systems requiring additional interrupt levels, slave 8259A PIC's may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Request Generation — Interrupt requests may originate from 17 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full, or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. An additional interrupt request line may be jumpered directly from the parallel I/O driver terminator section. Eight prioritized interrupt request lines allow the iSBC 86/12A board to recognize and service interrupts originating from peripheral boards interfaced via the MULTIBUS system bus. The MULTIBUS fail safe timer also can be selected as an interrupt source.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 and iSBC 640 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

Note: Certain system restrictions may be incurred by the inclusion of some of the iSBC 80 family options in an iSBC 86/12A system. Consult the Intel OEM Microcomputer System Configuration Guide for specific data.

***Note:** The first 32 vector locations are reserved by Intel for dedicated vectors. Users who wish to maintain compatibility with present and future Intel products should not use these locations for user-defined vector addresses.

System Development Capabilities

The development cycle of iSBC 86/12A products can be significantly reduced by using the Intellec® series microcomputer development systems. The Assembler, Locating Linker, Library Manager, Text Editor and system monitor are all supported by the ISIS-II disk based operating system. A minimum of 64K-bytes of RAM is needed in the Intellec system to support program development for the iSBC 86/12A board. To facilitate conversion of 8080A/8085A assembly language programs to un on the iSBC 86/12A board CONV-86 is available under the ISIS-II operating system.

In-Circuit Emulator — ICE-86 in-circuit emulator provides the necessary link between the software development environment provided by the Intellec system and the "target" iSBC 86/12A execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 86/12A board, ICE-86 in-circuit emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software. ICE-86 in-circuit emulator maximizes the use of available development resources by allowing Intellec resident resources (e.g., memory and peripherals) to be accessed by software running on the target iSBC 86/12A system. In addition, software can be executed without an iSBC 86/12A execution vehicle, in 2K bytes of RAM resident in the ICE-86 system itself. Symbolic references to instruction and data locations can be made through ICE-86 in-circuit emulator to allow the user to reference memory locations with assigned names.

PL/M-86 — Intel's high level programming language, PL/M-86, is also available as an Intellec Microcomputer Development System option. PL/M-86 provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M-86 programs can be written in a much shorter time than assembly language programs for a given application. PL/M-86 includes byte and word, integer, pointer and floating point (32-bit) data types and also includes conditional compilation and macro features.

SPECIFICATIONS

Word Size

Instruction — 8, 16, 24, or 32 bits
Data — 8, 16 bits

Cycle Time

Basic Instruction Cycle — 1.2 μsec
— 400 nsec (assumes instruction in the queue)

Note:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles)

Memory Capacity

On-Board Read Only Memory — 16K bytes (sockets only); expandable to 32K bytes with iSBC 340 EPROM/ROM expansion module.

On-Board RAM — 32K bytes; expandable to 64K bytes with iSBC 300 RAM expansion module.

Off-Board Expansion — Up to 1 megabyte in user specified combinations of RAM, ROM, and EPROM.

Note:
Read only memory may be added in 2K, 4K, or 8K-byte increments.

Memory Addressing

On-Board EPROM/ROM — FF000-FFFFF$_H$ (using 2758 EPROMs); FE000-FFFFF$_H$ (using 2716 EPROMs or 2316 ROMs); FC000-FFFFF$_H$ (using 2732 EPROMs or 2332A ROMs); F8000-FFFFF$_H$ (with iSBC 340 EPROM option and four additional 2732 EPROMs).

On-Board RAM — 32K bytes of dual port RAM. Optionally expandable to 64K bytes with iSBC 300 RAM option.

CPU Access — 32K bytes: 00000-07FFF$_H$; 64K bytes: 00000-0FFFF$_H$.

MULTIBUS Access — Jumper selectable for any 8K-byte boundary, but not crossing a 128K-byte boundary. Access for 8K, 16K, 24K or 32K (16K, 32K, 48K, 64K with iSBC 300 option) bytes may be selected for on-board CPU use only.

I/O Capacity

Parallel — 24 programmable lines using one 8255A.
Serial — 1 programmable line using one 8251A.

I/O Addressing

On-Board Programmable I/O

Port	8255A				USART	
	1	2	3	Control	Data	Control
Address	C8	CA	CC	CE	D8 or DC	DA or DE

Serial Communications Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5—8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Note:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Interrupts

Addresses for 8259A Registers (Hex notation I/O address space)

C0 or C4 Write: Initialization Command Word 1 (ICW1) and Operation Control Words 2 and 3 (OCW2 and OCW3)
Read: Status and Poll Registers

C2 or C6 Write: ICW2, ICW3, ICW4, OCW1 (Mask Register)
Read: OCW1 (Mask Register)

Note:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels — 8086 CPU includes a non-maskable Interrupt (NMI) and a maskable interrupt (INTR). NMI interrupt is provided for catastrophic events such as power failure. NMI vector address is 00008. INTR interrupt is driven by on-board 8259A PIC, which provides 8-bit identifier of interrupting device to CPU. CPU multiplies identifier by four to derive vector address. Jumpers select interrupts from 17 sources without necessity of external hardware. PIC may be programmed to accommodate edge-sensitive or level-sensitive inputs.

Timers

Register Addresses (Hex notation, I/O address space)

D0	Timer 0
D2	Timer 1
D4	Timer 2
D6	Control register

Note:
Timer counts are loaded as two sequential output operations to same address as given.

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 µs period, nominal); 1.23 MHz ±0.1% (0.81 µs period, nominal); or 153.60 kHz ±0.1% (6.51 µs period nominal).

Note:
Above frequencies are user selectable.

Event Rate: 2.46 MHz max

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.63 µs	427.1 ms	3.26 s	466.50 min
Programmable one-shot	1.63 µs	427.1 ms	3.26 s	466.50 min
Rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-wave rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software triggered strobe	1.63 µs	427.1 ms	3.26 s	466.50 min
Hardware triggered strobe	1.63 µs	427.1 ms	3.26 s	466.50 min
Event counter	—	2.46 MHz	—	—

Interfaces

MULTIBUS — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Interrupt Requests — All TTL compatible
Timer — All signals TTL compatible
Serial I/O — RS232C compatible, data set configuration

System Clock (8086 CPU)

5.00 MHz ± 0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	VIKING 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000
Serial I/O	26	0.1	3M 3462-000

Memory Protect

An active low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power down sequences.

Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/12A board.

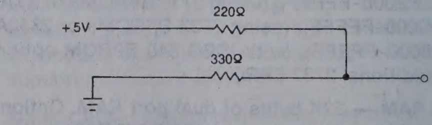
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note:
I = inverting; NI = non-inverting; OC = open collector.

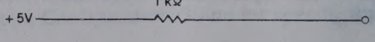
Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup

220Ω/330Ω (iSBC 901 OPTION)



1 K Ω (iSBC 902 OPTION)



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.70 in. (1.78 cm)
Weight — 19 oz. (539 gm)

Electrical Characteristics

DC Power Requirements

Configuration	Current Requirements			
	$V_{CC} = +5V$ ± 5% (max)	$V_{DD} = +12V$ ± 5% (max)	$V_{BB} = -5V$ ± 5% (max)	$V_{AA} = -12V$ ± 5% (max)
Without EPROM[1]	5.2A	350 mA	—	40 mA
RAM Only[3]	390 mA	40 mA	1.0 mA	—
With iSBC 530[4]	5.2A	450 mA	—	140 mA
With 4K EPROM[5] (using 2758)	5.5A	350 mA	—	40 mA
With 8K ROM[5] (using 2316E)	6.1A	350 mA	—	40 mA
With 8K EPROM[5] (using 2716)	5.5A	350 mA	—	40 mA
With 16K ROM[5] (using 2732 or 2332A)	5.4A	350 mA	—	40 mA

Notes:

1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. Does not include power required for optional ROM/EPROM, I/O drivers and I/O terminators.
3. RAM chips powered via auxiliary power bus.
4. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators. Power for iSBC 530 is supplied via serial port connector.
5. Includes power required for four ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°C
Relative Humidity — to 90% (without condensation)

Reference Manual

9803074-01 — iSBC 896/12A Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 86/12A	Single Board Computer with 32K bytes RAM

iSBC 310
HIGH SPEED MATHEMATICS UNIT

Provides iSBC 80 high speed mathematical functions

Performs functions independently and concurrently with iSBC 80 single board computer functions

Fixed point integer arithmetic
- **16- and 32-bit format**
- **Multiply and divide**
- **Extended divide**

Floating point arithmetic
- **Intel standard 32-bit format**
- **Add, subtract, multiply, divide**
- **Square and square root**

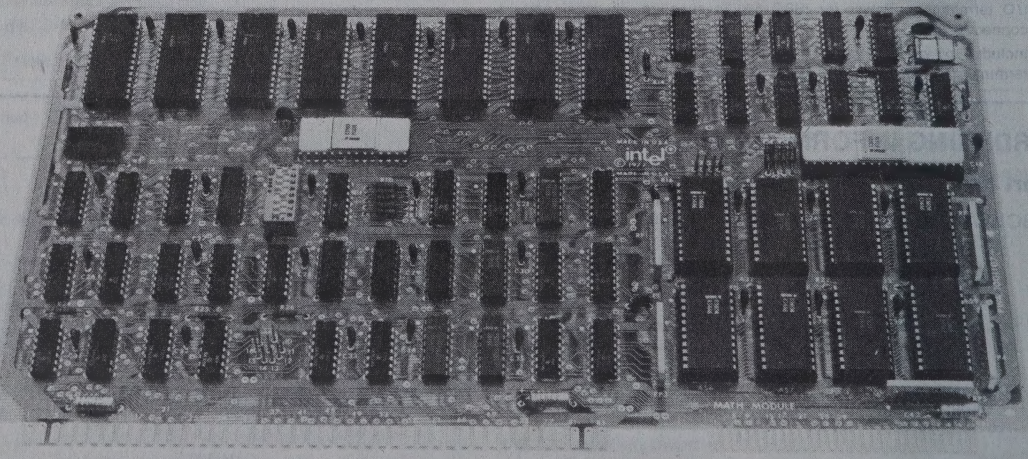
Compare and test operation
- **Relative to zero**
- **Relative to floating point constant**

Float-to-fix and fix-to-float conversions

Multimaster access — multiple masters may access iSBC 310 via system bus

Single +5V power requirement

The iSBC 310 High Speed Mathematics Unit is a member of Intel's complete family of OEM computers and expansion modules. The iSBC 310 acts as an intelligent slave processor to one or more iSBC computer masters as it performs its high speed arithmetic functions. It plugs into a standard iSBC 604/614 cardcage to interface directly into any iSBC 80 single board computer. Designed to increase the computational throughput of all computers in the iSBC 80 family, the iSBC 310 utilizes Intel's high speed Series 3000 Bipolar Microprocessor. The iSBC 310 performs arithmetic functions an order of magnitude faster than is possible with software routines. Standard operations include floating point add, subtract, multiply, divide, square, and square root; fixed point integer multiply, divide, and extended divide; and conversions between fixed and floating point representations, as well as test, compare, and argument exchange.



FUNCTIONAL DESCRIPTION

iSBC 80 single board computers communicate with the iSBC 310 using I/O and memory read/write commands. To pass arguments from the iSBC 80 to the iSBC 310, a memory write command is used for each byte to be loaded into the iSBC 310's working registers. An operation command is then given to the iSBC 310 by using an output instruction to pass the appropriate opcode. The mathematics unit will then perform the function independently from the single board computer; therefore, any iSBC 80 can continue to operate while the iSBC 310 is performing its arithmetic operations. Upon completion of its designated operation, the high speed mathematics unit notifies the iSBC 80 via an interrupt or by setting a status bit. The resultant data can then be read by the iSBC 80 via a memory read command to the proper memory address.

Arithmetic Functions

The iSBC 310 provides a full complement of arithmetic functions which operate on 16- and 32-bit unsigned fixed point integers, 32-bit signed fixed point integers, and 32-bit single precision floating point numbers. These functions are detailed in Table 1. The results of comparison operations are described in the operation results section.

Status Byte

The iSBC 310 may be operated in either an interrupt driven or polled mode. Three status indications are available:

Busy — The iSBC 310 is currently processing an arithmetic command, and cannot respond to further requests.

Complete — The iSBC 310 has completed an operation without error. This line may be connected to an interrupt level via an on-board jumper.

Error — The iSBC 310 has completed an operation which results in an error condition. This line may be connected to an interrupt level via an on-board jumper.

Result Byte

After completion of an operation, a result byte may be read. This byte indicates the error conditions where applicable (see Specifications), and the results of a compare or test operation.

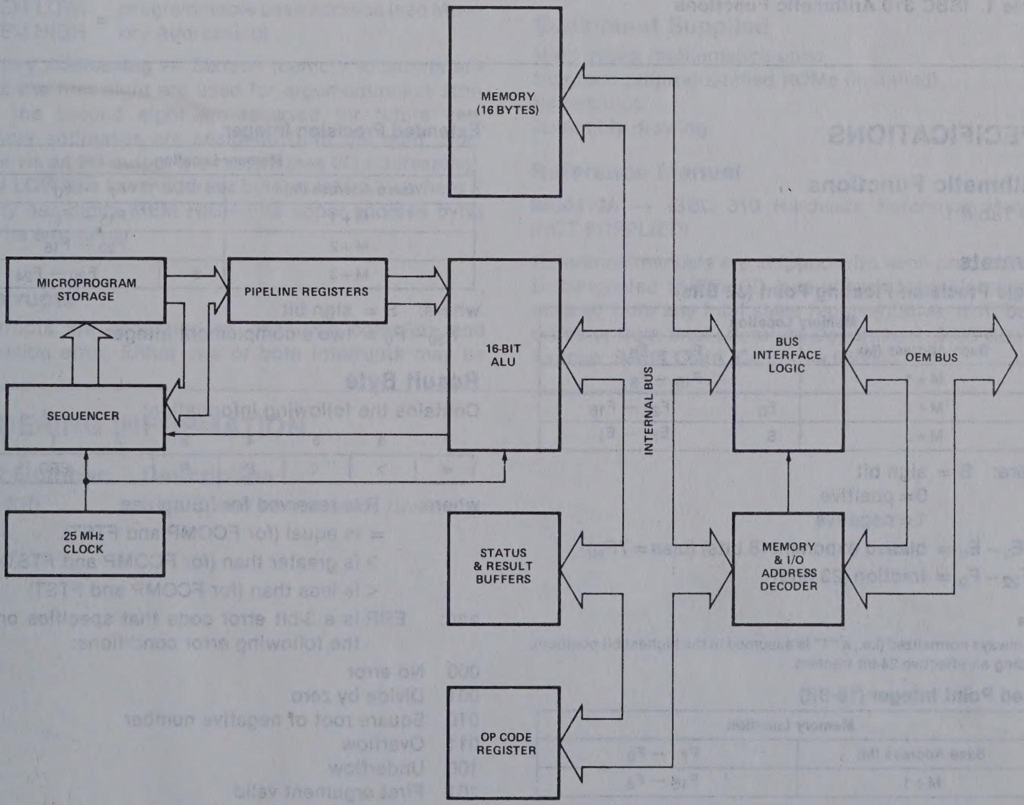


Figure 1. iSBC 310 Block Diagram Showing Functional Components

Operation	Op Code	Max Time[1] (μs)	Notes[2]
Fixed point multiply (MUL)	0	19	$M_1 = m_1 * m_1$
Fixed point divide (DIV)	1	28	$m_1 = m_1/M_2$, $m_2 =$ remainder
Extended fixed point divide (EDIV)	E	94	$M_1 = M_1/m_2$, $M_2 =$ remainder
Floating point multiply (FMUL)	2	91	$X_1 = X_1 * X_2$
Floating point divide (FDIV)	3	102	$X_1 = X_1/X_2$
Floating point add (FADD)	4	56	$X_1 = X_1 + X_2$
Floating point subtract (FSUB)	5	56	$X_1 = X_1 - X_2$
Square (FSQR)	6	91	$X_1 = X_1^2$
Square root (FSQRT)	7	199	$X_1 = \sqrt{X_1}$
Fixed-to-float-conversion (FLOAT)	8	89	$X_1 = N_1$
Float-to-fixed-conversion (FIX)	9	81	$N_1 = X_1$
Compare (FCOMP)	A	5	Compare X_1 and X_2
Test (FTST)	B	5	Compare X_1 and 0.0
Exchange (EXCH)	F	4	Exchange arguments (fixed or floating)

Notes

1. Does not include register setup time
2. m — 16-bit unsigned fixed point integers; M — 32-bit unsigned fixed point integer; N — 32-bit two's complement signed fixed integer; X — 32-bit single precision floating point number

Table 1. iSBC 310 Arithmetic Functions

SPECIFICATIONS

Arithmetic Functions

See Table 1

Formats

Single Precision Floating Point (32 Bits)

Memory Location		
Base Address (M)	$F_7 - F_0$	
M + 1	$F_{15} - F_8$	
M + 2	E_0	$F_{22} - F_{16}$
M + 3	S	$E_7 - E_1$

where: S = sign bit
0 = positive
1 = negative
$E_2 - E_0 =$ biased exponent (8 bits) (bias $= 7F_H$)
$F_{22} - F_0 =$ fraction (23 bits)

Note

F is always normalized (i.e., a "1" is assumed in the highest bit position), yielding an effective 24-bit fraction.

Fixed Point Integer (16-Bit)

Memory Location	
Base Address (M)	$F_7 - F_0$
M + 1	$F_{15} - F_8$

where:
$F_{15} - F_0 =$ 16-bit integer

Extended Precision Integer

Memory Location		
Base Address (M)	$F_7 - F_0$	
M + 1	$F_{15} - F_8$	
M + 2	$F_{23} - F_{16}$	
M + 3	S	$F_{30} - F_{24}$

where: S = sign bit
$F_{30} - F_0 =$ two's complement integer

Result Byte

Contains the following information:

7	6	5	4	3	2	1	0
=	>	<	R	R		ERR	

where: R is reserved for future use
= is equal (for FCOMP and FTST)
> is greater than (for FCOMP and FTST)
< is less than (for FCOMP and FTST)

and: ERR is a 3-bit error code that specifies one of the following error conditions:

000	No error
001	Divide by zero
010	Square root of negative number
011	Overflow
100	Underflow
101	First argument valid
110	Second argument valid
111	Reserved

Status Byte

Contains the following information:

7	6	5	4	3	2	1	0
R	R	R	R	R	E	C	B

where: R is reserved for future use
B is busy
C is operation complete without error
E is operation complete with error

Addressing

I/O Addressing — Used to pass operation codes, memory address boundaries, and result and status bytes between host processor and iSBC 310.

Port Address	Output	Input
Base (P)	OP CODE	R
P+1	MEM LOW	Result byte
P+2	MEM HIGH	R
P+3	R	R
P+4	R	R
P+5	R	R
P+6	R	R
P+7	R	Status byte

where: P = I/O base address of X0 or X8 (where X = any hex digit)
R = reserved for iSBC 310 usage
OP CODE = mathematic commands (see Table 1)
MEM LOW, MEM HIGH = programmable base address (see Memory Addressing)

Memory Addressing — Sixteen memory locations are used; the first eight are used for argument/result storage; the second eight are reserved for future use. Memory addresses are assigned from the host processor via an I/O output instruction (see I/O Addressing). MEM LOW (the lower address byte) must be X0 (where X is any hex digit). MEM HIGH (the upper address byte) may be any value.

Interrupts

Interrupts are generated on operation complete and operation error. Either one or both interrupts may be connected to any of the 8 interrupt levels on the iSBC 80 bus via jumper selection.

Bus Interface

All signals are TTL compatible.

Bus Connector

Bus Connector — 86-pin, double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Viking 3KH43/9AMK12

Physical Characteristics

Width — 12.00 in (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

V_{CC}	I_{CC}
5V ± 5%	6.7A max; 4.9A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Equipment Supplied

High speed mathematics units
Standard preprogrammed ROMs (installed)
Schematics
Assembly drawing

Reference Manual

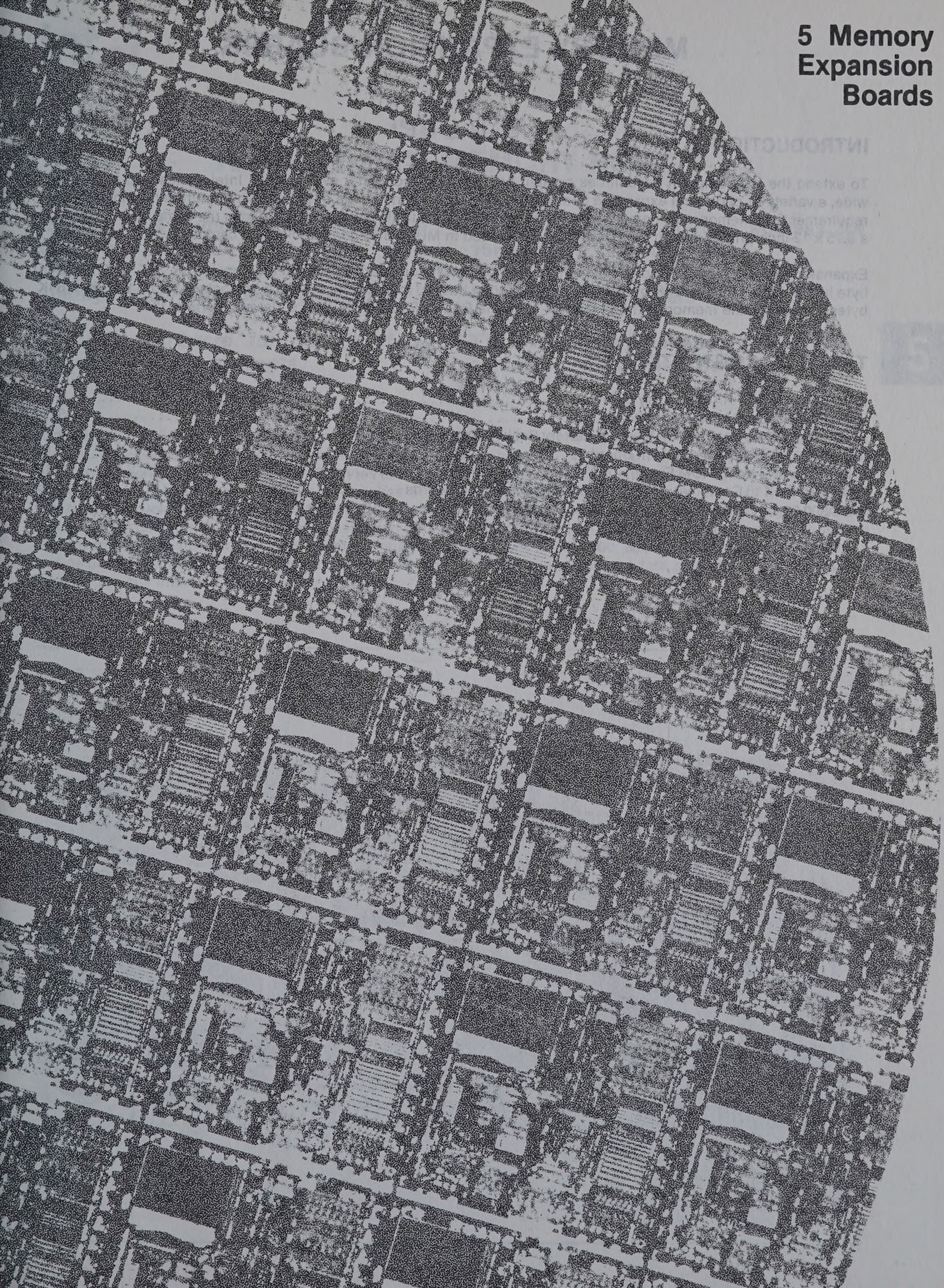
9800410A — iSBC 310 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 310	High Speed Mathematics Unit

5 Memory Expansion Boards



MEMORY EXPANSION BOARDS

INTRODUCTION

To extend the full computer capabilities present on each iSBC computer even further, Intel makes available, worldwide, a variety of peripheral expansion boards designed to meet the needs of those manufacturers having increased requirements in memory. All memory expansion modules in the iSBC family are provided in the same form factory (on a 6.75 × 12-inch printed circuit card), and may be housed in MULTIBUS-compatible Intel cardcages.

Expansion memory modules include dynamic RAM boards with on-board read/write memory in 16K, 32K, 48K, and 64K byte increments. There is a 4K byte CMOS, RAM battery backup module and boards with sockets for up to 16K or 64K bytes of non-volatile memory. Three modules combine RAM, EPROMROM, and serial and parallel I/O.

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iSBC 016
16K-BYTE RAM MEMORY BOARD

iSBC-80 RAM memory expansion through direct bus interface

16K-byte read/write memory capacity

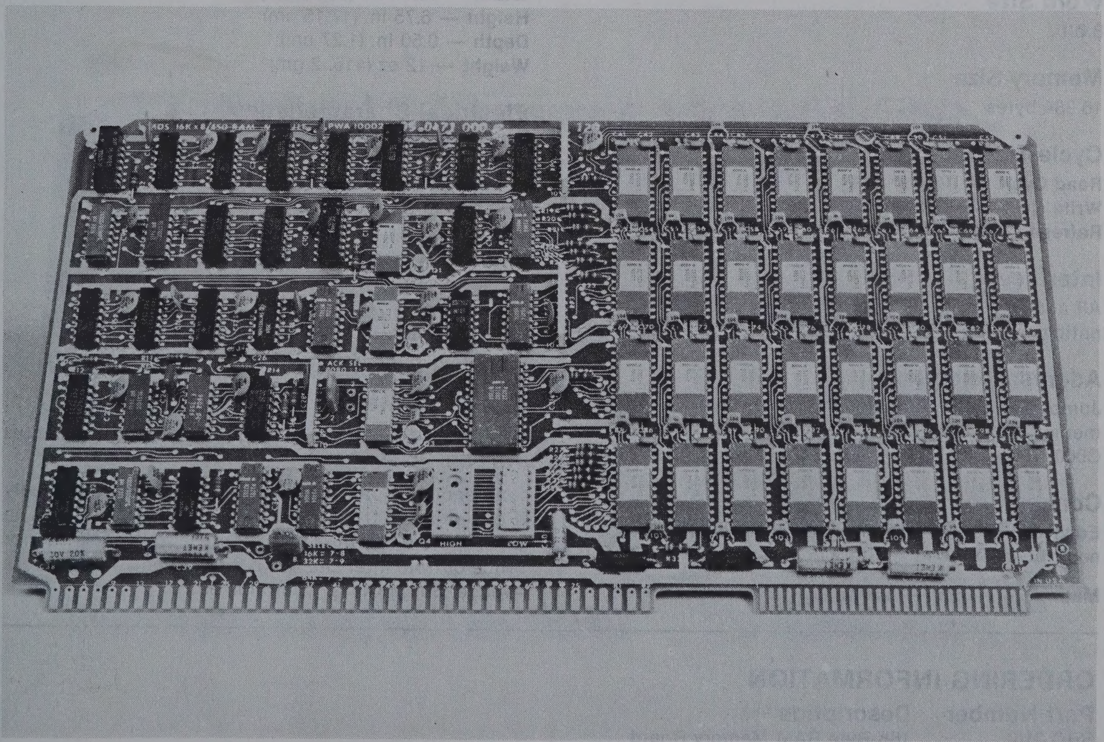
On-board hardware for refresh of all dynamic memory elements

Jumper selectable starting address for 16K contiguous addresses

Read/write data buffers

TTL compatible data, address, and command signal interface

The iSBC 016 16K-Byte Ram Memory Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 016 interfaces directly to any iSBC 80 single board computer via the system bus to expand RAM memory capacity. The board contains 16K bytes of read/write memory, implemented using 2107 dynamic RAM memory components. On-board refresh hardware refreshes 64 bit positions of all 32 RAM elements every 14 microseconds. Each refresh cycle utilizes memory for 735 nanoseconds. If a read or write cycle is in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the cycle. The iSBC 016 contains a jumper used to select contiguous 16K-byte address segments starting in locations 0000, 4000, 8000, or C000. Read/Write buffers reside on the board to buffer all data written into or read from the memory array. All data, address, and command signals on the bus interface are TTL compatible.



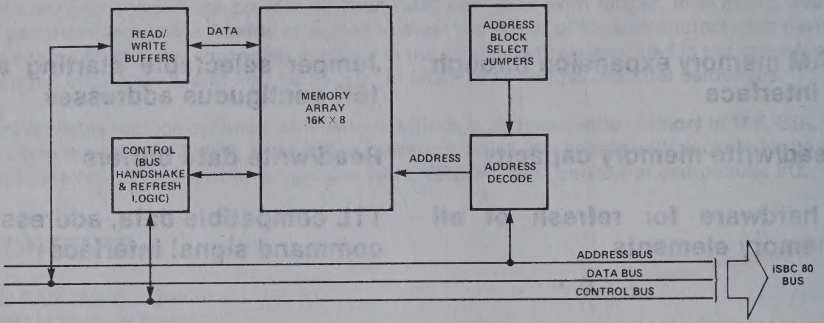

READ/ WRITE BUFFERS
DATA
MEMORY ARRAY 16K × 8
ADDRESS BLOCK SELECT JUMPERS
CONTROL (BUS HANDSHAKE & REFRESH LOGIC)
ADDRESS
ADDRESS DECODE
ADDRESS BUS
DATA BUS
CONTROL BUS
iSBC 80 BUS

Figure 1. iSBC 016 16K RAM Memory Expansion Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

16,384 bytes

Cycle Times

Read Cycle — 735 ns max
Write Cycle — 1360 ns max
Refresh Cycle — 735 ns max

Interface

All address, data, and command signals are TTL compatible.

Address Selection

Jumper selection of base address of 16K contiguous memory block to reside in locations 0000, 4000, 8000, or C000.

Connectors

Edge Connector — 86-pin double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Viking 3KH43/9AMK12

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (415. 2 gm)

Electrical Characteristics

DC Power Requirements

V_{CC} = + 5V DC ± 5%
I_{CC} = 1.2A typ; 1 5A max
V_{DD} = + 12V DC ± 5%
I_{DD} = 0.7A typ; 1.0A max
V_{BB} = − 5V DC ± 5%
I_{BB} = 0.2 mA typ; 3.2 mA max

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manual

9800279A — iSBC 016 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 016	16K-Byte RAM Memory Board

iSBC 032/048/064 RAM MEMORY BOARDS

iSBC 80 and iSBC 86 RAM memory expansion through direct MULTIBUS interface

32K, 48K, 64K bytes of read/write memory (iSBC 032, iSBC 048, iSBC 064 boards, respectively)

On-board hardware for refresh of all dynamic memory elements

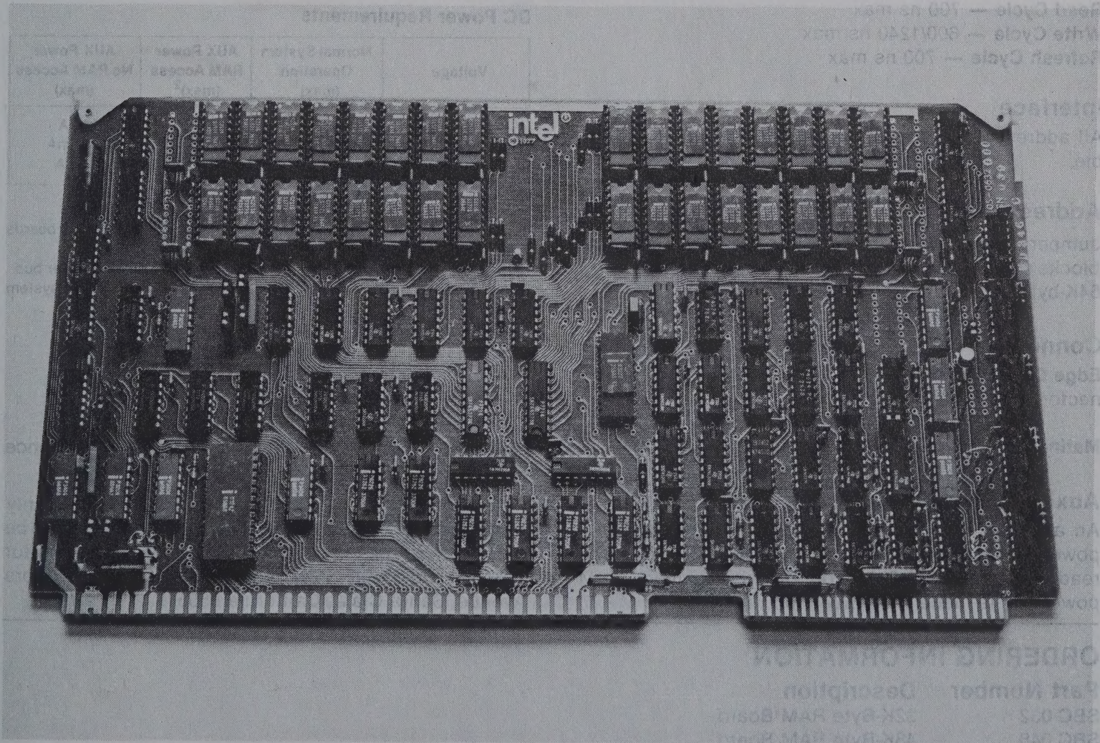
Auxiliary power bus and memory protect control logic provided for battery backup RAM requirements

Jumper selectable starting address for independent 16K-byte memory segments

Read/write data buffers

TTL compatible data, address, and command signal interface

The iSBC 032, iSBC 048, and iSBC 064 RAM Memory Boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Each board interfaces directly to any Intel iSBC 80 or iSBC 86 single board computer via the MULTIBUS interface to expand RAM memory capacity. The iSBC 032 contains 32K, the iSBC 048, 48K, and the iSBC 064, 64K bytes of read/write memory implemented using dynamic RAM memory components. On-board refresh hardware refreshes a portion of RAM memory every 14 microseconds. Each refresh cycle utilizes memory for 585 nanoseconds. If a read or write cycle is in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the cycle. The iSBC 032 contains jumpers used to individually select two independent 16-byte memory segments, and the iSBC 048 contains jumpers used to individually select three independent 16K-byte memory segments starting on 16K-byte boundaries in one of sixteen 64K-byte pages. Read/write buffers reside on each board to buffer all data written into or read from the memory array. All data, address, and command signals on the bus interface are TTL compatible.



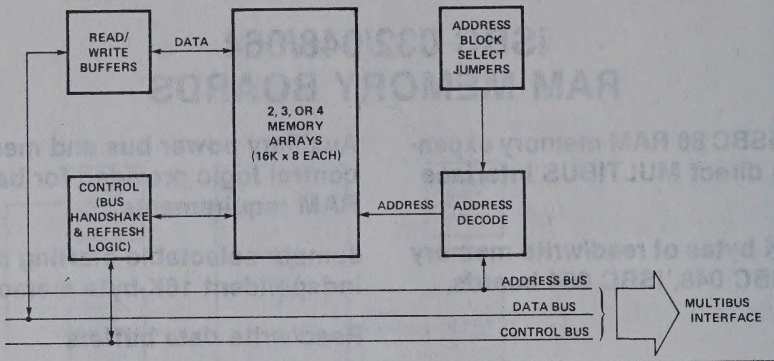

READ/ WRITE BUFFERS
DATA
2, 3, OR 4 MEMORY ARRAYS (16K x 8 EACH)
ADDRESS BLOCK SELECT JUMPERS
CONTROL (BUS HANDSHAKE & REFRESH LOGIC)
ADDRESS
ADDRESS DECODE
ADDRESS BUS
DATA BUS
CONTROL BUS
MULTIBUS INTERFACE

Figure 1. RAM Memory Expansion Boards Block Diagram

SPECIFICATIONS

Word Size

8 bits and 16 bits

Memory Size

32,768 bytes (iSBC 032), 49,152 bytes (iSBC 048), 65,536 bytes (iSBC 064)

Access Time

450 ns max

Cycle Times

Read Cycle — 700 ns max
Write Cycle — 600/1240 ns max
Refresh Cycle — 700 ns max

Interface

All address, data, and command signals TTL compatible.

Address Selection

Jumper selection for independent 16K-byte memory blocks starting on 16K-byte boundaries in one of sixteen 64K-byte pages.

Connectors

Edge Connectors — 86-pin double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Viking 3KH43/9AMK12

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery back up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.76 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (415.2 gm)

Electrical Characteristics

DC Power Requirements

Voltage	Normal System Operation (max)[1]	AUX Power RAM Access (max)[2]	AUX Power No RAM Access (max)
$V_{CC} = +5V \pm 5\%$	$I_{CC} = 3.2A$	1.7A	1.7A
$V_{DD} = +12V \pm 5\%$	$I_{DD} = 600$ mA	600 mA	120 mA
$V_{BB} = -5V \pm 5\%$	$I_{BB} = 10$ mA	10 mA	3 mA

Notes

1. All current values apply to the iSBC 032, iSBC 048 or iSBC 064 boards and include AUX power.
2. RAM chips and RAM control logic powered via auxiliary power bus.
3. Power necessary to refresh RAMs and maintain data, as after system power failure.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800488B — iSBC 032/048/064 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 032	32K-Byte RAM Board
SBC 048	48K-Byte RAM Board
SBC 064	64K-Byte RAM Board

iSBC 094
4K-BYTE CMOS RAM MEMORY BATTERY BACKUP BOARD

iSBC 80 nonvolatile RAM memory expansion through direct bus interface

4K bytes of low power static CMOS RAM memory

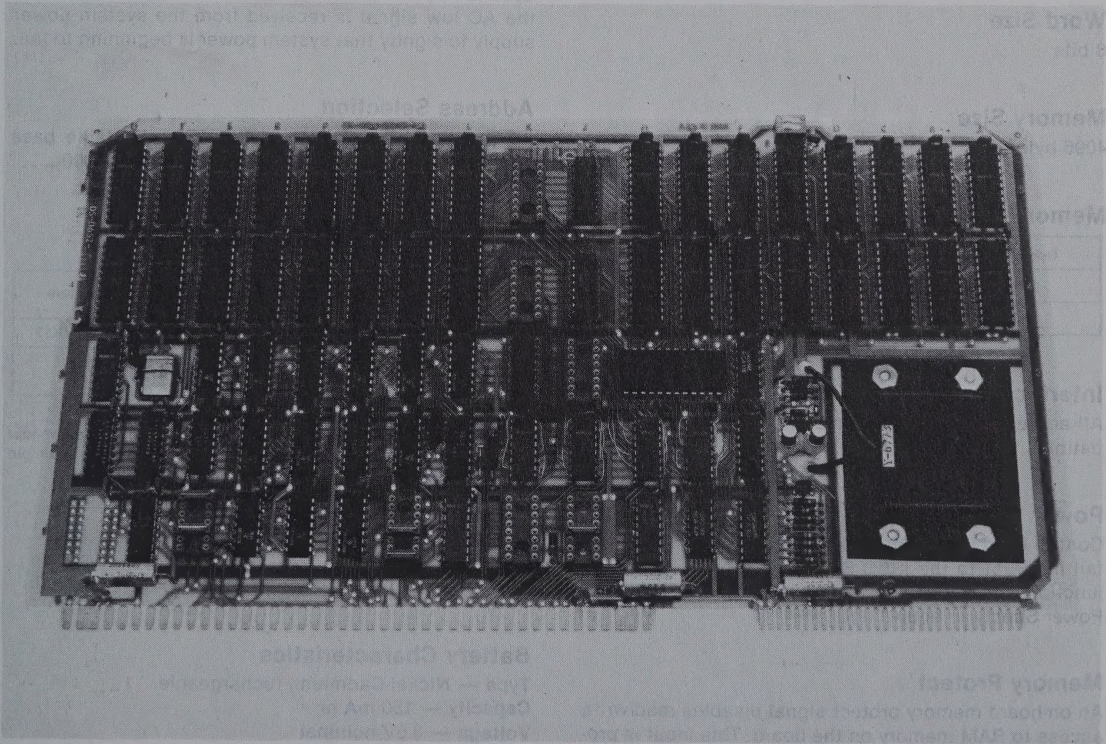
On-board power-fail interface logic

Base address selectable to start on any 4K memory address boundary

On-board rechargeable batteries and charging circuitry for 96-hour data retention

Single +5V power requirement

The iSBC 094 4K-Byte CMOS RAM Memory/Battery Backup Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 094 interfaces directly to iSBC 80 single board computer via the system bus to expand RAM memory capacity. The board contains 4K bytes of read/write memory, implemented using 32 Intel 5101 CMOS RAM memory components. On-board rechargeable batteries and charging circuitry insure that data contained in RAM will be retained for at least 96 hours after system bus power (+5V) is removed. Critical system parameters stored in the iSBC 094 RAM will thus be saved during temporary system power failures. Full power-fail interface logic is provided on the board to generate a CPU interrupt when system power fails. Orderly system shutdown procedures may then be executed and critical system parameters may be retrieved and stored. The use of CMOS RAM on the iSBC 094 also reduces power dissipation during normal system operation. The iSBC 094 contains jumpers for use in selecting a contiguous 4K-byte address segment beginning on any 4K memory address boundary (0000H, 1000H, 2000H, etc). Read/write buffers reside on the board to buffer all data written into or read from the memory array. All address, data, and command signals on the bus interface are TTL compatible.



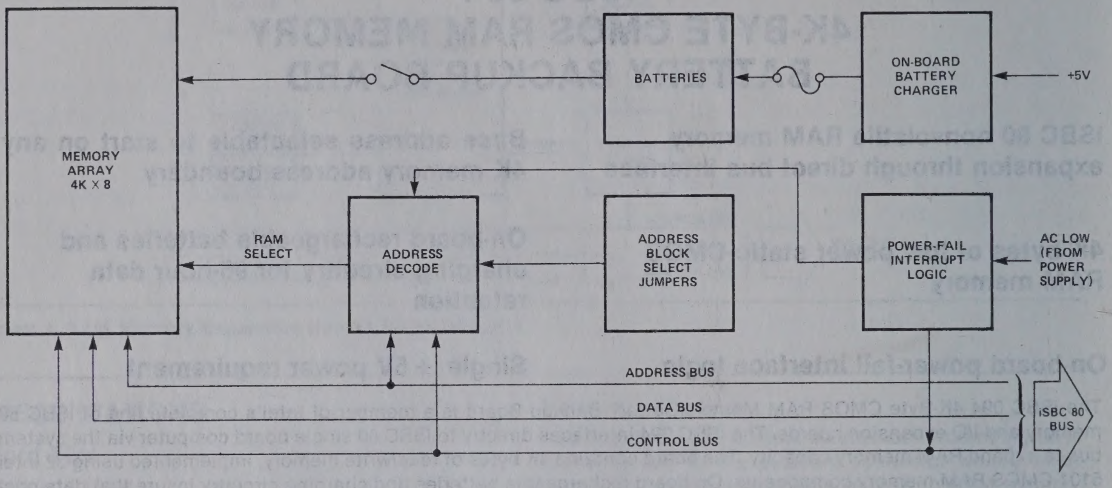

MEMORY
ARRAY
4K × 8
BATTERIES
ON-BOARD
BATTERY
CHARGER
+5V
RAM
SELECT
ADDRESS
DECODE
ADDRESS
BLOCK
SELECT
JUMPERS
POWER-FAIL
INTERRUPT
LOGIC
AC LOW
(FROM
POWER
SUPPLY)
ADDRESS BUS
DATA BUS
CONTROL BUS
iSBC 80
BUS

Figure 1. iSBC 094 Memory Backup Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

4096 bytes

Memory Response Time

Operation	Access (ns, max)	Cycle (ns, max)
Read	750	900
Write	—	900

Interface

All address, data, and command signals are TTL compatible.

Power Fail Interrupt

Control logic is also included for generation of a power-fail interrupt to the iSBC 80 bus, which works in conjunction with the AC low signal from the Intel iSBC 635 Power Supply or equivalent.

Memory Protect

An on-board memory protect signal disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. This signal is automatically asserted by the power-fail interface logic 3.6 ms after the AC low signal is received from the system power supply to signify that system power is beginning to fail.

Address Selection

4K segments starting at any jumper selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, . . . $F000_H$).

Mating Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Auxiliary[1]	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector Dimensions vary from vendor to vendor. Review vendor specifications to ensure that connector heights and wire-wrap pin lengths to conform to your system packaging requirements.

Data Retention

96 hours minimum after +5V bus power is removed.

Battery Characteristics

Type — Nickel-Cadmium, rechargeable
Capacity — 150 mA hr
Voltage — 3.6V nominal

Battery Charger Characteristics

Charge Time

14 hours for full charge (150 mA hr)

Full overcharge protection

Full short-circuit protection

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.60 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

Average DC Current

V_{CC} = +5V DC ±5%

I_{CC} = 0.8A typ, 1.7A max

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manual

9800449B — iSBC 094 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 094	4K-Byte CMOS RAM Memory Battery Backup Board

iSBC 416
16K PROM EXPANSION BOARD

Allows iSBC 80 EPROM/ROM expansion through direct bus interface

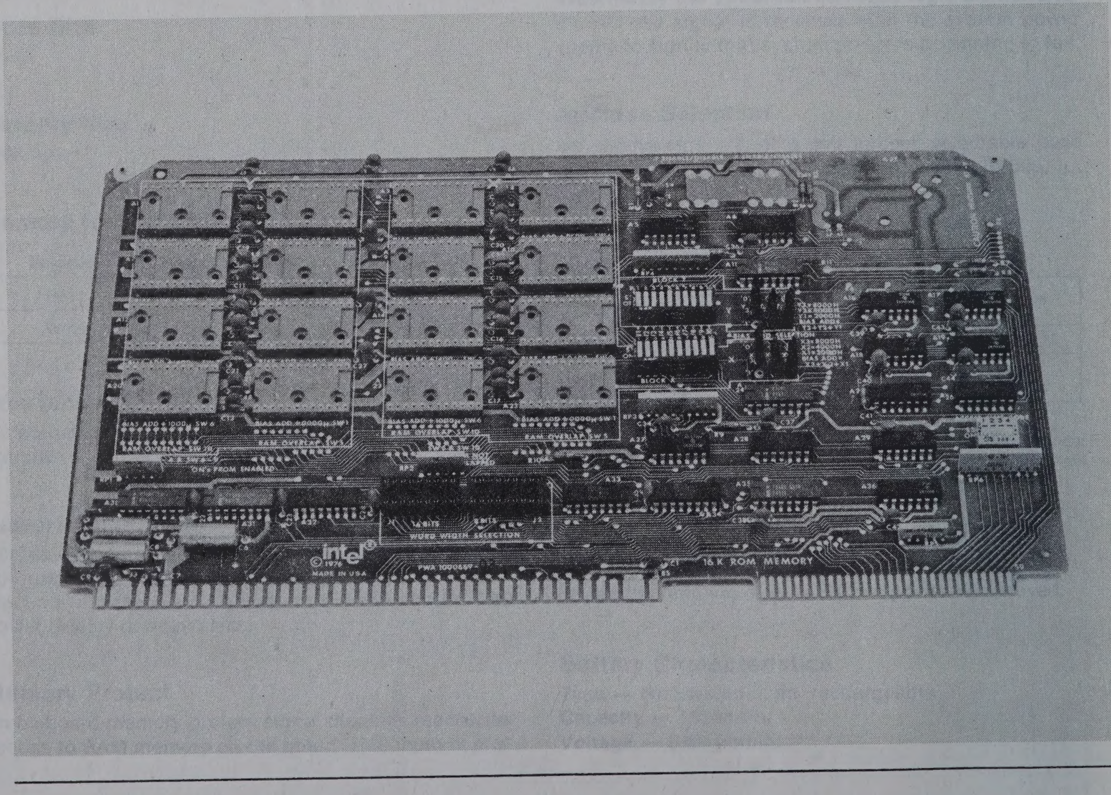
Sockets for up to 16K bytes of interchangeable Intel 2608 ROM or 2708 programmable and erasable PROM

Switches to enable or disable each memory block

Jumper selectable addresses for each 8K block

Buffered address and data lines

The iSBC 416 16K PROM Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 416 interfaces directly to any iSBC 80 single board computer via the system bus to expand ROM/PROM memory capacity. The board contains 16 sockets that can house either Intel 2608 masked ROMs or Intel 2708 programmable and erasable EPROMs. ROM/PROM memory can be added in 1K-byte increments. The iSBC 416 contains a set of jumpers allowing the selection of the base address of independent 8K memory blocks, to begin on any 8K boundary. Switches are used to enable on-board memory in 1K-block increments.



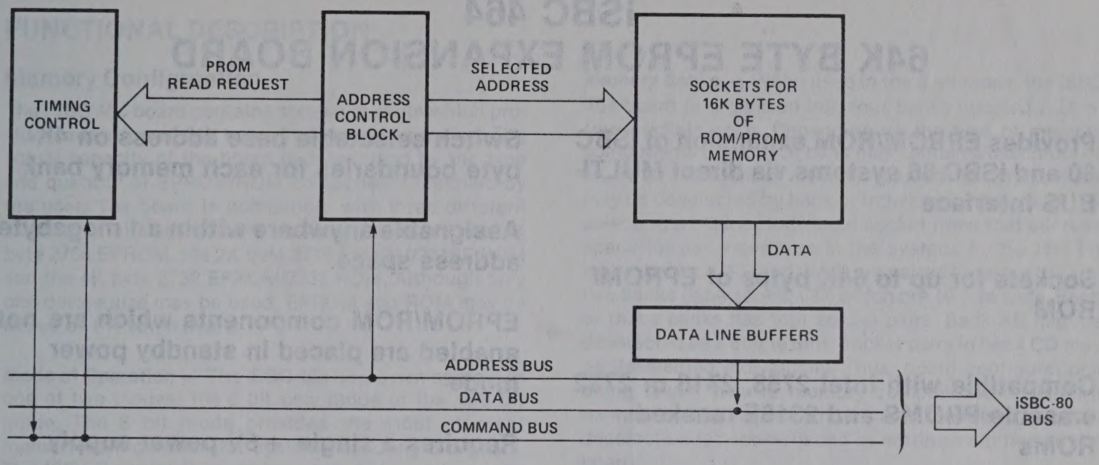

TIMING CONTROL
PROM READ REQUEST
ADDRESS CONTROL BLOCK
SELECTED ADDRESS
SOCKETS FOR 16K BYTES OF ROM/PROM MEMORY
DATA
DATA LINE BUFFERS
ADDRESS BUS
DATA BUS
COMMAND BUS
iSBC-80 BUS

Figure 1. iSBC 416 PROM Expansion Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

Sockets for up to 16K bytes. Memory may be added in 1K-byte increments.

Compatible Intel Memory

ROM — 2608
PROM — 2708

Interface

All address, data, and command signals are TTL compatible and iSBC 80 bus compatible.

Address Selection

Switches and jumpers allowing the selection of a base address for each independent 8K block of memory, on any 8K boundaries

Connectors

Edge Connector — 86-pin double-sided PC edge connector with 0.156-in. (0.40 cm) contact centers.

Mating Connector — Viking 3KH43/9AMK12

Physical Characteristics

Width — 12.00 in. (30.40 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

	Without Memory	With 2608		With 2708	
		Typ	Max	Typ	Max
+5V	0.75A	0.77A	0.79A	0.85A	0.91A
−5V	—	0.001A	0.010A	0.48A	0.75A
+12V	—	0.58A	0.96A	0.80A	1.04A

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800265A — iSBC 416 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 416	16K PROM Expansion Board

iSBC 464
64K BYTE EPROM EXPANSION BOARD

Provides EPROM/ROM expansion of iSBC 80 and iSBC 86 systems via direct MULTIBUS interface

Sockets for up to 64K bytes of EPROM/ROM

Compatible with Intel 2758, 2716 or 2732 erasable PROMS and 2316E masked ROMs

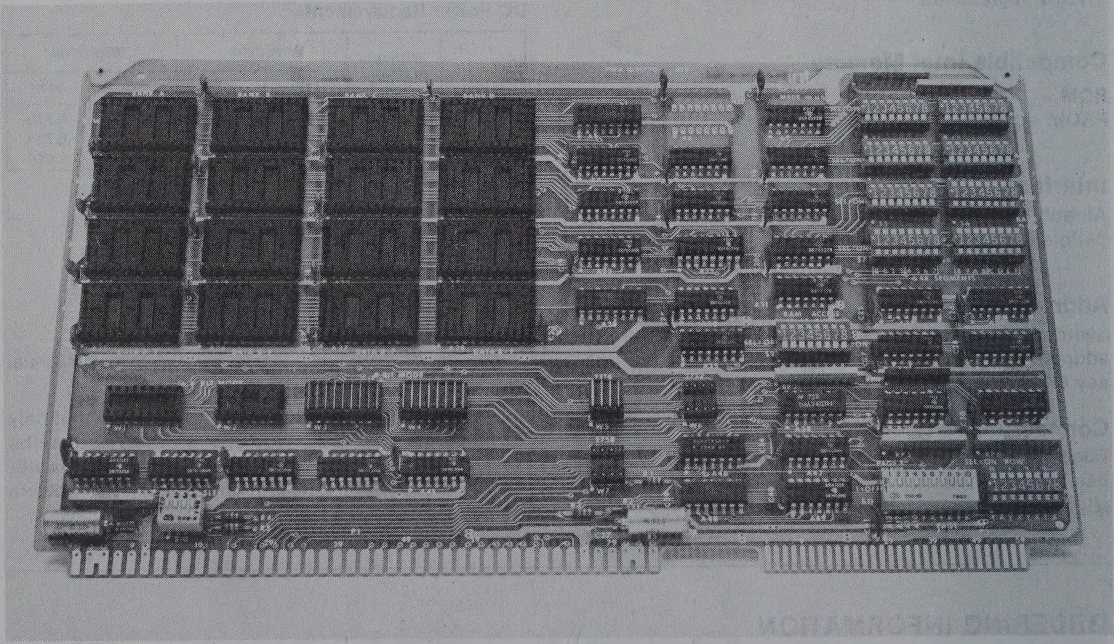
Switch selectable base address on 4K-byte boundaries for each memory bank

Assignable anywhere within a 1 megabyte address space

EPROM/ROM components which are not enabled are placed in standby power mode

Requires a single +5V power supply

The iSBC 464 64K Byte EPROM Expansion Board is a member of Intel's complete line of iSBC memory and I/O expansion boards. The iSBC 464 board interfaces directly to the iSBC 80 or iSBC 86 single board computers via the MULTIBUS system bus, to expand system EPROM/ROM memory capacity.



FUNCTIONAL DESCRIPTION

Memory Configuration

The iSBC 464 board contains sixteen sockets which provide a maximum of 64K bytes of memory expansion. The actual capacity of the board is determined by the type and quantity of EPROM/ROM components installed by the user. The board is compatible with three different sizes of Intel EPROM/ROM devices. These are the 1K byte 2758 EPROM, the 2K byte 2716 EPROM/2316E ROM and the 4K byte 2732 EPROM/2332 ROM. Although only one device size may be used, EPROM and ROM may be mixed on the same board.

Mode of Operation — The iSBC 464 board can operate in one of two modes: the 8 bit only mode or the 16/8 bit mode. The 8 bit mode provides the most efficient memory configuration for systems handling 8 bit data. The 16/8 bit mode allows 16 bit words to be accessed by 16 bit processors. In the 16/8 bit mode, 16 bit and 8 bit microprocessors may also access either the high order byte or the low order byte of a 16 bit word. The mode of operation is selected by placing two option jumper blocks in the appropriate sockets.

Memory Banks — When used in the 8 bit mode, the iSBC 464 board is organized into four banks (labeled A-D) of four sockets each. Depending on the type of memory components used, each bank may contain a maximum of 4K, 8K or 16K bytes of memory. Unused memory sockets may be deselected by bank or individually in bank D. Deselecting a bank or individual socket frees that address space for use elsewhere in the system. In the 16/8 bit mode, banks A & B and C & D are paired together to form two banks (labeled AB, CD) which are 16 bits wide. Each of these banks has four socket pairs. Bank AB may be deselected as a single unit. Socket pairs in bank CD may be deselected individually. Thus, board configurations using fewer than 16 memory components do not fill memory address space with unused sockets. Selection/deselection is accomplished by setting switches on the board.

Memory Access Time — The iSBC 464 board operates with one of 15 switch selectable memory access times ranging from 35 to 1435 nanoseconds. This feature allows the board to be tailored to the performance of the installed components and the system CPU.

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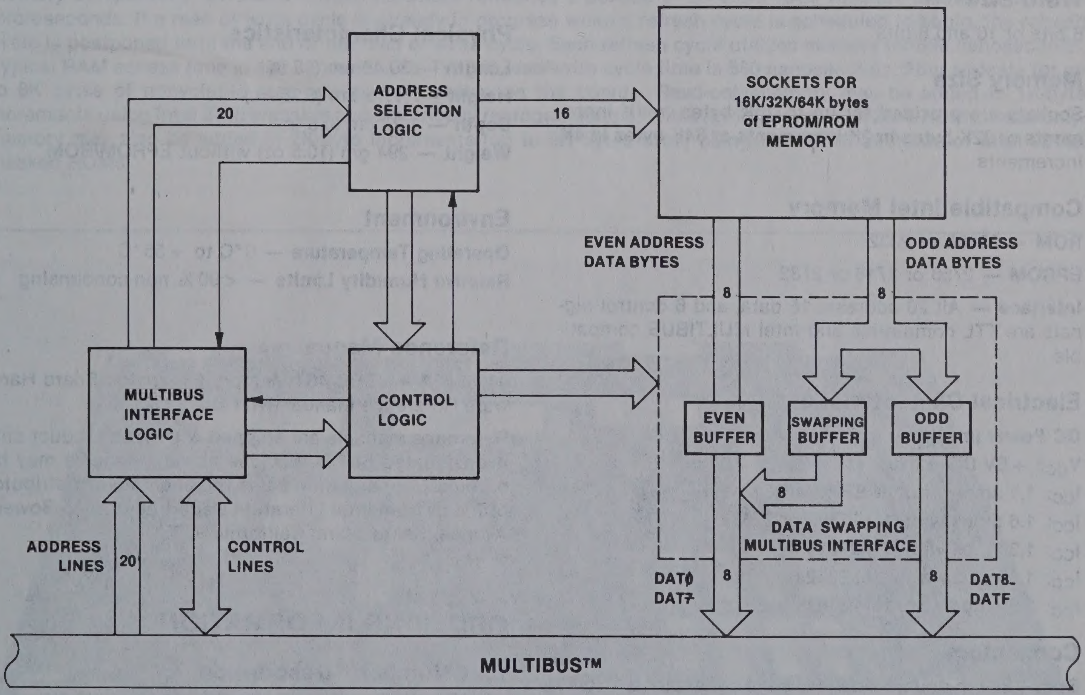


ADDRESS SELECTION LOGIC
20
16
SOCKETS FOR 16K/32K/64K bytes of EPROM/ROM MEMORY
EVEN ADDRESS DATA BYTES
ODD ADDRESS DATA BYTES
8
8
MULTIBUS INTERFACE LOGIC
CONTROL LOGIC
EVEN BUFFER
SWAPPING BUFFER
ODD BUFFER
8
DATA SWAPPING MULTIBUS INTERFACE
ADDRESS LINES
20
CONTROL LINES
DAT0 DAT7
8
8
DAT8 DATF
MULTIBUS™

Figure 1. iSBC 464 BLOCK DIAGRAM

Memory Addresses

Switch selectable options on the iSBC 464 board allow the board to be assigned anywhere within a 1 megabyte address space. In either operating mode, the base address of each memory bank may be set to any 4K byte boundary within a 64K byte memory page. There is one exception. If the 4K byte devices are used in the 16/8 bit mode, then base addresses are restricted to 8K byte boundaries. If the board is used in a system with an address range greater than 64K bytes, memory on the iSBC 464 board may reside in one or two 64K byte memory pages. Any two pages out of a possible 16 may be chosen by setting switches on the board.

Standby Power Operation

The iSBC 464 board takes advantage of the standby modes of the Intel 2758, 2716, 2332, and 2732. When they are not enabled, these components draw as little as 25% of their active level power with no degradation in access time. The iSBC 464 board is designed so that only two memory components are enabled during a read operation.

RAM Overlap

Memory banks of the iSBC 464 board can be overlapped with the addresses of system RAM by setting on-board switches. The process of addressing a memory bank will drive the inhibit RAM (INH1/) signal true. This signal is issued to the MULTIBUS system bus in order to prevent any MULTIBUS accessable RAM in the system from responding to the current address. If an EPROM/ROM is addressed which has its corresponding RAM overlap switch on, an access time of 15 clock cycles is imposed. This allows overlapped dynamic RAM to refresh before the address on the MULTIBUS is changed. The RAM overlap feature does not apply to RAM which is not on the MULTIBUS system bus.

SPECIFICATIONS

Word Size

8 bits or 16 and 8 bits

Memory Size

Sockets are provided for up to 16K bytes in 1K increments or 32K bytes in 2K increments or 64K bytes in 4K increments

Compatible Intel Memory

ROM — 2316E or 2332

EPROM — 2758 or 2716 or 2732

Interface — All 20 address, 16 data, and 6 control signals are TTL compatible and Intel MULTIBUS compatible

Electrical Characteristics

DC Power (max)

V_{CC}: +5V DC ±5%

I_{CC}: 1.1 amps without EPROM/ROMs

I_{CC}: 1.6 amps with (16) 2716s or 2758s

I_{CC}: 1.3 amps with (16) 2732s

I_{CC}: 1.35 amps with (16) 2332s

I_{CC}: 3.0 amps with (16) 2316s

Connectors

Bus — 86-pin double-sided PC edge connector with 0.40 cm (0.156 in.) contact centers

Mating Connector — Viking 3KH43/9AMK12 or compatible connector

Physical Characteristics

Length — 30.48 cm (12 in.)

Height — 17.15 cm (6.75 in.)

Depth — 1.27 cm (0.5 in.)

Weight — 294 gm (10.5 oz) without EPROM/ROM

Environment

Operating Temperature — 0°C to +55°C

Relative Humidity Limits — <90% non-condensing

Reference Manual

9800643A — iSBC 464 Memory Expansion Board Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avanue, Santa Clara, California 95051.

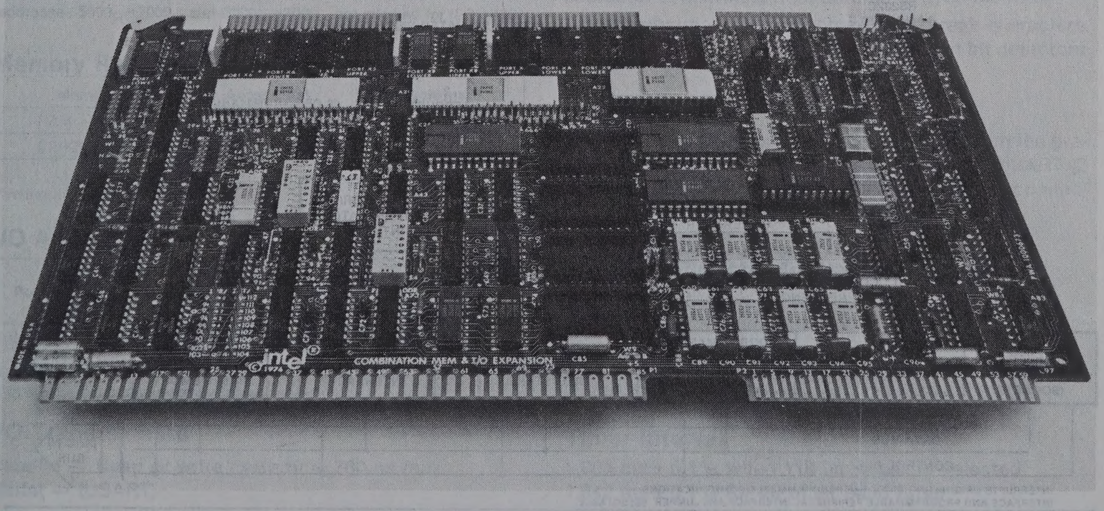
ORDERING INFORMATION

Part Number	Description
SBC 464	64K EPROM Expansion Board

iSBC 104/108/116
COMBINATION MEMORY AND I/O EXPANSION BOARDS

- **4K, 8K, 16K bytes of read/write memory (iSBC 104, iSBC 108, iSBC 116, respectively)**
- **Sockets for up to 8K bytes of programmable or masked read only memory**
- **Auxiliary power bus and memory protect control logic provided for battery backup RAM requirements**
- **48 programmable I/O lines with sockets for interchangeable line drivers and terminators**
- **Synchronous/asynchronous communications interface with RS232C drivers and receivers**
- **Eight maskable interrupt request lines with a pending interrupt register**
- **1 ms interval timer**

The iSBC 104, iSBC 108, and iSBC 116 Combination Memory and I/O Expansion Boards are members of Intel's complete line of iSBC 80 memory and I/O expansion boards. Each board interfaces directly with any iSBC 80 single board computer via the system bus to expand RAM and ROM memory capacity and serial and parallel I/O capacity. The iSBC 104 contains 4K, the iSBC 108 8K, and the iSBC 116 16K bytes of RAM memory implemented using Intel dynamic RAM memory components. On-board refresh hardware refreshes a portion of all eight RAM memory elements every 14 microseconds. If a read or write cycle is already in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the read or write cycle. Each refresh cycle utilizes memory for 590 nanoseconds. Typical RAM access time is 485 nanoseconds. Typical read/write cycle time is 560 nanoseconds. Four sockets for up to 8K bytes of nonvolatile read-only-memory reside on the boards. Read-only-memory may be added in 1K-byte increments using Intel 2708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2608 ROMs. Read-only-memory may also be added in 2K-byte increments (up to 8K bytes total) using Intel 2716 EPROMs or Intel 2316E masked ROMs.



FUNCTIONAL DESCRIPTION

Each combination board contains 48 programmable I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable. Typical I/O read access time is 280 nanoseconds. Typical I/O read cycle time is 600 nanoseconds.

Communications Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on each board. A jumper selectable baud rate generator provides the USART with all common communications frequencies between 75 Hz and 38.4 kHz. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of a comprehensive RS232C interface on the boards in conjunction with the USART provides a direct interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C, serial data lines, and signal ground lines are brought out to a 26-pin edge connector mates with RS232C compatible flat or round cables.

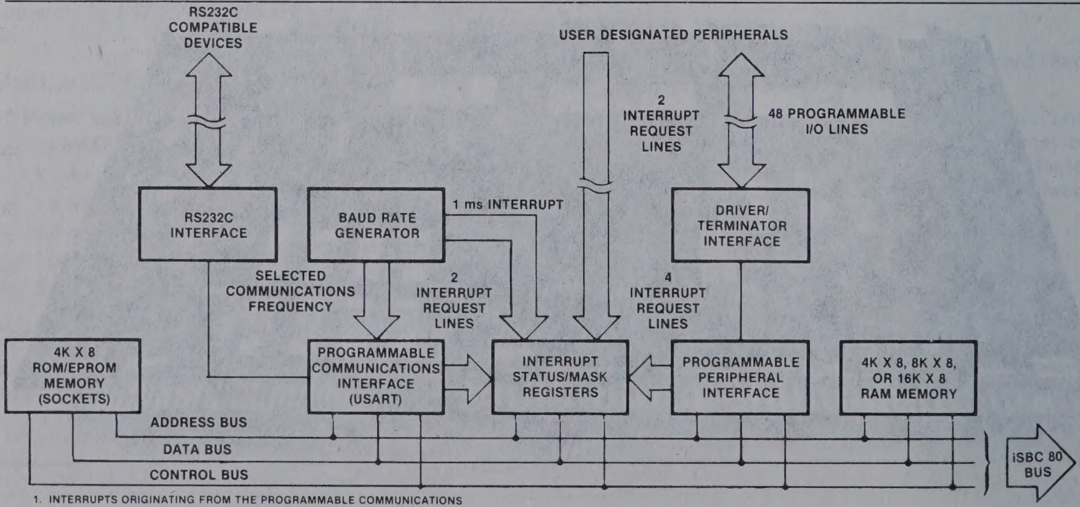
Optically Isolated Interface — The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 104/108/116 combination boards to teletypewriters and other 20 mA current loop equipment.

Interrupt Request Lines

Interrupt requests may originate from eight sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interfaces when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper selectable. They may be ORed to provide a single interrupt request line for the iSBC 80/10A, or they may be individually provided to the system bus for use by the other iSBC 80 single board computers.

Interval Timer

Each board contains a jumper selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.


RS232C COMPATIBLE DEVICES
USER DESIGNATED PERIPHERALS
2 INTERRUPT REQUEST LINES
48 PROGRAMMABLE I/O LINES
RS232C INTERFACE
BAUD RATE GENERATOR
1 ms INTERRUPT
DRIVER/ TERMINATOR INTERFACE
SELECTED COMMUNICATIONS FREQUENCY
2 INTERRUPT REQUEST LINES
4 INTERRUPT REQUEST LINES
4K X 8 ROM/EPROM MEMORY (SOCKETS)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)
INTERRUPT STATUS/MASK REGISTERS
PROGRAMMABLE PERIPHERAL INTERFACE
4K X 8, 8K X 8, OR 16K X 8 RAM MEMORY
ADDRESS BUS
DATA BUS
CONTROL BUS
iSBC 80 BUS

1. INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER SELECTABLE.

Figure 1. iSBC 104/108/116 Combination Memory and I/O Expansion Board Block Diagram

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

SPECIFICATIONS

Memory Addressing

ROM/EPROM — 4K or 8K segments starting at any jumper selectable base address on a 4K-byte boundary (e.g., 0000_H, 10000_H, . . . , $F000_H$)

Note

All EPROM/ROM addresses must reside in the range of 0000_H to $7FFF_H$ or 8000_H to $FFFF_H$.

RAM — 4K, 8K, 16K segments starting at any jumper selectable base address on a 4K-byte boundary (e.g., 0000_H, 1000_H, . . . , $F000_H$).

Note

Base addresses 7000_H and $F000_H$ not allowed for iSBC 108. Base addresses 5000_H→7000_H and $D000_H$→$F000_H$ not allowed for iSBC 116.

Memory Response Time

Memory	Access (ns)	Cycle (ns)
RAM	575 max*	675 max*
EPROM/ROM	465 max	685 max

*Without refresh interruption.

I/O Addressing

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note

X is any hex digit assigned by jumper selection.

I/O Transfer Rate

Parallel — Read or write cycle time 760 ns max

Serial — (USART)

Freqency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Serial Communications Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5—8 bit characters; break characters generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines), or interval timer.

Interrupt Register Addresses

X1 Interrupt mask register
X0 Interrupt status register

Note

X is any hex digit assigned by jumper selection.

Timer Interval

1.003 ms ± 0.1% when 110 baud rate is selected
1.042 ms ± 0.1% for all other baud rates

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — RS232C
Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary Power	60	0.1	AMP PE5-14559 or TI H311130

Note
Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or MDS packaging.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

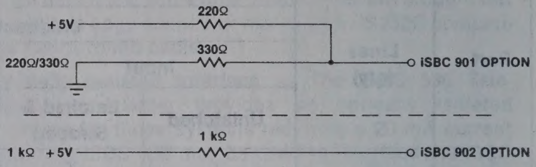
I/O Drivers

The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 104/108/116. Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note
I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup.



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (397.3 gm)

Electrical Characteristics[1]

Average DC Current

Voltage (±5%)	Without EPROM[2] (max)	With 2708 EPROM[3] (max)	With 2716 EPROM[4] (max)	RAM[5] (max)
$V_{CC} = +5V$	$I_{CC} = 2.85A$	3.6A	4.0A	600 mA
$V_{DD} = \pm 12V$	$I_{DD} = 450$ mA	700 mA	450 mA	350 mA
$V_{BB} = -5V$	$I_{BB} = 3$ mA	180 mA	3 mA	3 mA
$V_{AA} = -12V$	$I_{AA} = 60$ mA	60 mA	60 mA	Not Used

Notes
1. All current values given here include RAM power.
2. Does not include power required for optional EPROM, I/O drivers, and I/O terminators.
3. With four 2708 EPROMs and eight 220Ω/330Ω input terminators installed, all terminator inputs low.
4. With four Intel 2716 EPROMs and eight 220Ω/330Ω input terminators installed, all terminator inputs low.
5. RAM chips and RAM control logic (powered via auxiliary power bus).

Environmental Characteristics

Operating Temperature — 0°C to +55°C.

Reference Manuals

9800277—iSBC 104/108/116 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 104	Combination Memory and I/O Expansion Board with 4K bytes RAM
SBC 108	Combination Memory and I/O Expansion Board with 8K bytes RAM
SBC 116	Combination Memory and I/O Expansion Board with 16K bytes RAM

iSBC 300 32K-BYTE RAM EXPANSION MODULE
iSBC 340 16K-BYTE EPROM/ROM EXPANSION MODULE

On-board memory expansion for iSBC 86/12A Single Board Computer

iSBC 300 module provides 32K bytes of dual port dynamic RAM and plugs directly into the iSBC 86/12A board

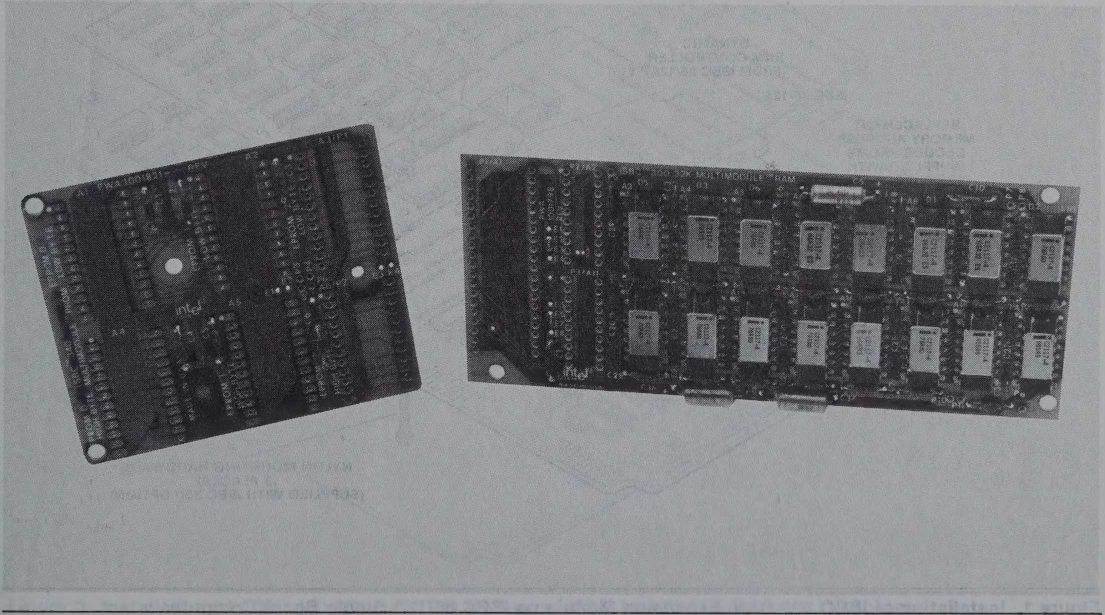
iSBC 340 module provides sockets for up to 16K bytes of additional EPROM/ROM and plugs directly into the iSBC 86/12A board

On-board memory expansion eliminates MULTIBUS system bus latency and increases system throughput

Low power requirements

Simple, reliable mechanical and electrical interconnection

The iSBC 300 32K-byte RAM expansion module and the iSBC 340 16K-byte EPROM/ROM expansion module provide simple, low cost expansion of the memory complement available on the iSBC 86/12A single board computer. Each module utilized individually or together can double the iSBC 86/12A board's on-board RAM and EPROM memory capacity. The iSBC 300 32K-byte RAM expansion module and the iSBC 340 16K-byte EPROM/ROM expansion module options for the iSBC 86/12A board offer system designers a new level of flexibility in defining and implementing Intel® single board computer systems. These options allow the systems designer to double the memory complement of an iSBC 86/12A board with a minimum of system implications. Because they expand the memory configuration on-board, they can be accessed as quickly as the existing iSBC 86/12A memory by eliminating the need for accessing the additional memory via the MULTIBUS system bus. With the iSBC 86/12A board mounted in the top slot of an iSBC 604 or iSBC 614 cardcage, sufficient clearance exists for mounting both the iSBC 300 and/or the iSBC 340 expansion module option(s). If the iSBC 86/12A board is inserted into some other slot, the combination of boards will physically (but not electrically) occupy two cardcage slots. Incremental power required by the options is minimal; for instance, only 305 mW is needed for the iSBC 300 RAM expansion module.



FUNCTIONAL DESCRIPTION

iSBC 300 32K-Byte Expansion Module

The iSBC 300 board measures 7.75″ by 2.35″ and mounts above the RAM area on the iSBC 86/12A single board computer. It expands the iSBC 86/12A board's on-board dual port RAM capacity from 32K bytes to 64K bytes. The iSBC 300 module contains sixteen 16K-byte dynamic RAM devices, sockets for the Intel® 8202 Dynamic RAM Controller and memory interface latching. To install the iSBC 300 module, the latches and controller from the iSBC 86/12A board are removed and inserted into the sockets on the iSBC 300 module. The add-on board is then mounted onto the iSBC 86/12A board. Pins extending from the controller's and latches' sockets mate with the devices' sockets underneath (see Figure 1). Additional pins mate to supply power and other signals to complete the electrical interface. The module is then secured at three additional points with nylon hardware to insure the mechanical security of the assembly.

To complete the installation, two socketed PROMs are replaced on the iSBC 86/12A board with those supplied with the iSBC 300 kit. These are the on-board memory and MULTIBUS address decode PROMs which allow the iSBC 86/12A board logic to recognize its expanded on-board memory complement.

iSBC 340 16K-Byte Expansion Module

The iSBC 340 module expands the iSBC 86/12A Single Board Computer's on-board EPROM capacity from 16K bytes to 32K bytes. It measures 3.3″ by 2.8″ and consists of a PC board with six 24-pin special sockets. Two of the sockets have extended pins which mate with two of the EPROM sockets on the iSBC 86/12A board. Two of the EPROMs which would have been inserted on the iSBC 86/12A board are then reinserted in the iSBC 340 module. Additional pins also mate for bringing chip selects for the remaining EPROM devices (see Figure 2). The mechanical interface is similar to that used on the iSBC 300 RAM module and consists of two additional mounting holes and the necessary mounting hardware.

The iSBC 340 module supports Intel® 2732 EPROM or 2332A ROMs as supplied by Intel. One section of the iSBC 86/12A on-board memory and MULTIBUS address decode PROMs (the same decode PROMs mentioned for the iSBC 300 module) is already preprogrammed to support the iSBC 340 module with Intel® 2732 EPROMs. This section is selected through the EPROM configuration switches on the iSBC 86/12A board. The iSBC 340 board can optionally be configured by the user to support Intel® 2758 or 2716 EPROMs or 2316E ROMs by programming new iSBC 86/12A decode PROMs to support these devices. Necessary documentation and PROM map listings are in the iSBC 86/12A Harware Reference Manual (order number 9803074-01).

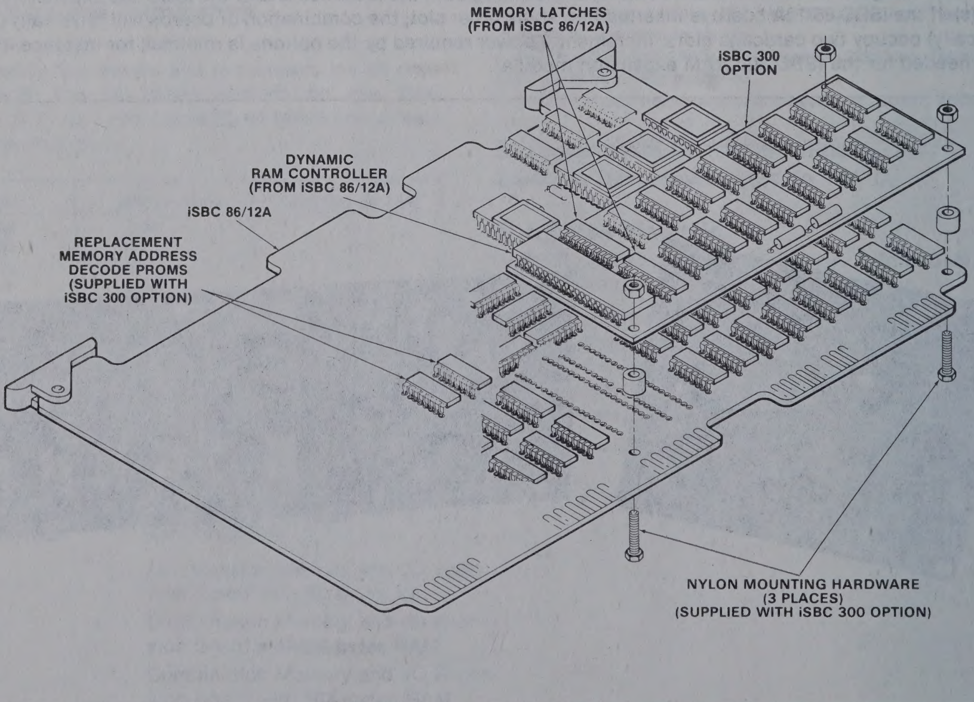

MEMORY LATCHES (FROM iSBC 86/12A)
iSBC 300 OPTION
DYNAMIC RAM CONTROLLER (FROM iSBC 86/12A)
iSBC 86/12A
REPLACEMENT MEMORY ADDRESS DECODE PROMS (SUPPLIED WITH iSBC 300 OPTION)
NYLON MOUNTING HARDWARE (3 PLACES) (SUPPLIED WITH iSBC 300 OPTION)

Figure 1. Installation of iSBC 300 RAM Expansion Module on iSBC 86/12A Single Board Computer

SPECIFICATIONS

Word Size

8 or 16 bits (16-bit data paths)

Memory Size

iSBC 300 Module — 32,768 bytes of RAM
iSBC 340 Module — 16,384 bytes (max) of EPROM/ROM

Access Time

iSBC 300 Module — Read: 1 μsec, write: 1.2 μsec
iSBC 340 Module — Standard EPROMs (450 nsec): 1 μsec, fast EPROMs (350 or 390 nsec): 800 nsec

Interface

The interface for the iSBC 300 and iSBC 340 module options is designed only for Intel's iSBC 86/12A Single Board Computer.

Memory Addressing

On-board RAM

CPU Access

iSBC 86/12A board only (32K bytes) — 00000-07FFFH.

iSBC 86/12A board + iSBC 300 module (64K bytes) — 00000-0FFFFH.

MULTIBUS Access — Jumper selectable for any 8K-byte boundary, but not crossing a 128K-byte boundary.

On-board EPROM/ROM

iSBC 86/12A board only (16K-bytes max.) — FF000-FFFFFH (using 2758 EPROMs); FE000-FFFFFH (using 2316E ROMs or 2716 EPROMs); and FC000-FFFFFH (using 2332A ROMs or 2732 EPROMs).

iSBC 86/12A board + iSBC 340 module (32K-bytes max.) — FE000-FFFFFH (using 2758 EPROMs); FC000-FFFFFH (using 2316E ROMs or 2716 EPROMs); F8000-FFFFFH (using 2332A ROMs or 2732 EPROMs).

On-board EPROM/ROM is not accessible via the MULTIBUS interface.

Auxiliary Power/Memory Protection

The low power memory protection option included on the iSBC 86/12A boards supports the iSBC 300 RAM module.

"Local Only" Memory Protection

The iSBC 86/12A Single Board Computer supports dedication of on-board RAM for on-board CPU access only in 8K, 16K, 24K, or 32K-byte segements. Installation of the iSBC 300 option allows protection of 16K, 32K, 48K, or 64K-byte segments.

Physical Characteristics

	iSBC 300	iSBC 340
Width	5.75″	3.3″
Length	2.35″	2.8″
Height of iSBC 86/12A plus mounted option	.718	.718*
Weight	13 oz.	5 oz.

*Includes EPROM/ROM's

All necessary mounting hardware (nylon, screws, spacers, nuts) are supplied with each kit.

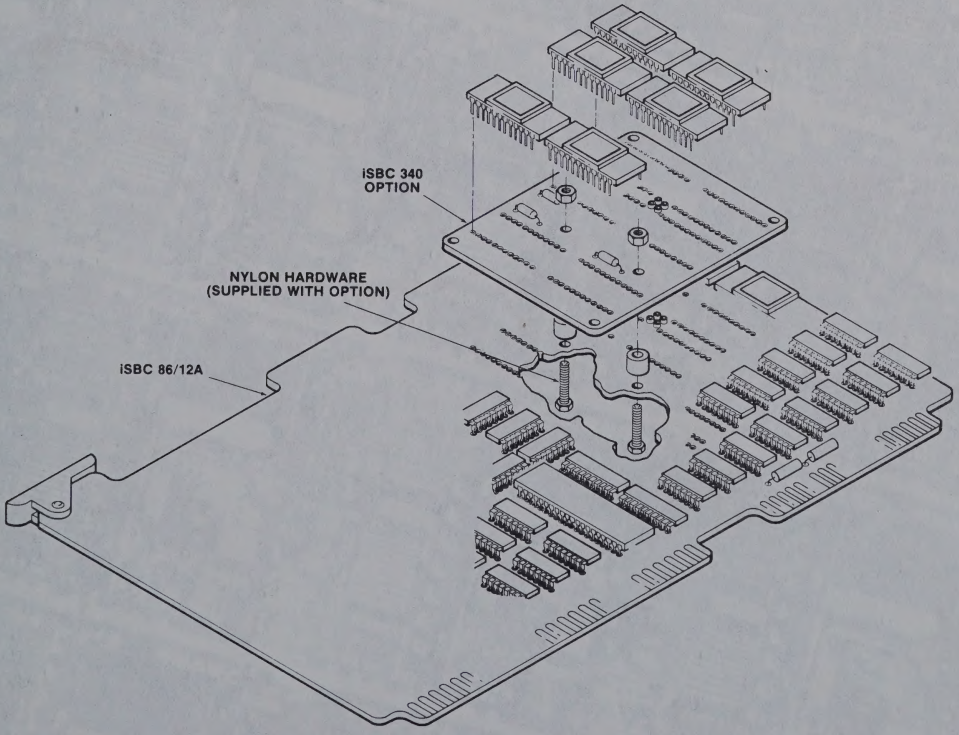


Figure 2. Installation of iSBC 340 EPROM/ROM Option on iSBC 86/12A Single Board Computer

Electrical Characteristics

DC power requirements:

Voltage	iSBC 300	iSBC 340
+5 ±5%	1 mA	120 mA[1]
+12 ±5%	24 mA	—
-12 ±5%	1 mA	—

Note:

1. Loaded with Intel 2732 EPROMs.

Environmental Characteristics

Operating Temperature — 0° to +55°C
Relative Humidity — to 90% (without condensation)

Reference Manuals

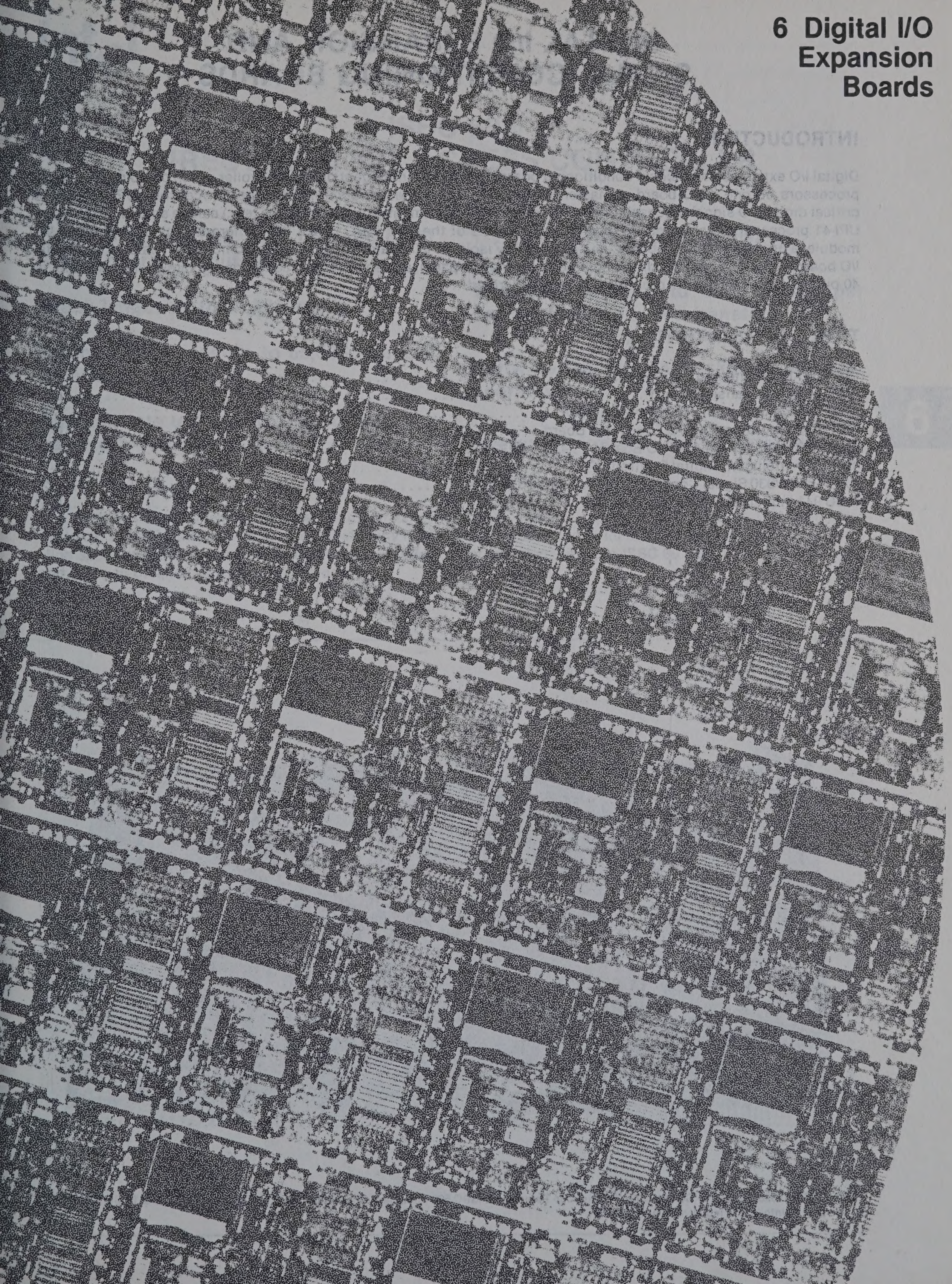
All necessary documentation for the iSBC 300 module and iSBC 340 module is included in the iSBC 86/12A Hardware Reference Manual; order #9803074-01. (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
SBC 300	32K-byte RAM Expansion Module
SBC 340	16K-byte EPROM Expansion Module

6 Digital I/O Expansion Boards



DIGITAL I/O EXPANSION AND SIGNAL CONDITIONING BOARDS

INTRODUCTION

Digital I/O expansion and signal conditioning boards include an intelligent digital controller which combines four 8-bit processors on one iSBC board, a master 8085A and up to three universal input/output processors (UPI-41s). Time critical digital I/O signal processing tasks (frequency measurement, pulse waveforms, etc.) can be shared by the slave UPI-41 processors, increasing the overall performance of the 8-bit iSBC board. Also, there is a general purpose I/O module, a programmable I/O board, and an optically isolated I/O board. There is also a combination parallel and serial I/O board, a digital signal conditioning/screw termination panel, and an AC signal conditioning/screw terminal panel. A 40-pin industrial digital I/O processor is also described.

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iSBC 569 Intelligent Digital Controller** 6-18
iCS 910/920/930 Signal Conditioning/Termination Panels** 6-23
iSBC 941 Industrial Digital Controller** 6-31

**The iCS 910/920/930 Signal Conditioning/Termination Panels, and iSBC 569 Intelligent Digital Controller and iSBC 941 Industrial Digital Controller are part of Intel's iCS Industrial Control Series.

iSBC 501
DIRECT MEMORY ACCESS CONTROLLER

Directly compatible with Intel iSBC 80 single board computers

Block length up to 65,536 words

Directly addresses up to 65,536 memory locations

Transfer rate up to 1 million words per second for block transfers

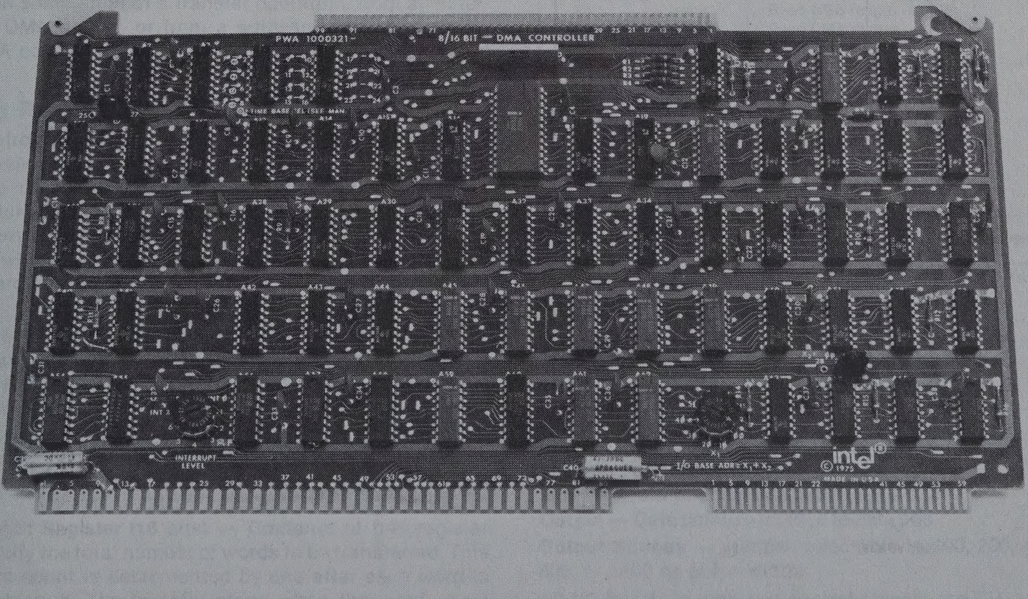
Transfers initialized via software

Transfers data up to 330K words per second for interleaved transfers

Software selectable/maskable interrupt operations

Interrupt priority switch selectable

The iSBC 501 Direct Memory Access Controller is a member of Intel's complete line of iSBC 80 OEM computer systems. The iSBC 501 interfaces directly with any iSBC 80 single board computer based system via the system bus. High speed, direct memory access control and interfacing for transfers between iSBC 80 expansion board memory and up to 16 peripheral devices is provided.



FUNCTIONAL DESCRIPTION

Transfer Capability

Block lengths up to 65,536 bytes long may be transferred directly to or from RAM memory in iSBC 80 systems at rates up to 1 million words per second. The iSBC 501 16-bit addressing capability allows transfers to take place at any location within memory. It is designed to control the direct transfer of data to or from Intel iSBC 80 memory expansion or combination memory and I/O boards. Two transfer modes of operation are included. System software is used to select the desired mode. Transfer rates up to 330K words per second may be achieved in the shared bus mode, wherein the iSBC 501 requests access to the system bus for 600 ns to perform a transfer of one word to or from memory. The second mode, the override mode, establishes the DMA controller as the only master which may access the system bus during the transfer period, thereby providing rapid block transfer capability. This mode provides transfer rates up to 1 million words per second. The iSBC 80/10A single board computer may only interact with the iSBC 501 in the shared bus mode. Either mode may be used with the other iSBC single board computers. Four timing strobes are provided for the control of data input transfers and four timing strobes are provided for output transfer operations. Strobes are initiated and selected via system software, and strobe pulses are jumper selectable to 100, 200, 400, 800, or 1600 ns widths.

Interrupt Requests

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selected DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Peripheral Interface

A 4-bit tag register is provided which may be used as a device select port to provide selection for four (up to 16 with external decoding) high speed peripheral devices interfacing through the iSBC 501.

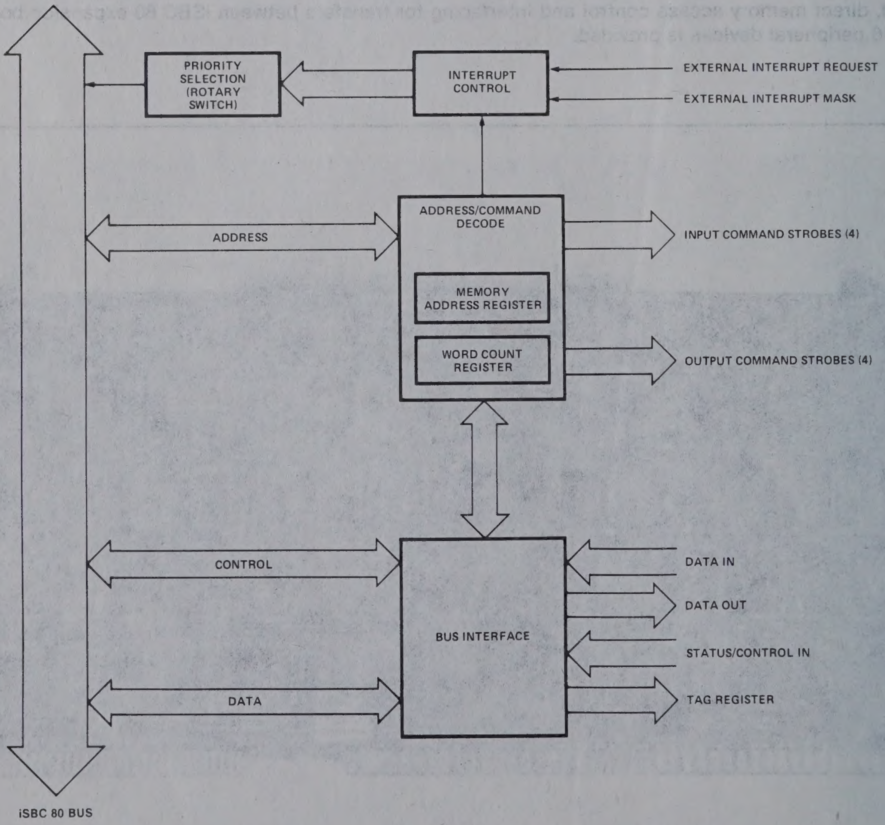

PRIORITY SELECTION (ROTARY SWITCH)
INTERRUPT CONTROL
EXTERNAL INTERRUPT REQUEST
EXTERNAL INTERRUPT MASK
ADDRESS
ADDRESS/COMMAND DECODE
INPUT COMMAND STROBES (4)
MEMORY ADDRESS REGISTER
WORD COUNT REGISTER
OUTPUT COMMAND STROBES (4)
CONTROL
BUS INTERFACE
DATA IN
DATA OUT
STATUS/CONTROL IN
TAG REGISTER
DATA
iSBC 80 BUS

Figure 1. iSBC 501 DMA Controller Block Diagram

SPECIFICATIONS

Word Size

8 bits

Block Size

65,536 words, max

Address Capability

65,536 words

Transfer Rates

Mode	Transfer Rates (K bytes/sec)[1]			
	Memory Read Operations		Memory Write Operations	
	Typical	Worst Case[3]	Typical	Worst Case[3]
Shared bus, CPU halted[2]	330	270	330	270
Shared bus, CPU executing code[2]	180	160	180	160
Override	1000	660	1000	660

Notes

1. Transfer rates given are to and from RAM memory on iSBC 104 or iSBc 108 combination memory and I/O boards.
2. Shared bus mode may be used with Intel iSBC 80/10 or Intel iSBC 80/20. iSBC 80/20 may also operate in override mode.
3. Assumes every DMA transfer must wait for RAM refresh cycle to be completed, worst case memory cycle times.

Interrupts

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selectable DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Key Registers

Control Register (6 bits) — The contents of the control register specify the busy status of the DMA board, the type of operation to be performed (transfer or non-transfer), the transfer direction (to or from memory), the interrupt condition (enabled or disabled), and the means by which the DMA board is using the system bus (shared mode or override mode).

Memory Address Register (16 bits) — Contains the address of the next memory location to be accessed by the iSBC 501. Loaded from the CPU, prior to a transfer operation, with the address of the first memory location to be accessed. The address is gated onto the system address bus during each transfer, and incremented by one for each word transferred.

Length Register (16 bits) — Contents of this register specify the total number of words to be transferred. This word count is decremented by one after each word is transferred. The transfer stops when the word count equals zero.

Tag Register (4 bits) — The contents of the tag register are used as control/select lines to the external peripheral devices being interfaced by the iSBC 501 (e.g., as the "go" command line to each of four devices), or the tag register outputs may be used with external decoding to expand the maximum number of DMA peripherals to 16.

Status Register (8-bits) — Provides 4 bits of DMA controller status: software interrupt, memory read/write operation requested, external/end-of-transfer interrupt, and DMA controller busy. The status register also provides four status/control bits directly from user peripheral devices.

Address Selection

iSBC 501 registers are located in a jumber selectable block starting at any 16-word boundary in the I/O address space.

Register Locations

Address[1]	I/O Operation	Function
X0	Output	Output strobe 0
X1	Output	Output strobe 1
X2	Output	Output strobe 2
X3	Output	Output strobe 3
X4	Output	Output tag strobe
X8	Output	Set interrupt
X9	Output	Reset interrupt
XA	Output	Load control register
XB	Output	Load tag register
XC	Output	Load LSB length register
XD	Output	Load MSB length register
XE	Output	Load LSB memory address register
XF	Output	Load MSB memory address register
X0	Input	Input command strobe 0
X1	Input	Input command strobe 1
X2	Input	Input command strobe 2
X3	Input	Input command strobe 3
X4	Input	Read LSB length register
X5	Input	Read MSB length register
X6	Input	Read DMA status
X7	Input	Invalid command

Note

1. X is any hex digit, assigned by jumbers.

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
I/O	100	0.100	Intel MDS 990 Viking 3VH50/1JN5

Interface Characteristics

I/O Line Driver Sink Current — 48 mA

I/O Line Terminator Load — 150Ω pullup

Input — Data positive relative to data bus

Output — Data positive relative to data bus

Output Strobes — Jumper selectable to 100, 200, 400, 800, or 1600 ns pulse widths.

All I/O interface data and control signals are TTL compatible and iSBC 80 bus compatible.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

$V_{CC} = 5V \pm 5\%$

$I_{CC} = 3.35A$ max; 2.70A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Equipment Supplied

iSBC 501 DMA Controller Board

Reference Manuals

9800294A — iSBC 501 Hardware Reference Manual (NOT SUPPLIED)

iSBC 501 Schematic (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 501	Direct Memory Access Controller

iSBC 508
I/O EXPANSION BOARD

iSBC-80 I/O expansion via direct bus interface

Four 8-bit terminated input ports

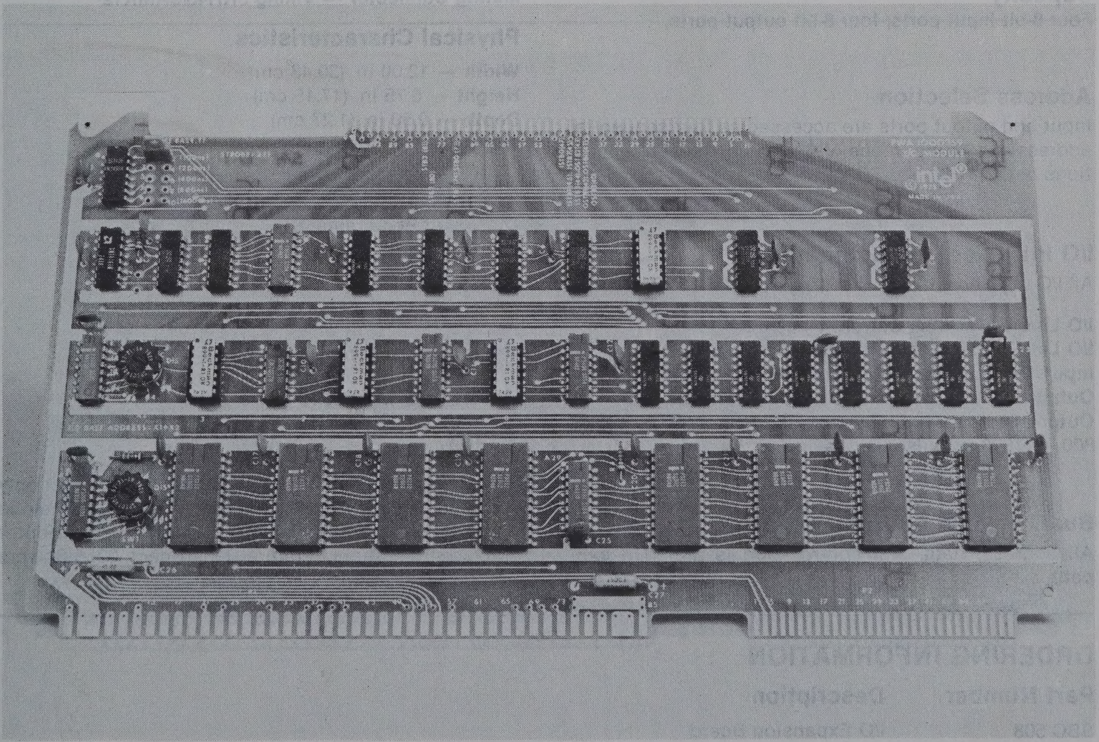
Four 8-bit output ports with buffered TTL drivers

Selectable latched or unlatched input ports

Latched outputs with selectable width strobes

Switch selectable I/O port addresses

The iSBC-508 I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 508 interfaces directly to any iSBC 80 single board computer via the system bus to expand input and output port capacity. Four 8-bit terminated input ports are contained on the board. Data is gated into the port while the strobe is present and latched if the strobe is removed. The iSBC 508 contains four 8-bit output ports. All output lines are driven by TTL level buffer drivers residing on the board. Output data is latched. A strobe signal of jumper selectable width is sent to the peripheral device during an output operation. Address selection is accomplished using two resident rotary switches to select one of 64 unique base addresses for all input and output ports. The board operates with a single +5V power supply.



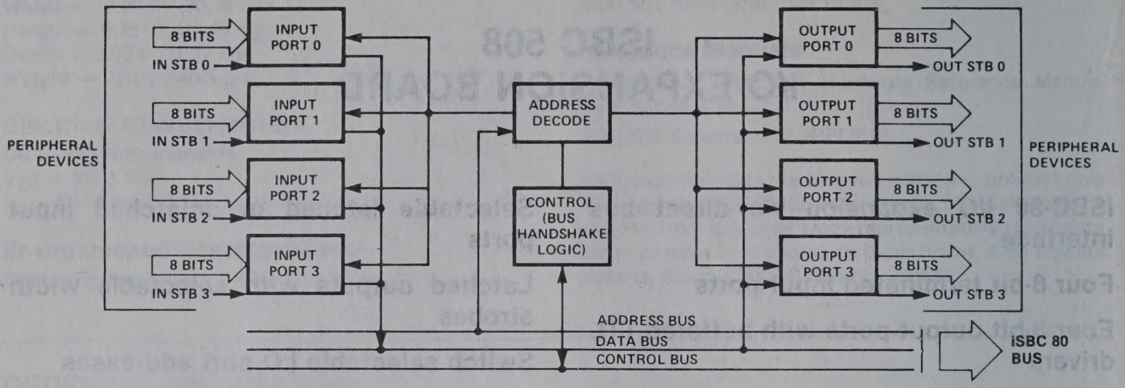

PERIPHERAL DEVICES
8 BITS
IN STB 0
INPUT PORT 0
8 BITS
IN STB 1
INPUT PORT 1
8 BITS
IN STB 2
INPUT PORT 2
8 BITS
IN STB 3
INPUT PORT 3
ADDRESS DECODE
CONTROL (BUS HANDSHAKE LOGIC)
OUTPUT PORT 0
8 BITS
OUT STB 0
OUTPUT PORT 1
8 BITS
OUT STB 1
OUTPUT PORT 2
8 BITS
OUT STB 2
OUTPUT PORT 3
8 BITS
OUT STB 3
PERIPHERAL DEVICES
ADDRESS BUS
DATA BUS
CONTROL BUS
iSBC 80 BUS

Figure 1. iSBC 508 I/O Expansion Board Block Diagram

SPECIFICATIONS

Word Size
8 bits

Capacity
Four 8-bit input ports; four 8-bit output ports.

Address Selection
Input and output ports are accessed as four sequential addresses starting in one of 64 switch selectable locations between 00 and FC_{16}.

I/O Interface Characteristics
All I/O interface data and control signals are TTL levels.

I/O Line Driver Sink Current — 48 mA
I/O Line Terminator Load — 1 kΩ pullup
Inputs — Data positive relative to data bus
Outputs — Data positive relative to data bus
Output Strobe — Jumper selectable to 100, 200, 400, 800, or 1600-ns pulse widths

Bus Interface Characteristics
All address, data, and control signals are TTL compatible.

Connectors
Bus Edge Connector — 86-pin double-sized PC edge connector with 0.156-in. contact centers
Mating Connector — Control Data VPB01E43A00A1

I/O Edge Connector — 100-pin double-sided PC edge connector with 0.1 in. contact centers
Mating Connector — Viking 3KH43/9AMK12

Physical Characteristics
Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (415.2 gm)

Electrical Characteristics
DC Power Requirements
$V_{CC} = +5V \pm 5\%$
$I_{CC} = 2.6A$ max, 1.9A typ

Environmental Characteristics
Operating Temperature — 0°C to 55°C

Reference Manuals
9800278 — iSBC 508 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 508	I/O Expansion Board

iSBC 517
COMBINATION I/O EXPANSION BOARD

I/O addressing and connectors directly compatible with iSBC 104, iSBC 108, and iSBC 116 combination boards

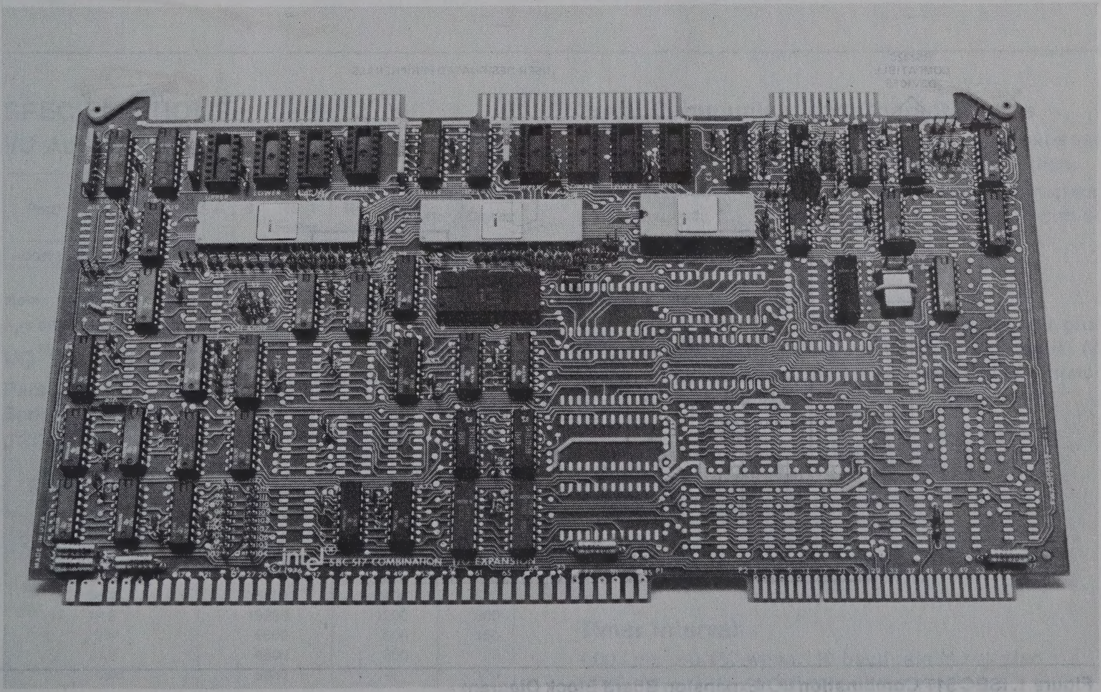
48 programmable I/O lines with sockets for interchangeable line drivers and terminators

Synchronous/asynchronous communications interface with RS232C drivers and receivers

Eight maskable interrupt request lines with a pending interrupt register

1 ms interval timer

The iSBC 517 Combination I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The board interfaces directly with any iSBC 80 single board computer via the system bus to expand serial and parallel I/O capacity. The combination I/O board contains 48 programmable parallel I/O lines. The system software is used to configure the I/O lines to meet a wide variety of system peripheral requirements. The flexibility of the I/O interface is significantly enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. A programmable RS232C communications interface is provided on the iSBC 517. This interface may be programmed by the system software to provide virtually any asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). A comprehensive RS232C interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems is thus on the board. An on-board register contains the status of eight interrupt request lines which may be interrogated from the system bus, and each interrupt request line is maskable under program control. The iSBC 517 also contains a jumper selectable 1 ms interval timer and interface logic for eight interrupt request lines.



FUNCTIONAL DESCRIPTION

Programming Flexibility

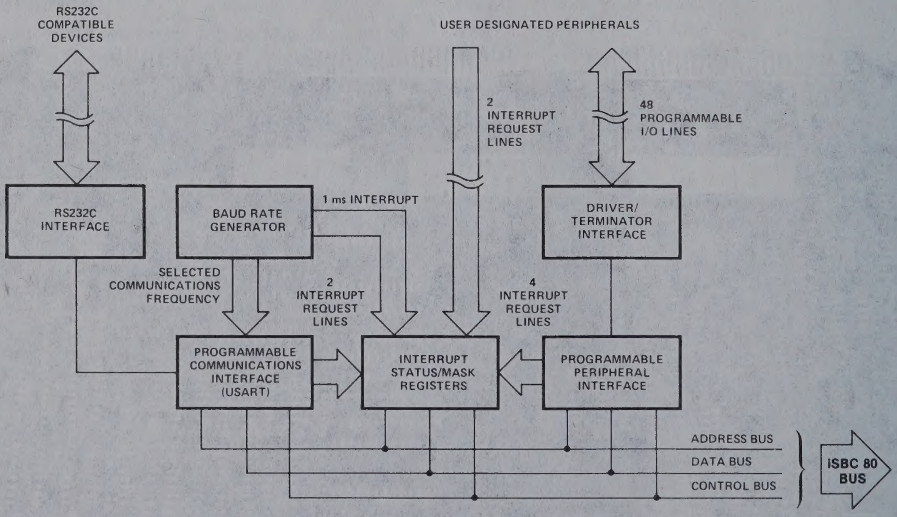
The 48 programmable I/O lines on the iSBC 517 are implemented utilizing two Intel 8255 programmable peripheral interfaces. The system software is used to configure these programmable I/O lines in any of the combinations of unidirectional input/output, and bidirectional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable. Typical I/O read access time is 280 nanoseconds. Typical I/O read cycle time is 600 nanoseconds.

Communications Interface

The programmable communications interface on the iSBC 517 is provided by an Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability, and parity, overrun, and framing error detection are all incorporated in the USART. The comprehensive RS232C interface on the board provides a direct interface to RS232C compatible equipment. The RS232C serial data lines and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 517 Combination I/O Expansion Board to teletypewriters and other 20 mA current loop equipment.

Interrupt Request Lines

Interrupt requests may originate from eight sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is


RS232C
COMPATIBLE
DEVICES
USER DESIGNATED PERIPHERALS
2
INTERRUPT
REQUEST
LINES
48
PROGRAMMABLE
I/O LINES
RS232C
INTERFACE
BAUD RATE
GENERATOR
1 ms INTERRUPT
DRIVER/
TERMINATOR
INTERFACE
SELECTED
COMMUNICATIONS
FREQUENCY
2
INTERRUPT
REQUEST
LINES
4
INTERRUPT
REQUEST
LINES
PROGRAMMABLE
COMMUNICATIONS
INTERFACE
(USART)
INTERRUPT
STATUS/MASK
REGISTERS
PROGRAMMABLE
PERIPHERAL
INTERFACE
ADDRESS BUS
DATA BUS
CONTROL BUS
iSBC 80
BUS

NOTES: INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER-SELECTABLE.

Figure 1. iSBC 517 Combination I/O Expansion Board Block Diagram

Ports	Lines (qty)	Mode of Operation					
		Unidirectional					
		Input		Output		Bidirectional	Control
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X^1
	4	X		X			X^1
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X^2
	4	X		X			X^2

Notes

1. Part of port 3 must be used as control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

maskable under program control. Routing for the eight interrupt request lines is jumper selectable. They may be ORed to provide a single interrupt request line for the iSBC 80/10A, or they may be individually provided to the system bus for use by the iSBC 80/20-4 priority interrupt controller.

Interval Timer

Each board contains a jumper selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

SPECIFICATIONS

I/O Addressing

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note

X is any hex digit assigned by jumper selection.

I/O Transfer Rate

Parallel — Read or write cycle time 760 ns max

Serial — (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; peak characters generation; 1, 1½, or 2 stop bits; false start bit detectors.

Interrupts

Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines), or user specified devices via the I/O edge connector (2 lines) or interval timer.

Interrupt Register Address

X1	Interrupt mask register
X0	Interrupt status register

Note

X is any hex digit assigned by jumber selection.

Timer Interval

1.003 ms ±0.1% when 110 baud rate is selected

1.042 ms ±0.1% for all other baud rates

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — RS232C
Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary[1]	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or system packaging. Auxiliary connector is used for test purposes only.

Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 517:

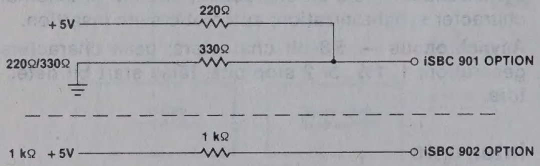
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open-collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Commands	Tri-state	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (397. 3 gm)

Electrical Characteristics

Average DC Current

$V_{CC} = +5V \pm 5\%$
$V_{DD} = +12V \pm 5\%$
$V_{AA} = -12V \pm 5\%$
$I_{CC} = 2.4$ mA max
$I_{DD} = 40$ mA max
$I_{AA} = 60$ mA max

Note

Does not include power required for optional I/O drivers and I/O terminators. With eight 220Ω/330Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800388B — iSBC 517 hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

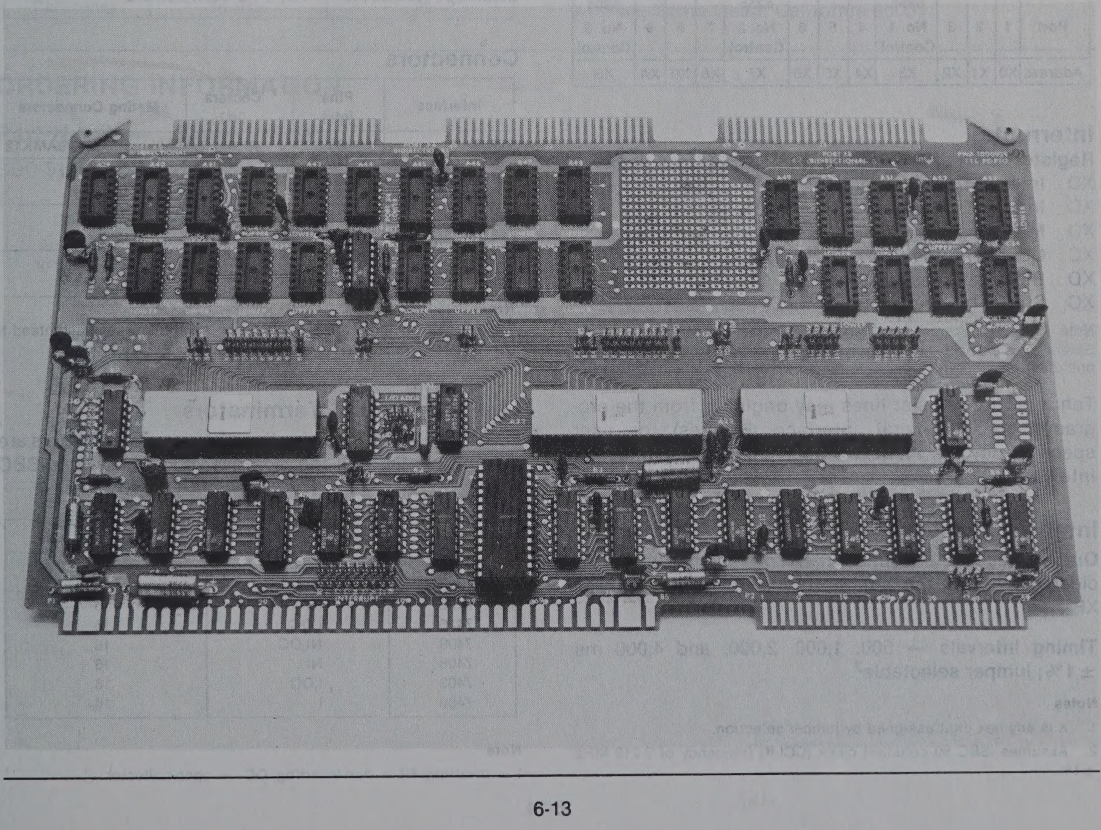
ORDERING INFORMATION

Part Number	Description
SBC 517	Combination I/O Expansion Board

iSBC 519 PROGRAMMABLE I/O EXPANSION BOARD

- **iSBC 80 I/O expansion via direct bus interface**
- **72 programmable I/O lines with sockets for interchangeable line drivers and terminators**
- **Jumper selectable I/O port addresses**
- **Jumper selectable 0.5, 1.0, 2.0, or 4.0 ms interval timer**
- **Eight maskable interrupt request lines with priority encoded and programmable interrupt algorithms**

The iSBC 519 Programmable I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 519 interfaces directly to any iSBC 80 single board computer via the system bus to expand input and output port capacity. The iSBC 519 provides 72 programmable I/O lines. The system software is used to configure the I/O lines to meet a wide variety of peripheral requirements. The flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. Address selection is accomplished by using wire-wrap jumbers to select one of 16 unique base addresses for the input and output ports. The board operates with a single +5V power supply.



Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels are based in sequence numerically on this assignment.

Table 2. Interrupt Priority Options

manner in which requests are serviced may be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel I/O interfaces, the interval timer, or direct from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the system master. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the interrupt mask register of the PIC.

Interrupt Request Generation — Interrupt requests may originate from 10 sources. Six jumper selectable interrupt requests can be automatically generated by the programmable peripheral interfaces when a byte of information is ready to be transferred to the system master (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Three interrupt request lines may be interfaced to the PIC directly from user designated peripheral devices via the I/O edge connectors. One interrupt request may be generated by the interval timer.

Bus Line Drivers — The PIC interrupt request output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus. Any of the on-board request lines may also drive any iSBC 80 bus interrupt line directly via jumpers and buffers on the board.

SPECIFICATIONS

Addressing

Port	1	2	3	8255 No. 1 Control	4	5	6	8255 No. 2 Control	7	8	9	8255 No. 3 Control
Address	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	XA	XB

Interrupts

Register Addresses (hex notation, I/O address space)

XD	Interrupt request register
XC	In-service register
XD	Mask register
XC	Command register
XD	Block address register
XC	Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Ten interrupt request lines may originate from the programmable peripheral interface (6 lines), or user specified devices via the I/O edge connector (3 lines), or interval timer (1 line).

Interval Timer

Output Register — Timer interrupt register output is cleared by an output instruction to I/O address XE or XF[1].

Timing Intervals — 500, 1,000, 2,000, and 4,000 ms ± 1%; jumper selectable[2].

Notes

1. X is any hex digit assigned by jumper selection.
2. Assumes iSBC 80 constant clock (CCLK) frequency of 9.216 MHz ± 1%.

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary[1]	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector heights and wirewrap pin lengths are not guaranteed to conform to Intel OEM or System packaging.

Line Drivers and Terminators

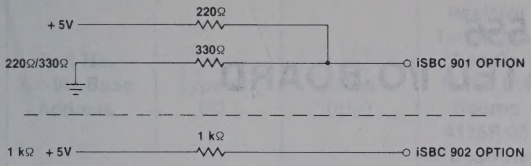
I/O Drivers — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 519:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open-collector.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup



Ports 1, 4, and 7 may use any of the drivers or terminators shown above for unidirectional (input or output) port configurations. Either terminator and the following bidirectional drivers and terminators may be used for ports 1, 4, and 7 when these ports are used as bidirectional ports.

Bidirectional Drivers

Driver	Characteristic	Sink Current (mA)
Intel 8216	NI, TS	25
Intel 8226	I, TS	50

Note

I = inverting; NI = non-inverting; TS = three-state.

Terminators (for ports 1, 4, and 7 when used as bidirectional ports)

Supplier	Product Series
CTS	760-
Dale	LDP14k-02
Beckman	899-1

Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Commands	Tri-state	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (397.3 gm)

Electrical Characteristics

Average DC Current

Voltage	Without Termination[1]	With Termination[2]
$V_{CC} = +5V \pm 5\%$	$I_{CC} = 1.5A$ max	3.5A max

Note

1. Does not include power required for optional I/O drivers and I/O terminators.
2. With 18 220Ω/330Ω Input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800385B — iSBC 519 hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 519	Programmable I/O Expansion Board

iSBC 556
OPTICALLY ISOLATED I/O BOARD

iSBC 80 and MULTIBUS compatible

Up to 48 digital optically isolated input/output data lines

Choice of
- **24 fixed input lines**
- **16 fixed output lines**
- **8 programmable lines**

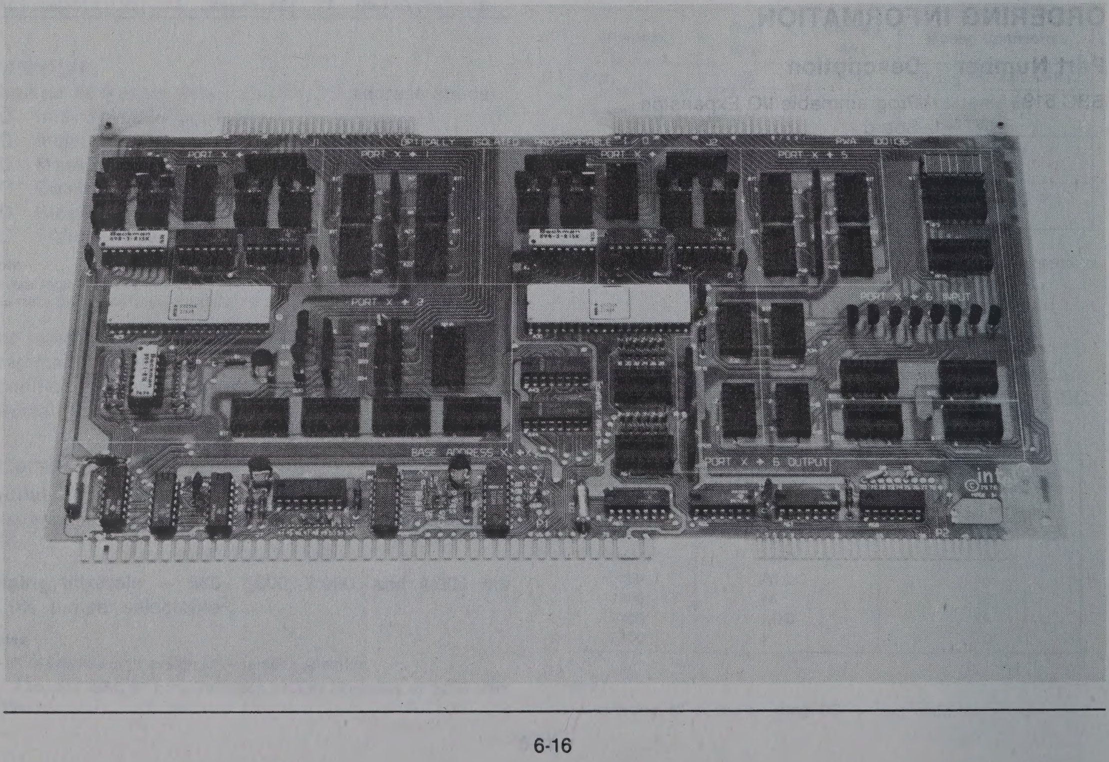
Provisions for plug-in, optically isolated receivers, drivers, and terminators

Voltage/current levels
- **Input up to 48V**
- **Output up to 30V, 60 mA**

Common interrupt for up to 8 sources

+5V supply only

The iSBC 556 Optically Isolated I/O Board provides 48 digital input/output lines with isolation between process application or peripheral device and the iSBC 80 series single board computers. The iSBC 556 contains two 8255A programmable interface devices, and sockets for user supplied optically isolated drivers, receivers, and input resistor terminators, together with common interrupt logic and iSBC 80 bus interface logic. Input signals can be single-ended or differential types with user defined input range (resistor terminator and opto-isolated receiver selection), allowing flexibility in design of voltage and threshold levels. The output allows user selection of Opto-Isolated Darlington Pair which can be used as an output driver either as an open collector or current switch.



Port No. X = I/O Base Address	Type of I/O	Lines (qty)	Resistor Terminator Pac Rp 16-Pin DIP Bourns 4116R-00 or Equivalent	Dual Opto-Isolator 8-Pin Dip Monsanto MC T66 or Equivalent	Dual Opto-Isolator Darlington Pair 6-Pin DIP Monsanto 4N29, 30 31, 32 or Equivalent	Driver 7438 or Equivalent	Pull-Up iSBC 902
X + 0	Input	8	1	4	—	—	
X + 1	Output	8	—		8	—	
X + 2	Input/ Control	8	1		8	—	
X + 4	Input	8	1	4	—	—	
X + 5	Output	8			8	—	
X + 6 X + 7	Input/ Output Control	8	1 if input		8	2 if output	2 if input

Table 1. I/O Ports Opto-Isolator Receivers, Drivers, And Terminators

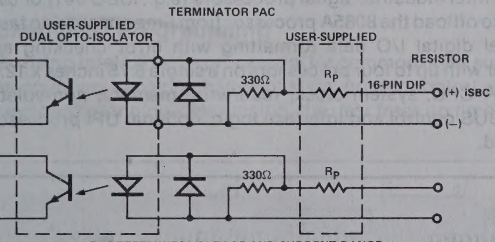
SPECIFICATIONS

Number of Lines

24 input lines
16 output lines
8 programmable lines: 4 input — 4 output

I/O Interface Characteristics

Line-to-Line Isolation — 235V DC or peak AC
Input/Output Isolation — 500V DC or peak AC



R_P DETERMINES VOLTAGE AND CURRENT RANGE.

Bus Interface Characteristics

All data address and control commands are iSBC 80 bus compatible.

I/O Addressing

Port	8255 #1			Control	8255 #2			Control
	A	B	C		A	B	C	
Address	X + 0	X + 1	X + 2	X + 3	X + 4	X + 5	X + 6	X + 7

Where:
base address is from 00H to 1FH (jumper selectable)

ORDERING INFORMATION

Part Number	Description
SBC 556	Optically Isolated I/O Board

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		in.	cm	
P1 iSBC bus	86	0.156		Viking 3KH43/9AMK12
J1 16 fixed input & 8 fixed output lines	50	0.1		3M 3415-000 or TI M312125
J2 8 fixed output, 8 fixed output, & 8 programmable input/output lines	50	0.1		3M 3415-000 or TI M312125

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (397.3 gm)

Electrical Characteristics

Average DC Current

$V_{CC} = +5V \pm 5\%$, 1.0A without user supplied isolated receiver/driver

$I_{CC} = 1.6A$ max with user supplied isolator receiver/driver

Environmental Characteristics

Temperature — 0°C to 55°C
Relative Humidity — 0 to 90%, non-condensing

Reference Manual

9800489-02 — iSBC 556 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

iSBC 569
INTELLIGENT DIGITAL CONTROLLER

Single board digital I/O controller with up to four microprocessors to share the digital input/output signal processing

3 MHz 8085A central control processor

Three sockets for 8041A/8741A Universal Peripheral Interface (UPI-41A) for distributed digital I/O processing such as:
- **Industrial signal processor (iSBC 941)**
- **Custom programmed 8041A/8741A**

Three operational modes
- **Stand alone digital controller**
- **MULTIBUS master**
- **Intelligent slave (slave to MULTIBUS master)**

2K bytes of dual port static read/write memory

Sockets for up to 8K bytes of Intel 2758, 2716, 2732 erasable programmable read only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers or terminators

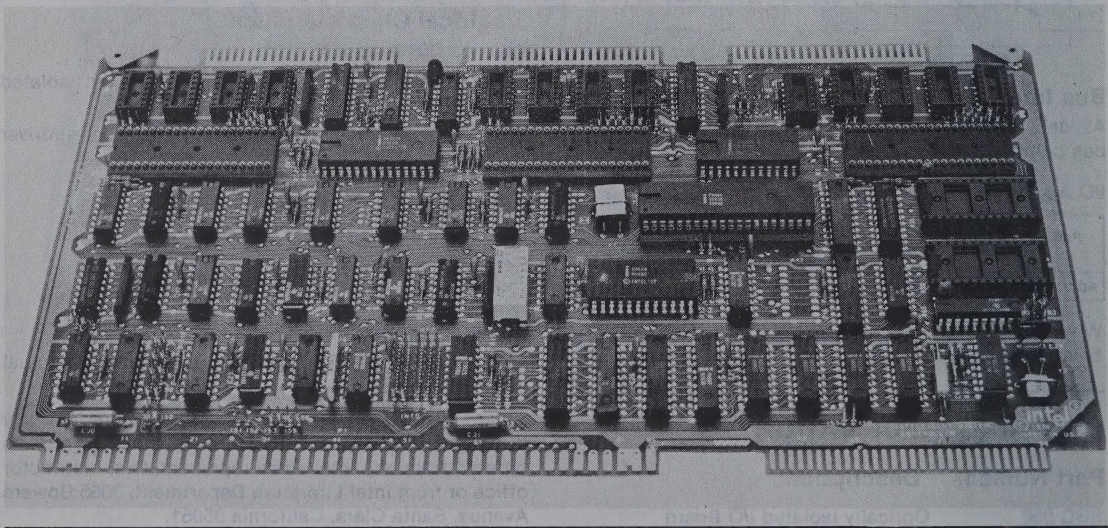
Three programmable counters

12 levels of programmable interrupt control

Single +5 Volt supply

MULTIBUS standard control logic compatible with optional iSBC 80 and iSBC 86 CPU, memory, and I/O expansion boards

The Intel iSBC 569 Intelligent Digital Controller is a single board computer (8085A based) with sockets for three 8041A/8741A Universal Peripheral Interface chips (UPI-41A). The I/O processing algorithm may be tailored to application requirements using designer selected combinations of standard Intel industrial signal processors (e.g., iSBC 941) or user programmed UPI-41A processors. These devices may be used to offload the 8085A processor from time consuming tasks such as pulse counting, event sensing, and parallel or serial digital I/O data formatting with error checking and handshaking. The iSBC 569 board is a complete digital controller with up to four processors on a single 6.75 inches x 12.00 inches (17.15cm x 30.48cm) printed circuit board. The 8085A CPU, system clock, read/write memory, non-volatile memory, priority interrupt logic, programmable timers, MULTIBUS control and interface logic, optional UPI processors and optional line driver and terminators all reside on one board.



FUNCTIONAL DESCRIPTION

Intelligent Digital Controller

Three modes of operation — the iSBC 569 Intelligent Digital Controller is capable of operating in one of three modes; stand alone controller, bus master, or intelligent slave.

Stand alone controller — the iSBC 569 board may function as a stand alone, single board controller with CPU, memory, and I/O elements on a single board. Five volt (+5VDC) only operation allows configuration of low cost controllers with only a single power supply voltage. The on-board 2K bytes RAM and up to 16K bytes ROM/EPROM, as well as the assistance of three UPI-41A processors, allow significant digital I/O control from a single board.

Bus master — in this mode of operation, the iSBC 569 controller may interface with and control iSBC expansion memory and I/O boards, or even other iSBC 569 Intelligent Digital Controllers configured as intelligent slaves (but no additional bus masters).

Intelligent slave — the iSBC 569 controller can perform as an intelligent slave to any 8- or 16-bit MULTIBUS master CPU by offloading the master of digital control related tasks. Preprocessing of data for the master is controlled by the on-board 8085A CPU which coordinates up to three UPI-41A processors. Using the iSBC 569 board as an intelligent slave, multi-channel digital control can be managed entirely on-board, freeing a system master to perform other system functions. The dual port RAM memory allows the iSBC 569 controller to process and store data without MULTIBUS memory contention.

Simplified Programming

By using Intel UPI-41A processors for common tasks such as counting, sensing change of state, printer control and keyboard scanning/debouncing, the user frees up time to work on the more important application programming of machine or process optimization. Controlling the Intel UPI-41A processors becomes a simple task of reading or writing command and data bytes to or from the data bus buffer register on the UPI device. Programming the iSBC 941 Industrial Digital Processor to produce a pulse output, for example, is as simple as sending command and parameter bytes indicating initialization, pulse output selection, period and delay parameters, followed by a command to begin execution.

Central Processing Unit

A powerful Intel 8085A 8-bit CPU, fabricated on a single LSI chip, is the central processor for the iSBC 569 ™ controller. The six general purpose 8-bit registers may be addressed individually or in pairs, providing both single and double precision operations. The program counter can address up to 64K bytes of memory using iSBC expansion boards. The 16-bit stack pointer controls the addressing of an external stack. This stack provides sub-routine nesting bounded only by memory size. The minimum instruction execution time is 1.30 microseconds. The 8085A CPU is software compatible with the Intel 8080A CPU.

Bus Structure

The iSBC 569 Intelligent Digital Controller utilizes a triple bus architecture concept. An internal bus is used for on-board memory and I/O operations. A MULTIBUS interface is available to provide access for all external memory and I/O operations. A dual port bus with controller enables access via the third bus to 2K bytes of static RAM from either the on-board CPU or a system master. Hence, common data may be stored in on-board memory and may be accessed either by the on-board CPU or by system masters. A block diagram of the iSBC 569 functional components is shown in Figure 1.

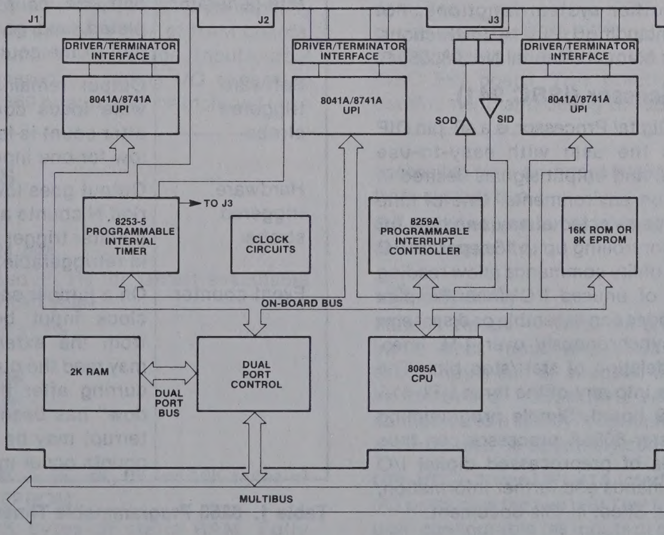


Figure 1. iSBC 569 Intelligent Digital Controller Block Diagram

RAM Capacity

The iSBC 569 board contains 2K bytes of read/write memory using Intel 2114 static RAMs. RAM accesses may occur from either the iSBC 569 controller or from any other bus master interfaced via the MULTIBUS system bus. The iSBC 569 board provides addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the system bus. In addition, a switch is provided which allows the user to reserve a 1K byte segment of on-board RAM for use by the 8085A CPU. This reserved RAM space is not accessible via the system bus and does not occupy any system address space.

EPROM/ROM Capacity

Two sockets for up to 16K bytes of nonvolatile read only memory are provided on the iSBC 569 board. Nonvolatile memory may be added in 1K-byte increments up to a maximum of 2K bytes using Intel 2758 erasable and electrically reprogrammable ROMs (EPROMs); in 2K-byte increments up to a maximum of 4K bytes using Intel 2316 ROMs or 2716 EPROMs; in 4K byte increments up to 8K bytes maximum using Intel 2732 EPROMs; or in 8K-byte increments up to 16K bytes maximum using Intel 2364 ROMs (both sockets must contain same type ROM/EPROM). All on-board ROM/EPROM operations are performed at maximum processor speed.

Universal Peripheral Interfaces (UPI-41A)

The iSBC 569 Intelligent Digital Controller board provides three sockets for user supplied Intel 8041A/8741A Universal Peripheral Interface (UPI-41A) chips. Sockets are also provided for the associated line drivers and terminators for the UPI I/O ports. The UPI-41A processor is a single chip microcomputer containing a CPU, 1K bytes of ROM (8041A) or EPROM (8741A), 64 bytes of RAM, 16 programmable I/O lines, and an 8-bit timer/event counter. Special interface registers included in the chip allow the UPI-41A processor to function as a slave processor to the iSBC 569 controller board's 8085A CPU. The UPI processor allows the user to specify algorithms for controlling peripherals directly thereby freeing the 8085A for other system functions. For additional information, including UPI-41A instructions, refer to the UPI-41 User's Manual (Manual No. 9800504).

Industrial Digital Processor (iSBC 941)

The iSBC 941 Industrial Digital Processor is a 40-pin DIP device which provides the user with easy-to-use processing of digital input and output signals desired in many industrial automation environments. One of nine digital I/O functions can be selected at any one time for measuring, counting, or controlling up to 16 separate I/O lines. An additional eight utility commands allow reading or setting the condition of unused I/O lines. Simplex serial input and output modes can assemble or disassemble bytes transmitted asynchronously over TTL lines, including insertion and deletion of start/stop bits. The iSBC 941 processor plugs into any of the three UPI-41A sockets on the iSBC 569 board. Simple programming commands from the master 8085A processor can thus implement up to 48 lines of preprocessed digital I/O signals. For specific commands and further information, refer to the iSBC 941 Data Sheet in this document.

Programmable Timers

The iSBC 569 Intelligent Digital Controller board provides three independently programmable interval timer/counters utilizing one Intel 8253 Programmable Interval Timer (PIT). The Intel 8253 PIT provides three 16-bit BCD or binary interval timer/counters. Each timer may be used to provide a time reference for each UPI™ processor or for a group of UPI processors. The output of each timer also connects to the 8259A Programmable Interrupt Controller (PIC) providing the capability of timed interrupts. All gate inputs, clock inputs, and timer outputs of the 8253 PIT are available at the I/O ports for external access.

Timer Functions — In utilizing the iSBC 569 controller, the systems designer simply configures, via software, each timer to meet systems requirements. The 8253 PIT modes are listed in Table 1. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications. The contents of each counter can be read "on-the-fly" for time stamping events or time clock referenced program initiations.

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N counts occur in the system.

Table 1. 8253 Programmable Timer Functions

Interrupt Capability

The iSBC 569 Intelligent Digital Controller provides interrupt service for up to 12 interrupt sources. Any of the 12 sources may interrupt the on-board processor. Four interrupt levels are handled directly by the 8085A CPU and eight levels are serviced from an Intel 8259A Programmable Interrupt Controller (PIC) routing an interrupt request output to the INTR input of the 8085A.

8085A Interrupt — Each of four direct 8085A interrupt inputs has a unique vector memory address. An 8085A jump instruction at each of these addresses then provides software linkage to interrupt service routines located independently anywhere in the memory.

8259A Interrupts — The eight interrupt sources originate from both on-board controller functions and the system bus:

UPI-41A Processors — one interrupt from each of three UPI processor sockets.

8253 PIT — one interrupt from each of three timer outputs.

MULTIBUS System Bus — one of eight MULTIBUS interrupt lines may be jumpered to either of two 8259A PIC interrupt inputs.

Programmable Reset — The iSBC 569 Intelligent Digital Controller board has a programmable output latch used to control on-board functions. Three of the outputs are connected to separate UPI-41A RESET inputs. Thus, the user can reset any or all of the UPI-41A processors under software control. A fourth latch output may be used to generate an interrupt request onto the MULTIBUS interrupt lines. A fifth latch output is connected to a light-emitting diode which may be used for diagnostic purposes.

Expansion Capabilities

When the iSBC 569 controller is used as a single board digital controller, memory and I/O capacity may be expanded using Intel MULTIBUS compatible expansion boards. In this mode, no other bus masters may be in the system. Memory may be expanded to a 64K byte capacity by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding I/O expansion boards. Multiple iSBC 569 boards may be included in an expanded system using one iSBC 569 Intelligent Digital Controller as the system master and additional controllers as intelligent slaves.

Intelligent Slave Programming

When used as an intelligent slave, the iSBC 569 controller appears as an additional RAM memory module. System bus masters communicate with the iSBC 569 board as if it were just an extension of system memory. To simplify this communication, the user has been given some specific tools:

Flag Interrupt — The Flag Interrupt is generated any time a write command is performed by an off-board CPU to the first location of iSBC 569 RAM. This interrupt provides a means for the master CPU to notify the iSBC 569 controller that it wished to establish a communications sequence. The flag interrupt is cleared when the on-board processor reads the first location of its RAM. In systems with more than one intelligent slave, the flag interrupt provides a unique interrupt to each slave outside the normal MULTIBUS interrupt lines (INT0/-INT7/).

RAM — The on-board 2K byte RAM area that is accessible to both an off-board CPU and the on-board 8085A may be configured for system access on any 2K boundary.

MULTIBUS Interrupts — The third tool to improve system operation as an intelligent slave is access to the MULTIBUS interrupt lines. The iSBC 569 controller can both respond to interrupt signals from an off-board CPU, and generate an interrupt to the off-board CPU via the system bus.

System Development Capability

Software development for the iSBC 569 Intelligent Digital Controller board is supported by the Intellec® Microcomputer Development System including a resident macroassembler, text editor, system monitor, a linker, object code locator, and Library Manager. In addition, both PL/M and FORTRAN language programs can be compiled to run on the iSBC 569 board. A unique in-circuit emulator (ICE-85™) option provides the capability of developing and debugging software directly on the iSBC 569 board. This greatly simplifies the design, development, and debug of iSBC 569 system software.

SPECIFICATIONS

8085A CPU

Word Size — 8, 16 or 24 bits

Cycle Time — 1.30 μsec ± .1% for fastest executable instruction; i.e., four clock cycles.

Clock Rate — 3.07 MHz ± .1%

System Access Time

Dual port memory — 725 nsec

Memory Capacity

On-board ROM/EPROM — 2K, 4K, 8K, or 16K bytes of user installed ROM or EPROM

On-board RAM — 2K bytes of static RAM. Fully accessible from on-board 8085A. Separately addressable from system bus.

Off-board expansion — up to 64K bytes of EPROM/ROM or RAM capacity.

I/O Capacity

Parallel-Timers — Three timers, with independent gate input, clock input, and timer output user-accessible. Clock inputs can be strapped to an external source or to an on-board 1.3824 MHz reference. Each timer is connected to a 8259A Programmable Interrupt Controller and may also be optionally connected to UPI processors.

UPI-I/O — Three UPI-41A interfaces, each with two 8-bit I/O ports plus the two UPI Test Inputs. The 8-bit ports are user-configurable (as inputs or outputs) in groups of four.

Serial — 1 TTL compatible serial channel utilizing SID and SOD lines of on-board 8085A CPU

On-Board Addressing

All communications to the UPI-41A processors, to the programmable reset latch, to the timers, and to the interrupt controller are via read and write commands from the on-board 8085A CPU.

Memory Addressing

On-board ROM/EPROM — 0–07FF (using 2758 EPROMs); 0–OFFF (using 2716 EPROMs or 2316 ROMs); 0–1FFF (using 2732 EPROMs); 0-3FFF (using the 2364 ROMs)

On-board RAM — 8000–87FF System access — any 2K increment 00000–FF800 (switch selectable); 1K bytes may be disabled from bus access by switch selection.

I/O Addressing

Source	Addresses
8253	0E0H–0E3H
UPI0	0E4H–0E5H
UPI1	0E6H–0E7H
UPI2	0E8H–0E9H
PROGRAMMABLE RESET	0EAH–0EBH
8259A	0ECH–0EDH

Timer Specifications

Input frequencies — jumper selectable reference

Internal: 1.3824 MHz ± .1% (.723 μsec, nominal)
External: User supplied (2 MHz maximum)

Output Frequencies (at 1.3824 MHz)

Function	Min[1]	Max[1]
Real-time interrupt interval	1.45 μsec	47.4 msec
Rate Generator (frequency)	21.09 Hz	691.2 KHz

1. Single 16-bit binary count

Interfaces

MULTIBUS™ Interface — All signals compatible with iSBC and MULTIBUS architecture

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — All signals TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125

Physical Characteristics

Width — 30.48 cm (12.00 inches)

Depth — 17.15 cm (6.75 inches)

Thickness — 1.27 cm (0.50 inch)

Weight — 3.97 gm (14 ounces)

Electrical Characteristics

DC Power Requirements — +5V @ 2.58A with no optional devices installed. For each 8741A add 135 mA. For each 220/330 resistor network, add 60 mA. Add the following for each EPROM/ROM installed.

Type	+5.0V Current Requirement	
	1ROM	2ROMS
2758	100 mA	125 mA
2716	100 mA	125 mA
2316E	120 mA	240 mA
2732	40 mA	55 mA
2364	40 mA	55 mA

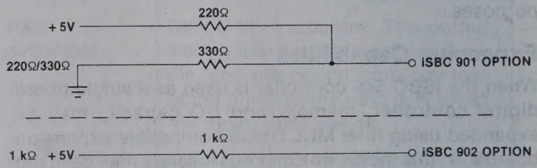
Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 569 Intelligent Digital Controller.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup



Environmental Characteristics

Operating Temperature — 0°C to 55°C (32°F to 131°F)

Relative Humidity — To 90% without condensation

Reference Manuals

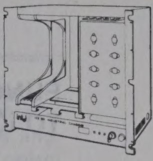
9800845-01 — iSBC 569 Intelligent Digital Controller Board Hardware Reference Manual (NOT SUPPLIED)

9803077 — iSBC 941 Digital Signal Processor User's Guide (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 569	Intelligent Digital Controller



iCS 910/920/930

SIGNAL CONDITIONING/TERMINATION PANELS

Interconnects iSBC analog and digital I/O ports to field signal/control wiring

Ribbon cable connection from panel is pin compatible with iSBC™ analog, CPU, and digital board I/O ports

Barrier strip screw terminals for

- **iCS 910: 32 single ended analog inputs (or 16 differential signal plus shield) plus four analog voltage outputs or two analog 4 to 20 mA current outputs**
- **iCS 920: 24 medium power digital inputs and/or outputs (55V, 300 mA max)**
- **iCS 930: 16 high power AC or DC digital inputs or outputs (280 VAC, 3A max)**

Flexible mounting kits for

- **19″ width RETMA rack**
- **NEMA type backwall**
- **iCS 80 Industrial Chassis**

Digital signal conditioning (iCS 920/930)

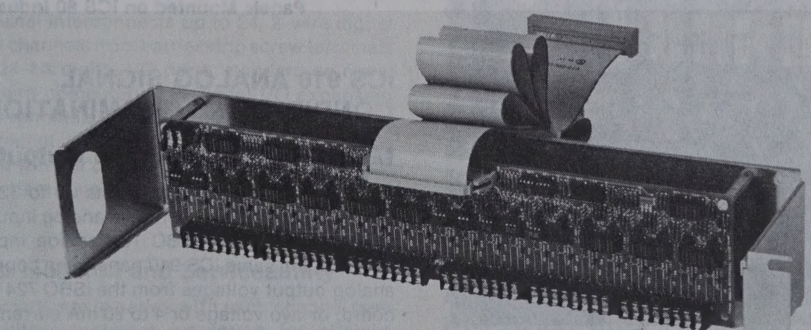
- **Sockets for optically isolated input filters and solid state output switches**
- **Pad space for transient suppressors, current limiting resistors, and voltage dividers**
- **Socketed fuse for overload protection (iCS 930)**
- **LED/channel status indicators**

Engineered printed circuit mounting space for customer analog input components (iCS 910)

- **Noise filters**
- **Current loop resistors**
- **Open circuit detection resistors**
- **Voltage divider resistors**
- **Thermistor bias current**

Submitted for UL recognition

The iCS 910/920/930 Signal Conditioning/Termination Panels are heavy duty printed circuit boards with screw terminations which allow industrial customers to easily connect their heavier gauge field signal wiring to Intel's line of 8- and 16-bit single board computers, and iSBC analog and digital I/O boards. Flat ribbon cables connect the iCS 910 panels to any of the Intel iSBC 700 series analog input and output board pin-outs. Flat ribbon cables also connect the iCS 920 panels and iCS 930 panel to the 50-pin digital I/O ports (8255 or UPI) on Intel's single board computers and digital I/O boards. Power for opto-isolators or line drivers (+5 VDC) can be supplied via this cable from the iSBC boards. Jumpers and a screw terminal block are provided on the iCS 920/930 panels to allow an external supply of +5V power. A similar jumper/terminal block is provided on the iCS 910 panel to allow users to connect external +15V (or greater) compliance voltage for larger analog output loads.



FUNCTIONAL DESCRIPTION COMMON TO iCS 910/920/930

Large Wire or Spade Lug Connections

The barrier strip screw terminations on the iCS 910/920/930 panels provide familiar connection points for factory electricians to terminate the heavier gauge wiring often pulled through conduits from sensors or control elements. These screw terminals securely connect up to 14 AWG gauge wire size (16-gauge on iCS 910/920 panels). Alternately, spade lugs can be crimped on field wiring and inserted under the screw terminals.

Mounting Flexibility and Serviceability

The iCS 910/920/930 panels were designed to be physically separate from iSBC boards or the iCS 80 chassis to allow maximum mounting flexibility and ease of serviceability. The panels and field wiring can be mounted in one area of the cabinet where electricians have access. Flat ribbon cable can then be run to the area where control electronics technicians have access.

The iCS 910/920/930 panels may be mounted horizontally in a 19" standard width (RETMA) rack using a recessed mounting panel (see Figure 1). Alternately, the panels can be mounted on a cabinet wall (e.g., NEMA cabinet backwall) using standoffs provided (see Figure 2). Or, for the most compact packaging, users can mount up to two iCS 910/920/930 panels vertically, directly on the front of the iCS 80 chassis using standoffs and holes provided (see Figure 3).

A black metal labelling strip is provided with each iCS 910/920/930 panel. White, blank gummed labels are included so that users can custom identify each input or output channel. A clear plastic cover is provided to protect against inadvertent touching or damage to the screw terminals or customer mounted components.

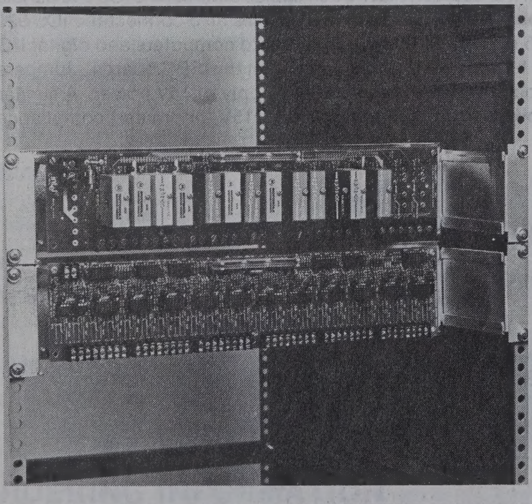


Figure 1. iCS 930 AC and iCS 920 Digital Signal Conditioning/Termination Panel Mounted on a 19" Width RETMA Rack

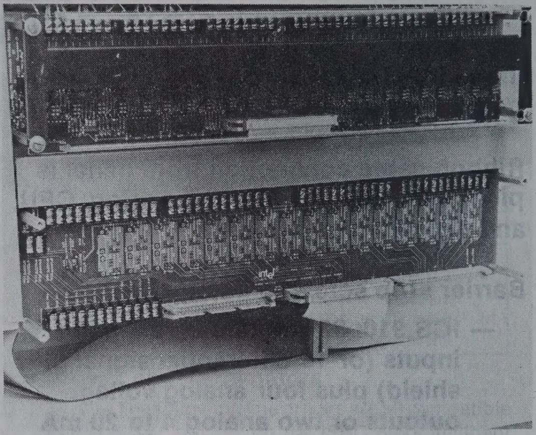


Figure 2. iCS 910/920 Signal Conditioning/Termination Panel Mounted on a NEMA Cabinet Backwall

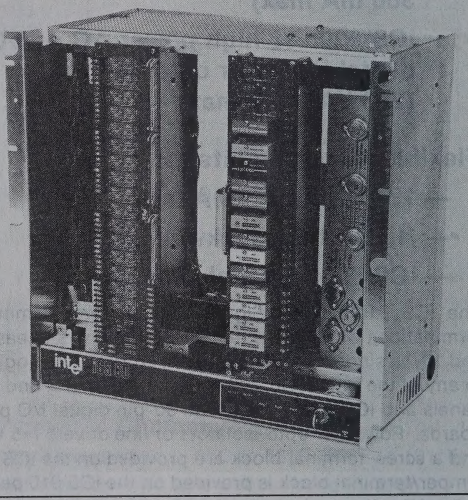


Figure 3. iCS 910/930 Signal Conditioning/Termination Panels Mounted on iCS 80 Industrial Chassis

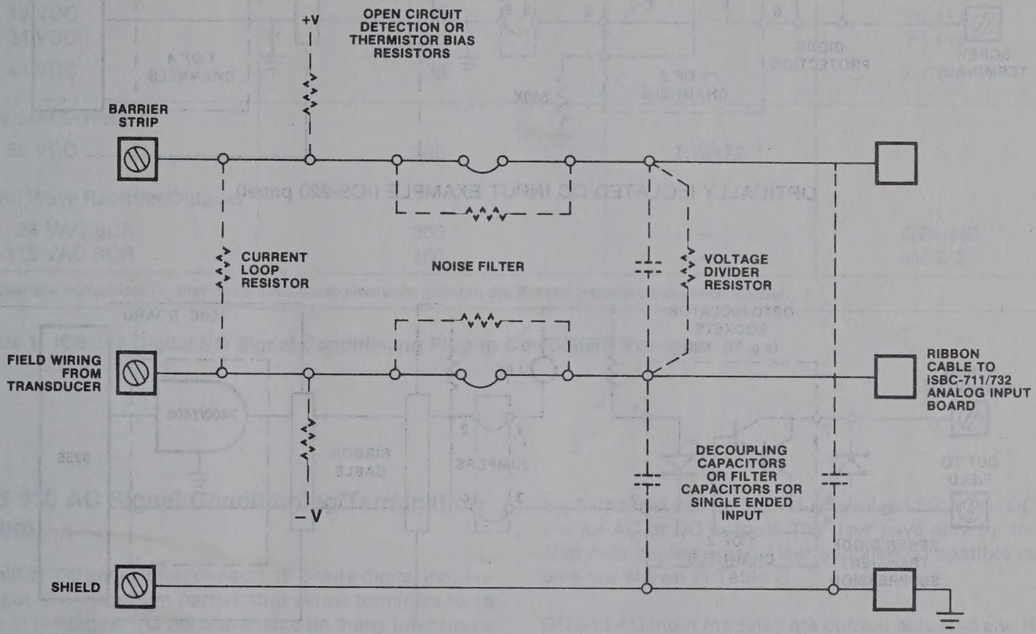
iCS 910 ANALOG SIGNAL CONDITIONING/TERMINATION PANEL

Mixed Analog Input and Output Signals

A single iCS 910 panel connects up to 32 single ended analog inputs (or 16 differential analog inputs plus shield) to the iSBC 711 or iSBC 732 analog input boards. In addition, the same iCS 910 panels can connect up to four analog output voltages from the iSBC 724 analog output board, or two voltage or 4 to 20 mA current loop outputs from the iSBC 732 combination analog input/output board. Three flat ribbon cables are included in the iCS 910 installation kit (two analog inputs, one analog output) to route signals to iSBC 711/724/732 boards.

Engineered Signal Conditioning Mounting Space

Printed circuit traces on the iCS 910 panel connect each screw terminal analog input channel to the flat ribbon cable connector. Users can jump straight through signal connections if they desire. Each input channel trace, however, passes through a custom engineered printed circuit area onto which users may mount components to signal condition analog input signals. Pad traces and holes are designed to allow easy mounting of R-C noise filters, input voltage resistor/divider networks, current loop input resistors, open circuit detection resistors, or to supply thermistor bias current (see Figure 4 for schematic of a typical analog input channel).



+V
OPEN CIRCUIT DETECTION OR THERMISTOR BIAS RESISTORS
BARRIER STRIP
CURRENT LOOP RESISTOR
NOISE FILTER
VOLTAGE DIVIDER RESISTOR
FIELD WIRING FROM TRANSDUCER
RIBBON CABLE TO iSBC-711/732 ANALOG INPUT BOARD
DECOUPLING CAPACITORS OR FILTER CAPACITORS FOR SINGLE ENDED INPUT
−V
SHIELD

Figure 4. iCS 910 Analog Input Signal Conditioning Examples

iCS 920 DIGITAL SIGNAL CONDITIONING/TERMINATION PANEL

The iCS 920 panel interconnects up to 24, 2-wire digital input or output channels from barrier strip screw terminals to the 16- or 24-bit digital I/O ports, standard on many Intel single board computers and digital I/O expansion boards. Screw terminals allow for one each 16 AWG size wire for differential (2-wire) connections or two each AWG 18-gauge wire for daisy chaining grounds or power for external contact sensing.

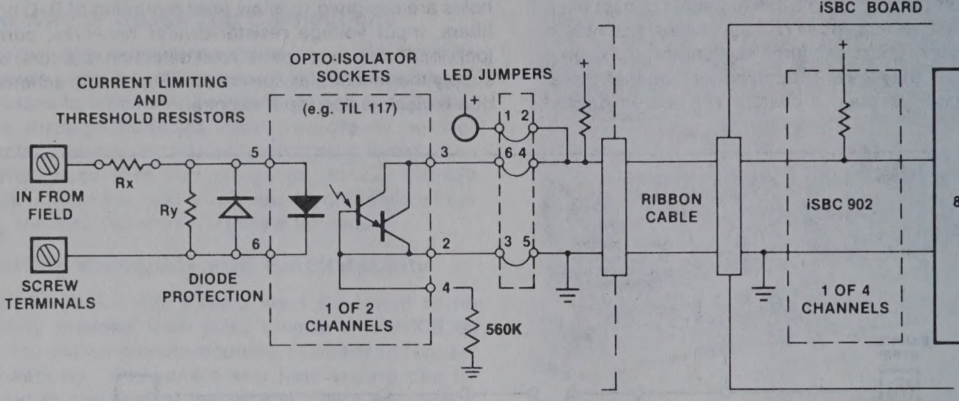
Flexibility in Isolation and Serviceability

Dual-in-line sockets are in series with each channel (see Figure 5) to allow customer jumpering for straight through connections (TTL I/O), or for insertion of popular DIP packaged opto-isolators or digital output high current driver transistors. Circuit pads are available for mounting voltage divider/threshold resistors and protection diodes.

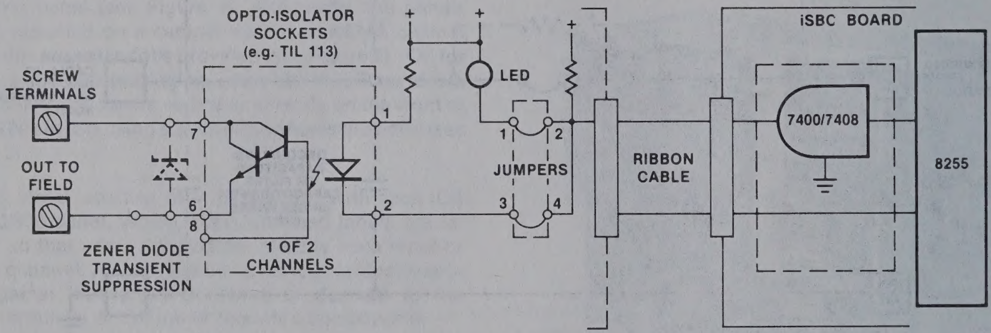
Groups of four inputs can have mixed voltage levels, opto-isolation, or straight through connections in groups of two. Output groups of four can be mixed opto-isolated or high current drive in groups of two. DIP components from a wide variety of vendors are selected and inserted by users based on their application. The iCS 920 manual recommends several alternative components and offers design assistance for your I/O configuration. Digital signal conditioning examples for several common industrial voltages are shown in Table 1 and in the diagrams below (see Figure 5).

Active Channel Indicators

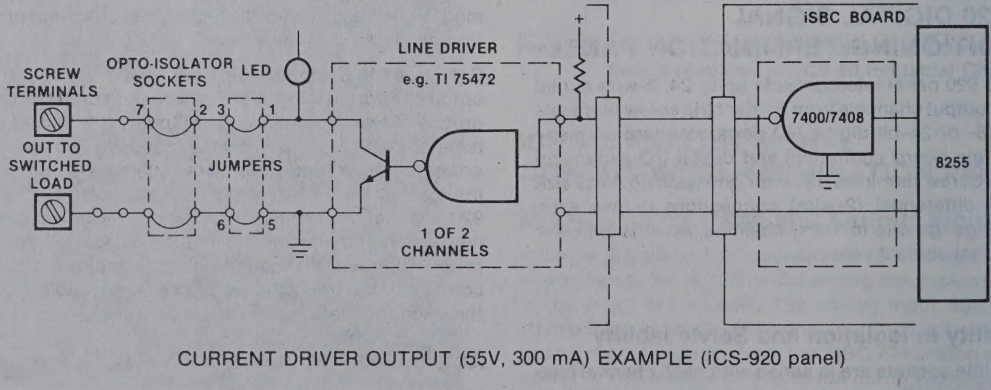
Light emitting diodes (LEDs) are mounted adjacent to each channel's screw terminals and may be jumpered in to indicate the Hi-Lo status of each of the 24 input or output channels.


iSBC BOARD
OPTO-ISOLATOR SOCKETS
(e.g. TIL 117)
LED JUMPERS
CURRENT LIMITING AND THRESHOLD RESISTORS
Rx
Ry
IN FROM FIELD
SCREW TERMINALS
DIODE PROTECTION
5
6
3
2
4
1 2
6 4
3 5
560K
1 OF 2 CHANNELS
RIBBON CABLE
iSBC 902
1 OF 4 CHANNELS
8255

OPTICALLY ISOLATED DC INPUT EXAMPLE (iCS-920 panel)


iSBC BOARD
OPTO-ISOLATOR SOCKETS
(e.g. TIL 113)
SCREW TERMINALS
OUT TO FIELD
ZENER DIODE TRANSIENT SUPPRESSION
7
6
8
1
2
1 OF 2 CHANNELS
LED
JUMPERS
1
2
3
4
RIBBON CABLE
7400/7408
8255

OPTICALLY ISOLATED DC OUTPUT EXAMPLE (iCS-920 panel)


iSBC BOARD
LINE DRIVER
e.g. TI 75472
SCREW TERMINALS
OPTO-ISOLATOR SOCKETS
LED
OUT TO SWITCHED LOAD
JUMPERS
7
2
3
1
6
5
1 OF 2 CHANNELS
7400/7408
8255

CURRENT DRIVER OUTPUT (55V, 300 mA) EXAMPLE (iCS-920 panel)

Figure 5. Digital Signal Conditioning Examples

Digital Voltage Input or Output Load Voltage	Maximum Input Current (mA)	Threshold Voltage (V)	Opto-Isolators*	Diode Protection*
Opto-Isolated Input				
5 VDC	50	3	TIL117	1N4002
12 VDC	50	6	TIL117	1N4002
24 to 26 VDC	40	6	TIL117	1N4002
48 VDC	20	12	4N36	1N4002
	Maximum Output Current (mA)		**Line Driver***	**Opto-Isolators***
Opto-Isolated Output				
12 VDC	100		—	TIL113
24 VDC	100		—	TIL119
48 VDC	100		—	MCS 2
Current Drivers				
55 VDC	300		TI75472	—
Half Wave Rectifier Outputs				
24 VAC SCR	300		—	GE4N40
115 VAC SCR	150		—	MCS 2

*Example component — alternate source components are listed in the iCS 920 Hardware Reference Manual.

Table 1. iCS 920 Digital I/O Signal Conditioning Plug-In Component Examples

iCS 930 AC Signal Conditioning/Termination Panel

The iCS 930 panel interconnects 16 2-wire digital input or output channels from barrier strip screw terminals to 16 bits of the digital I/O ports available on many Intel single board computers and digital I/O expansion boards. The iCS 930 panel differs from the iCS 920 digital signal conditioning/termination panel in that the iCS 930 panel handles higher AC or DC voltages and currents (up to 280V, 3A), such as those found on many 115 VAC machines, motor starters, and industrial control panels. The iCS 930 panel is also recommended for optically isolated DC outputs greater than 100 mA.

The iCS 930 screw terminals accept up to 14 AWG size wire each for differential (2 wires per channel) connections, or two 14 AWG size wires for daisy chaining grounds or power from external sources.

Modular Isolation/Switching with Easy Serviceability

Each iCS 930 panel accepts up to 16 user supplied, optically isolated input modules or optically isolated solid state switches, for either AC or DC voltages (see Figure 6). Each module is screw mountable/replaceable and can be mixed for AC or DC input, or AC or DC output, in groups of four. Among groups of four inputs (or outputs) each channel can be individually mixed for AC or DC input (or AC or DC output). The user pays only for those channels implemented. User supplied compatible modules are shown in Table 2.

DC and AC input modules are current actuated and thus provide a 5-ms filter against spurious noise spikes or contact bounce. AC solid state output modules provide zero crossing turn on to minimize arcing.

Protection Circuitry

Each of the 16 channels contain a socketed fuse to protect against overload. In addition, mounting pads are available on each channel output for user supplied voltage transient RC "snubber" components or inductive pulse suppression, e.g., metallic-oxide-varistor (MOV) for large motor starting.

Active Channel Indicators

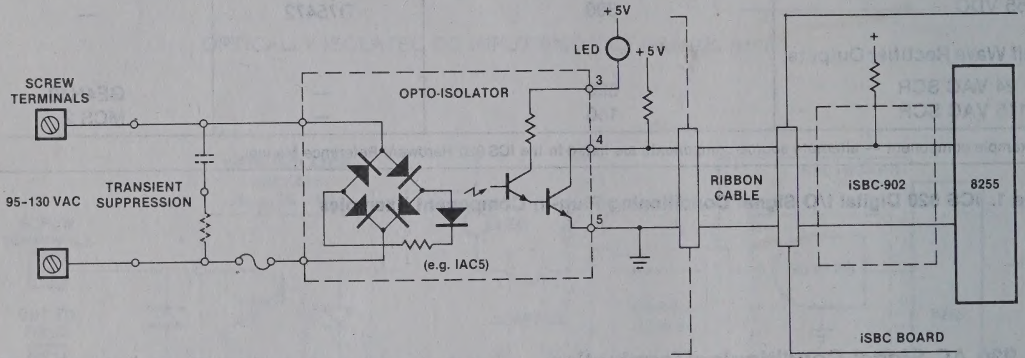
Light emitting diodes (LEDs) are mounted adjacent to each channel's screw terminals and opto-module to indicate Hi-Lo status of that channel and to assist in troubleshooting servicing.

Examples of iCS 930 input and output schematics are shown in Figure 6.

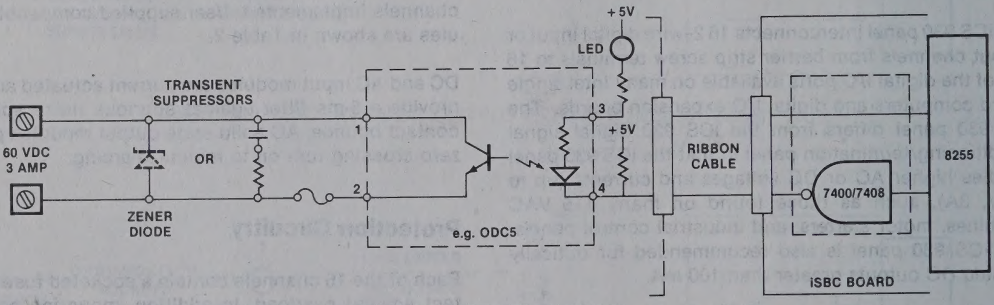
Signal Conditioning Desired	Voltage Rating	Maximum Input Current	Opto-22 Number*	Motorola Number*
AC Input — 115 VAC	95 to 130 VAC	10 mA	IAC5	IAC5
220 VAC	180 to 280 VAC	10 mA	IAC5A	
DC Input — 5 μsec Filter	10 to 32 VDC	32 mA	IDC5	IDC5
Fast, 50 μsec On	4 to 16 VDC	14 mA	IDC5B	
		Output Current Rating		
AC Output	12 to 140 VAC	3A	OAC5	OAC5
	24 to 280 VAC	3A	OAC5A	
DC Output	10 to 60 VDC	3A	ODC5	ODC5
	200 VDC	1A	ODC5A	

*Motorola and Opto-22 sales offices are located in North America, Europe, and Japan.

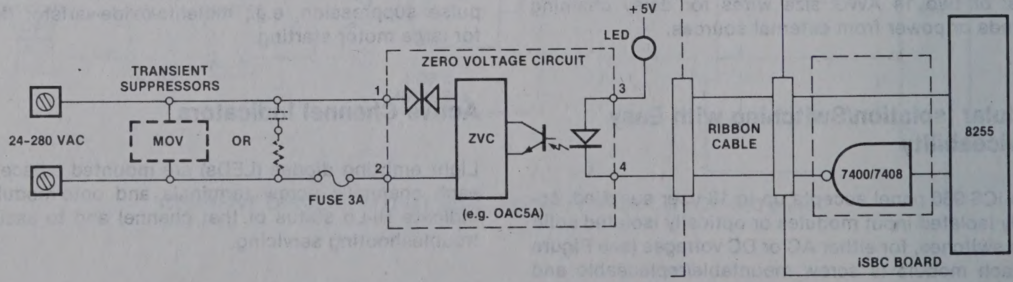
Table 2. Optically Isolated Modules Compatible with iCS 930 Signal Conditioning/Termination Panel


+5V
LED
+5V
SCREW TERMINALS
OPTO-ISOLATOR
3
4
5
95-130 VAC
TRANSIENT SUPPRESSION
(e.g. IAC5)
RIBBON CABLE
iSBC-902
8255
+
iSBC BOARD

AC INPUT EXAMPLE (iCS-930 panel)


+5V
LED
TRANSIENT SUPPRESSORS
60 VDC 3 AMP
OR
ZENER DIODE
1
2
3
4
+5V
e.g. ODC5
RIBBON CABLE
7400/7408
8255
iSBC BOARD

DC SOLID STATE OUTPUT


+5V
LED
ZERO VOLTAGE CIRCUIT
TRANSIENT SUPPRESSORS
24-280 VAC
MOV
OR
1
2
3
4
ZVC
FUSE 3A
(e.g. OAC5A)
RIBBON CABLE
7400/7408
8255
iSBC BOARD

AC SOLID STATE RELAY OUTPUT EXAMPLE (iCS-930 panel)

Figure 6. Typical iCS 930 Signal Conditioning Examples

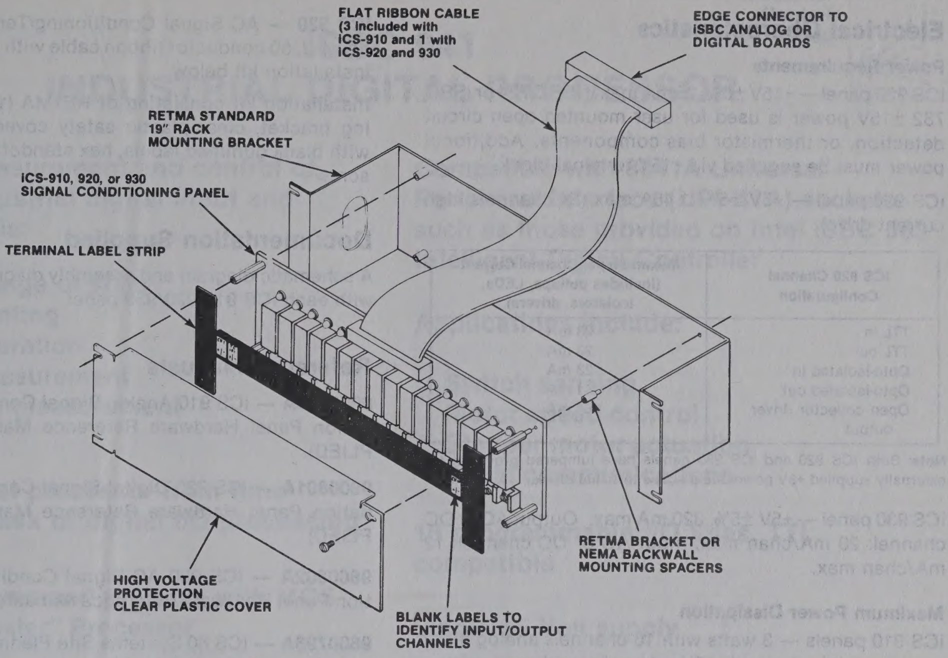

FLAT RIBBON CABLE
(3 included with
iCS-910 and 1 with
iCS-920 and 930
EDGE CONNECTOR TO
iSBC ANALOG OR
DIGITAL BOARDS
RETMA STANDARD
19" RACK
MOUNTING BRACKET
iCS-910, 920, or 930
SIGNAL CONDITIONING PANEL
TERMINAL LABEL STRIP
RETMA BRACKET OR
NEMA BACKWALL
MOUNTING SPACERS
HIGH VOLTAGE
PROTECTION
CLEAR PLASTIC COVER
BLANK LABELS TO
IDENTIFY INPUT/OUTPUT
CHANNELS

Figure 7. Mounting Arrangements for Signal Conditioning/Termination Panels

SPECIFICATIONS

(For iCS 910/920/930 panels unless otherwise specified)

Number of Lines

iCS 910 Panel

Analog Inputs — Sixteen 3-wire (differential signal plus shield) or 32 single ended

Analog Outputs — Four 2-wire voltage output (iSBC 724 Analog Board) or two 2-wire current output (iSBC 732 Analog Board)

iCS 920 Panel — Zero to 24 digital inputs or outputs in groups of four

iCS 930 Panel — Zero to 16 digital inputs or outputs in groups of four

Isolation Characteristics

Line-to-Line Isolation — 250 VDC or RMS AC (iCS 910/920 panels), 500 VDC or RMS AC (iCS 930 panel)

Input/Output Isolation — 250 VDC or RMS AC (iCS 920 panel), 500 VDC or RMS AC (iCS 930 panel)

Physical Characteristics

Width: 36.63 cm (14.65 in.)

Height: 8.13 cm (3.25 in.)

Thickness: 0.24 cm (0.093 in.), iCS 910/920 panel
0.32 cm (0.125 in.), iCS 930 panel

	iCS 910	iCS 920	iCS 930
Weight:	(Minimum, PC panel only)		
	455 gm(16 oz)	455 gm (16 oz)	681 gm (24 oz)
	(Maximum with all components and mounting kit installed)		
	1.6 Kg (56 oz)	1.8 Kg (64 oz)	3.4 Kg (120 oz)
Depth:	(With components and clear plastic cover installed)		
	5.08 cm(2.0 in.)	5.08 cm (2.0 in.)	5.08 cm(2.0 in.)
Connectors:	(Barrier strip)		
	2/56 screws 48 AI 12 AO 2 power	2/56 screws 48 DI/DO 2 +5V power	6/32 screws 32 DI/DO 2 +5V power
	(J1, J2, J3 to iSBC boards)		
	50-pin 0.1 in. centers (2.54 mm)	50-pin 0.1 in. centers (2.54 mm)	50-pin 0.1 in. centers (2.54 mm)
	(Mating connector: 3M 3415-0000 or TI H3-12125)		

Maximum Distance from iSBC Boards

The iCS 910/920/930 panels are shipped with 4-ft. long cables. With customer provided 50-conductor or twisted pair ribbon cable, however, the iCS 910/920/930 panels can be mounted remote from the iSBC analog or digital I/O boards. In electrically quiet environments using normal iSBC board line driver/receivers, the iCS 910/920/930 panels should be able to operate up to 25 ft. (7.69m) from the iSBC board.

Electrical Characteristics

Power Requirements

iCS 920 panel — +15V ±5%, 25 mA max if iSBC 724 or iSBC 732 ±15V power is used for user mounted open circuit detection, or thermistor bias components. Additional power must be supplied via +15V terminal block.

iCS 920 panel — +5V ±5%, 1.46A max (24 channels high current drive)

iCS 920 Channel Configuration	Maximum per Channel Current (Includes pullups, LEDs, isolators, drivers)
TTL in	23 mA
TTL out	23 mA
Opto-isolated in	23 mA
Opto-isolated out	41 mA
Open collector driver output	61 mA

Note: Both iCS 920 and iCS 930 panels have jumpered provision for externally supplied +5V power via a screw terminal block.

iCS 930 panel — +5V ±5%, 320 mA max. Output AC or DC channel: 20 mA/chan max; Input AC or DC channel: 12 mA/chan max.

Maximum Power Dissipation

iCS 910 panels — 3 watts with 16 channels analog input signal conditioning and +15V external compliance voltage

iCS 920 panels — 12 watts with 24 channels each containing high current driver outputs

iCS 930 panels — 80 watts with 16 channels of AC or DC output

Underwriters Laboratory (UL) Recognition

The iCS 910/920/930 signal conditioning/termination panels have been submitted to Underwriters Laboratories for approval as a UL recognized component under the UL safety standard for process control equipment, UL 1092.

Environmental Characteristics

Operating Temperature — 0 to 70°C (32°F to 158°F)

Relative Humidity — 0 to 90%, noncondensing

Hardware Supplied

iCS 910 — Analog Signal Conditioning/Terminating Panel, three 4-ft, 50-conductor flat ribbon cables with connectors, and installation kit below

iCS 920 — Digital Signal Conditioning/Termination Panel, one 4-ft, 50-conductor flat ribbon cable with connectors, and installation kit below

iCS 930 — AC Signal Conditioning/Termination Panel, one 4-ft, 50-conductor ribbon cable with connectors, and installation kit below

Installation kit consisting of RETMA (19″ rack) mounting bracket, clear plastic safety cover, labelling strip with blank gummed labels, hex standoffs and mounting screws

Documentation Supplied

A schematic diagram and assembly diagram are supplied with each iCS 910/920/930 panel.

Reference Manuals

9800800A — iCS 910 Analog Signal Conditioning/Termination Panel Hardware Reference Manual (NOT SUPPLIED).

9800801A — iCS 920 Digital Signal Conditioning/Termination Panel Hardware Reference Manual (NOT SUPPLIED)

9800802A — iCS 930 AC Signal Conditioning/Termination Panel Hardware Reference Manual (NOT SUPPLIED)

9800798A — iCS 80 Systems Site Planning and Installation Guide (NOT SUPPLIED), but supplied with iCS 80 Industrial Chassis

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

Installation

Complete instructions for installation and service are contained in the applicable iCS 910/920/930 Hardware Reference Manual. Additional system level information is available in the iCS 80 Systems Site Planning and Installation Guide, including RETMA and NEMA cabinet mounting, field signals, ground wiring and cooling suggestions.

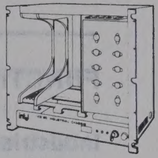
Warranty

The iCS 80 Industrial Chassis is warranted to be free from defects in materials and workmanship under normal use and service for a period of 90 days from date of shipment.

ORDERING INFORMATION

Part Number	Description
iCS 910	Analog signal conditioning/termination panel
iCS 920	Digital signal conditioning/termination panel
iCS 930	AC signal conditioning/termination panel

iCS
Industrial
Control
Series



iSBC 941
INDUSTRIAL DIGITAL PROCESSOR

Provides measurement and control of common industrial digital input and output signals:

Sense change of state
Pulse counting
Pulse generation
Period measurement
Frequency measurement

Off-loads host processor from time-consuming task of digital I/O processing

Simplified command protocol with MCS 80/85/86 "Master" Processor

Compatible with 8041A Universal Peripheral Interface (UPI-41A) sockets such as those provided on Intel iSBC 569 Intelligent Digital Controller

Applications include:

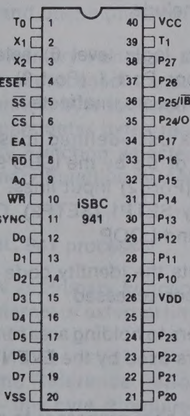
Switch sensing
Motor speed control
Stepper motor actuation
Serial communications

16 programmable I/O lines, TTL compatible

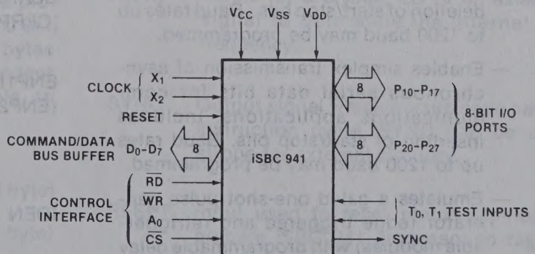
Single +5 Volt supply

The iSBC 941 Industrial Digital Processor is a 40-pin DIP device which provides the user with easy-to-use processing of digital input and output signals desired in many industrial automation environments. One of nine digital I/O functions can be selected at any one time for measuring, counting, or controlling up to 16 separate I/O lines. Additional utility commands allow reading or setting the condition of unused I/O lines. Simplex serial input and output modes can assemble or disassemble bytes transmitted asynchronously over TTL lines, including insertion and deletion of start/stop bits. The device has two 8-bit, TTL compatible I/O ports.

PIN CONFIGURATION


T_0 1
X_1 2
X_2 3
RESET 4
$\overline{SS}$ 5
$\overline{CS}$ 6
EA 7
$\overline{RD}$ 8
A_0 9
$\overline{WR}$ 10
SYNC 11
D_0 12
D_1 13
D_2 14
D_3 15
D_4 16
D_5 17
D_6 18
D_7 19
V_{SS} 20
iSBC 941
40 V_{CC}
39 T_1
38 P_{27}
37 P_{26}
36 $P_{25}/\overline{IBF}$
35 P_{24}/OBF
34 P_{17}
33 P_{16}
32 P_{15}
31 P_{14}
30 P_{13}
29 P_{12}
28 P_{11}
27 P_{10}
26 V_{DD}
25
24 P_{23}
23 P_{22}
22 P_{21}
21 P_{20}

BLOCK DIAGRAM


V_{CC} V_{SS} V_{DD}
CLOCK
X_1
X_2
RESET
COMMAND/DATA BUS BUFFER
D_0-D_7
8
CONTROL INTERFACE
$\overline{RD}$
$\overline{WR}$
A_0
$\overline{CS}$
iSBC 941
8
P_{10}-P_{17}
8
P_{20}-P_{27}
8-BIT I/O PORTS
T_0, T_1 TEST INPUTS
SYNC

FUNCTIONAL DESCRIPTION

Industrial Digital Processor

Designed to operate as a slave device, the iSBC 941 processor may be requested to implement one of nine preprogrammed Primary Functions. These Primary Functions are subroutines which are stored in program memory of the iSBC 941 device. Each Primary Function has a specific I/O task. Available Primary Functions include:

EVENT — Monitors and counts up to eight input lines for event counting or comparison to a preset count for each line. Interrupts may be generated or counter can be read 'on-the-fly' without changing its state.

FCOUNT — Measures frequency of one of eight digital inputs over a programmable period. Inputs may be selected under user program control or iSBC 941 processor may be requested to automatically scan inputs in sequential order, update, and hold or interrupt for reading each 16-bit counter. Input frequencies up to 18 KHz may be measured.

FREQ — Generates up to eight gated frequency outputs with separately programmable pulse width and periods and complementary synchronous outputs.

PERIOD — Measures the period of up to four inputs.

SCAN — Monitors up to 16 input lines for change-of-state and direction of change. Change-of-state interrupts may be generated. User can individually disable inputs.

SERIN — Enables simplex reception and 8-bit byte assembling of asynchronously transmitted serial data bits for communications applications. Includes detection/deletion of start/stop bits. Baud rates up to 1200 baud may be programmed.

SEROUT — Enables simplex transmission of asynchronous serial data bits for communications applications. Includes insertion of start/stop bits. Baud rates up to 1200 baud may be programmed.

SHOT1 — Emulates a gated one-shot pulse generator (edge triggered and retriggerable modules) with programmable delay and period. Complimentary, synchronous one-shots can be created on separate output lines, on up to eight lines.

STEPPER — Generates up to eight programmable outputs that may be used for control of stepper motors. Step rate, step count, and step direction are user defined. Stepper motors designed for up to eight phase control may be controlled directly or stepper motor translator signals may be generated..

Any of the sixteen UPI processor I/O lines that are not used by a Primary Function are available for general purpose use; e.g., direct status reads or latched digital outputs, through the use of Utility Commands.

Commands recognized by the iSBC 941 Industrial Digital Processor are defined by one of two categories, Control Commands or Utility Commands. Control Commands are used to start and stop a Primary Function. Utility Commands are typically associated with moving a byte of information or reading the status of the iSBC 941 processor through the COMMAND/DATA Bus Buffer.

Control Commands available are:

ENFLAG — Enables the iSBC 941 processor to send interrupts via its I/O lines to the host processor.

INITPF — Selects the desired Primary Function and initializes parameters used by the Primary Function.

LOOP — Continuously executes the selected Primary Function at a specific rate.

PACIFY — Resets all iSBC 941 processor I/O lines to the input state and clears all control variables.

PAUSE — Commands the iSBC 941 processor to exit the LOOP or INITPF mode.

Utility Commands include:

CLRP1 (CLRP2) — Sets (to logic level 0) selected iSBC 941 processor Port 1 (Port 2) output lines. All other lines are unaffected.

ENP1IN (ENP2IN) — Enables user-defined mask to inhibit the writing of '0's by the iSBC 941 processor to Port 1 (Port 2) input lines. This function is used by SETP1 (SETP2), CLRP1 (CLRP2), STEP and LOOP.

IDEN — Requests the identity code of the iSBC 941 processor accessed.

LATCH — Transfers to holding area for reading all eight counters used by the EVENT Primary Function.

RDEC — Enables host processor to read one of eight user-specified event accumulators used by the EVENT Primary Function.

RDFQ — Reads bytes from the iSBC 941 processor's first-in-first-out (FIFO) buffer (used by SCAN and SEROUT Primary Functions).

RDHR — Enables the host processor to read the contents of the iSBC 941 holding register specified (used by PULSE, PERIOD, and EVENT Primary Functions).

RDIDV — Enables the host processor to read the iSBC 941 processor's input-data-valid (IDV) flags.

RDLC — Enables host processor to read one of eight user specified EVENT counters previously stored by LATCH command.

RDP1 (RDP2) — Reads data byte present at iSBC 941 processor Port 1 (Port 2) and sends to host processor.

SETOE — Sets output enable parameter bits.

SETP1 (SETP2) — Sets (to logic level 1) selected iSBC 941 processor Port 1 (Port 2) output lines. All other lines are unaffected.

SETSF — Sets the Time Reference Period scale factor for value.

WRP1 (WRP2) — Allows host processor to write to iSBC 941 processor Port 1 (Port 2).

Simple Command Protocol

iSBC 941 functions may be implemented with minimum software overhead required of the host processor. An easy-to-implement protocol ensures that communication between the iSBC 941 processor and host CPU is straightforward and uncomplicated.

Implementing a Primary Function involves simple programming; the host processor transmits to the iSBC 941 processor a command byte followed by parameter bytes (the number of parameter bytes required is dependent upon the Primary Function selected). For example, to execute the Primary Function SCAN:

(1) Initialize iSBC 941 processor (Command byte)

(2) Select SCAN as Primary Function and select internal or external time reference (Parameter byte)

(3) Program Time Reference Period (scan rate — this byte is required only if internal time reference was selected in (2)) (Parameter byte)

(4) Define return message format (Parameter byte)

(5) Enable selected SCAN input lines (enabled in groups of eight) (Parameter byte)

(6) Terminate parameter list (Command byte)

(7) Enable iSBC 941 processor interrupt outputs (Command byte)

(8) Request execution (Command byte)

PIN DESCRIPTION

Signal	**Description**
D_0-D_7	Three-state, bidirectional COMMAND/DATA BUS BUFFER lines used to interface the iSBC 941 processor to an 8-bit master system data bus.
P_{10}-P_{17}	8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}-P_{27}	8-bit, PORT 2 quasi-bidirectional I/O lines. Control can configure P_{24} as OBF (Output Buffer Full), P_{25} as IBF (Input Buffer Full) to send interrupt signals to master CPU.
$\overline{WR}$	I/O write input which enables the master CPU to write data and command words to the iSBC 941 COMMAND/DATA BUS BUFFER.
$\overline{RD}$	I/O read input which enables the master CPU to read data and status words from the COMMAND/DATA BUS BUFFER or status register.
$\overline{CS}$	Chip select input used to select one iSBC 941 processor out of several connected to a common data bus.
A_0	Address input used by the master processor to indicate whether byte transfer is data or command.
T_0, T_1	Input pins used by various iSBC 941 processor routines.
X_1, X_2	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	Output signal which occurs once per iSBC 941 instruction cycle. SYNC can be used as a strobe for external circuitry.
RESET	Input used to reset status flip-flops and to prepare iSBC 941 processor to receive commands.
V_{CC}	+5V power supply pin.
V_{DD}	+5V during normal operation.
V_{SS}	Circuit ground potential.
EA	Circuit ground potential.
$\overline{SS}$	Connect to +5V through 10K-ohm pull-up resistor

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Ambient Temperature Under Bias ....0°C to 70°C
Storage Temperature ....−65°C to +150°C
Voltage on Any Pin With Respect
 to Ground ....0.5V to +7V
Power Dissipation ....1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} = 0V$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except X_1, X_2)	-0.5	0.8	V	
V_{IH1}	Input High Voltage (All except X_1, X_2, $\overline{RESET}$, $\overline{WR}$, $\overline{CS}$)	2.0	V_{CC}	V	
V_{IH2}	Input High Voltage (X_1, X_2, $\overline{RESET}$)	3.0	V_{CC}	V	
V_{IH3}	Input High Voltage ($\overline{WR}$, $\overline{CS}$)	2.2	V_{CC}	V	
V_{OL1}	Output Low Voltage (D_2–D_7, Sync)		0.45	V	$I_{OL} = 2.0$ mA
V_{OL2}	Output Low Voltage (All Other Outputs Except Prog)		0.45	V	$I_{OL} = 1.6$ mA
V_{OH1}	Output High Voltage (D_0–D_7)	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4		V	$I_{OH} = -50\ \mu A$
I_{IL}	Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0,)		±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{OZ}	Output Leakage Current (D_0–D_7, High Z State)		±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{LI1}	Low Input Load Current ($P_{10}P_{17}$, $P_{20}P_{27}$)		0.5	mA	$V_{IL} = 0.8V$
I_{LI2}	Low Input Load Current ($\overline{RESET}$, SS)		0.2	mA	$V_{IL} = 0.8V$
I_{DD}	V_{DD} Supply Current		15	mA	
$I_{CC} + I_{DD}$	Total Supply Current		125	mA	

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} = 0V$, $V_{CC} = V_{DD} = +5V \pm 5\%$

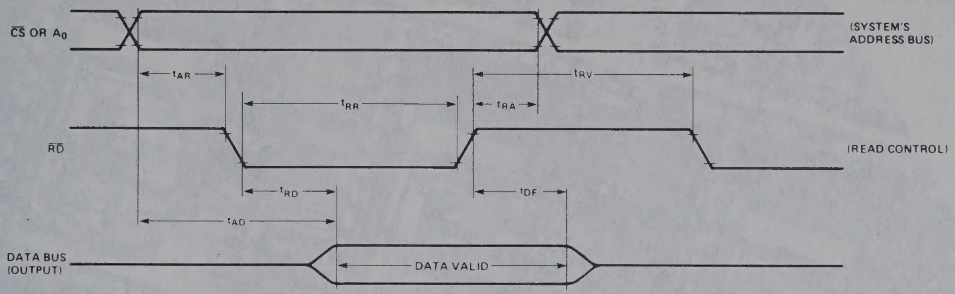
DBB READ

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	$\overline{CS}$, A_0 Setup to $\overline{RD}$↓	0		ns	
t_{RA}	$\overline{CS}$, A_0 Hold After $\overline{RD}$↑	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay		225	ns	$C_L = 150$ pF
t_{RD}	$\overline{RD}$↓ to Data Out Delay		225	ns	$C_L = 150$ pF
t_{RDF}	$\overline{RD}$↑ to Data Float Delay		100	ns	
t_{RV}	Recovery Time Between Reads And/Or Write	300		ns	
t_{CY}	Cycle Time	2.5	15	μs	

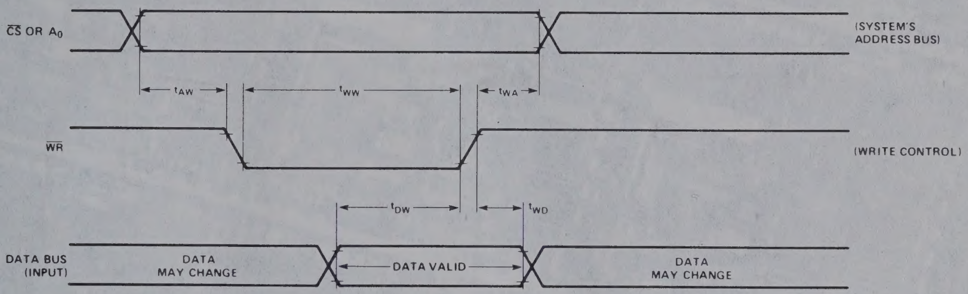
DBB WRITE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	CS, A_0 Setup to WR↓	0		ns	
t_{WA}	CS, A_0 Hold After WR↑	0		ns	
t_{WW}	WR Pulse Width	250		ns	
t_{DW}	Data Setup to WR↑	150		ns	
t_{WD}	Data Hold Aftert WR↑	0		ns	

1. READ OPERATION—DATA BUS BUFFER REGISTER.


$\overline{CS}$ OR A_0
(SYSTEM'S ADDRESS BUS)
t_{AR}
t_{RV}
t_{RR}
t_{RA}
$\overline{RD}$
(READ CONTROL)
t_{RD}
t_{DF}
t_{AD}
DATA BUS (OUTPUT)
DATA VALID

2. WRITE OPERATION—DATA BUS BUFFER REGISTER.


$\overline{CS}$ OR A_0
(SYSTEM'S ADDRESS BUS)
t_{AW}
t_{WW}
t_{WA}
$\overline{WR}$
(WRITE CONTROL)
t_{DW}
t_{WD}
DATA BUS (INPUT)
DATA MAY CHANGE
DATA VALID
DATA MAY CHANGE

Reference Manuals

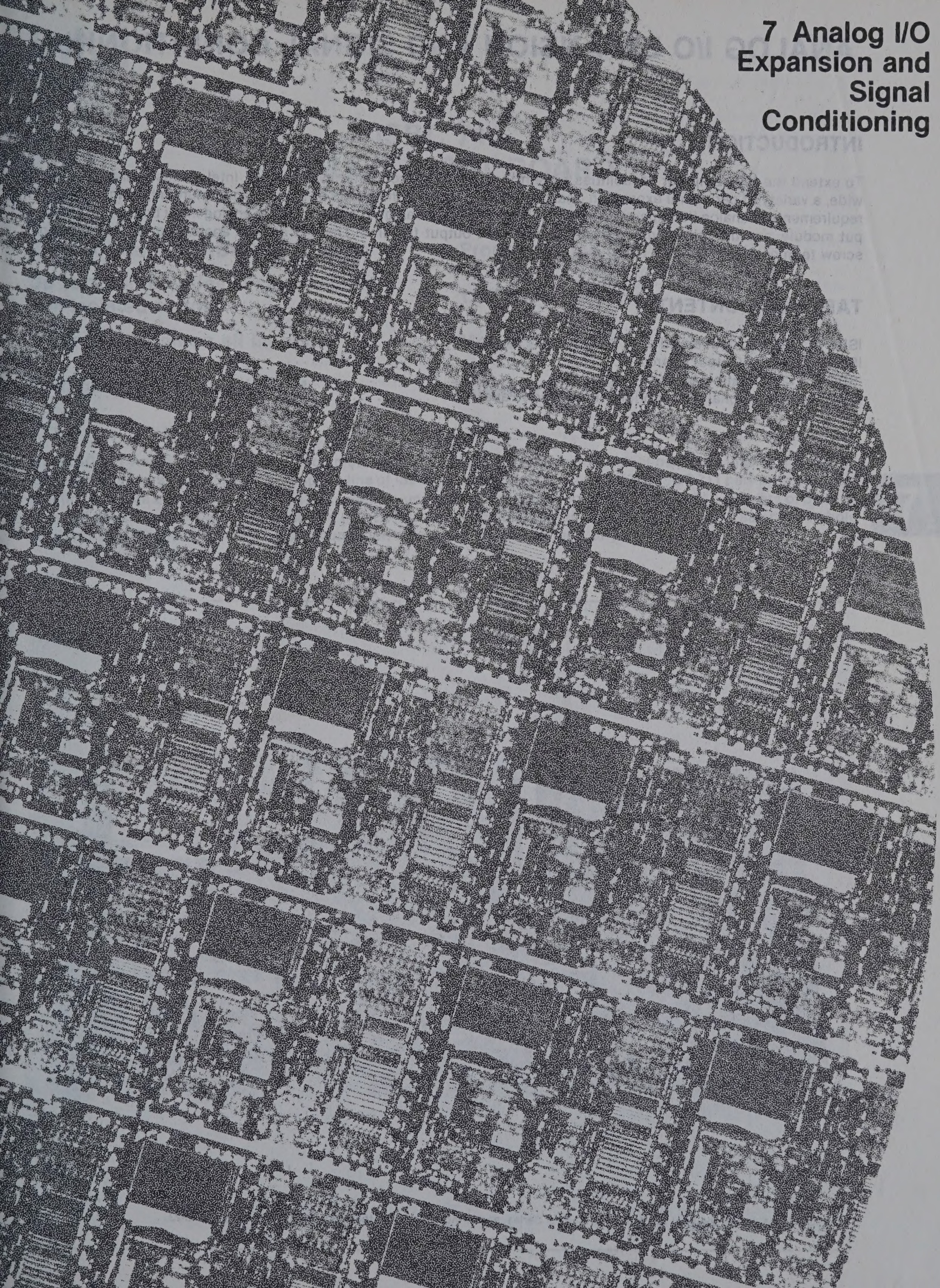
9803077 — iSBC 941 Industrial Digital Processor User's Guide (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	**Description**
SBC 941	Industrial Digital Processor

7 Analog I/O Expansion and Signal Conditioning



ANALOG I/O EXPANSION AND SIGNAL CONDITIONING

INTRODUCTION

To extend the full computer capabilities present on each iSBC computer even further, Intel makes available, worldwide, a variety of peripheral expansion boards designed to meet the needs of those manufacturers having increased requirements in analog I/O expansion boards. There are three analog I/O boards, one an analog input board, one an output module, and the third combines analog input and output features. There is also an analog signal conditioning/screw termination panel.

TABLE OF CONTENTS

iSBC 711 Analog Input Board 7-3
iSBC 724 Analog Output Board 7-7
iSBC 732 Combination Analog I/O Board 7-10
iCS 910 Analog Signal Conditioning/Termination Panel . . . . **

**The iCS 910 is part of the Intel iCS Industrial Control Series, and is incorporated in the iCS 910/920/930 Data Sheet. 6-23.

iSBC 711
ANALOG INPUT BOARD

iSBC 80 and MULTIBUS compatible

Up to 16 differential/32 single-ended non-isolated inputs

Fault protection on all inputs

Voltage or current loop input

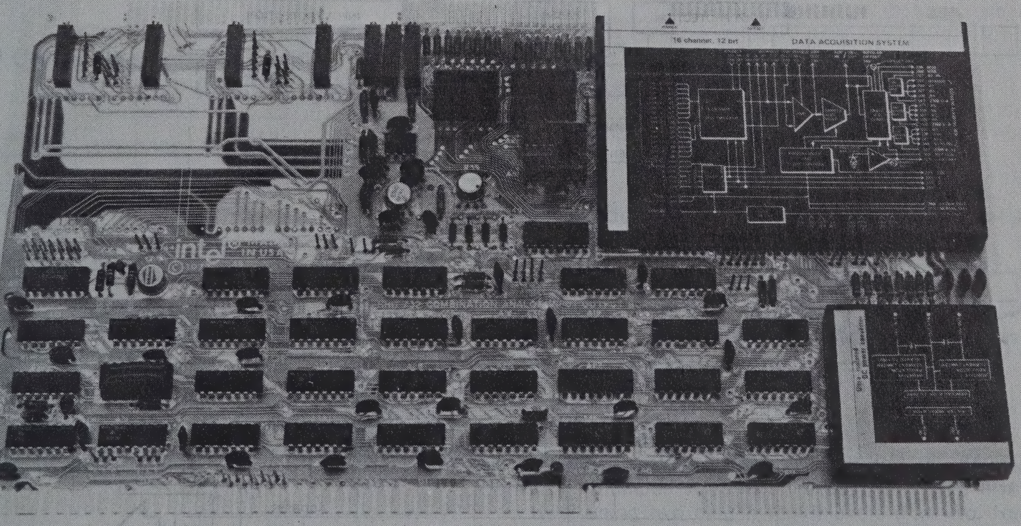
Programmable gain amplifier

12-Bit A/D converter

Memory mapped I/O

Single +5V supply

The iSBC 711 Analog Input Board is a complete single board input subsystem which allows easy interfacing of high level analog input signals to Intel's complete line of iSBC 80 single board computers. The iSBC 711 performs the basic functions of data acquisition of analog input signals under microprocessor control. The iSBC 711 consists of 8 differential/16 single ended channel multiplexer, input protection circuits, programmable gain amplifier, sample and hold amplifer, 12-bit A/D converter, DC to DC converter, memory mapped interface, and control logic.



FUNCTIONAL DESCRIPTION

The iSBC 711 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the iSBC 732 Analog Combination I/O Board. A block diagram of the iSBC 711 Analog Input Board is shown in Figure 1.

Input Capacity

The iSBC 711 contains an 8 differential or 16 single ended analog input multiplexer. Optionally, the iSBC 711 can be expanded up to 16 differential or 32 single ended, non-isolated input channels via two plug-in multiplexers (Part No. Harris H1818A).

Fault Protection

All input channels are protected up to ±28V via diode clamping, together with fusible current limit resistors, limiting potentially destructive overloads under fault conditions.

Current Loop Input

The differential input channels have provisions for up to 16 user supplied 250-ohm resistors to accept 4 to 20 mA current loop inputs.

Programmable Gain Amplifier

The programmable gain amplifier allows gains of 1, 2, 4, and 8 to be specified under program control.

12-Bit A/D Converter

The A/D converter is a 12-bit 35 μs successive approximation device with sample and hold amplifier which can be jumper selected for 0 to +5V, 0 to +10V, ±5V, and ±10V input ranges. A/D conversion can be initiated by external trigger, pacer clock, or programmed I/O. Interrupt on conversion or end of scan is a standard feature. The external trigger is useful when the A/D conversion is to be synchronized to some external event. The internal pacer clock (10 ranges jumper selectable from 976 μs to 1 sec) allows precise, evenly spaced A/D conversions where signal reconstruction is required.

OPERATIONAL DESCRIPTION

Analog Input

The iSBC 711 has three modes of operation for acquisition of analog inputs. These are:

1. Repetitive single channel input
2. Sequential input scan
3. Random channel input

Repetitive Single Channel Input — The channel is selected by a write to the multiplexer address register (MAR). The initiation of the first conversion is stated by a write to the command register (CR). Setting the appropriate bits in the command register allows stop/start, pacing, external trigger. Subsequent conversions are initiated by read of the A/D register (ADCR), or by another write to the command register.

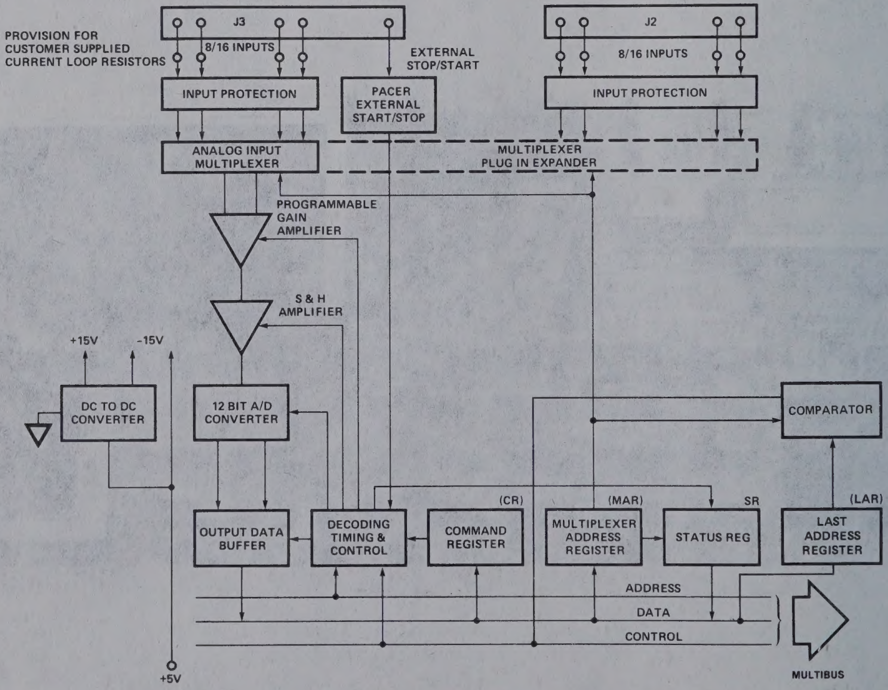

PROVISION FOR CUSTOMER SUPPLIED CURRENT LOOP RESISTORS
J3
8/16 INPUTS
EXTERNAL STOP/START
J2
8/16 INPUTS
INPUT PROTECTION
PACER EXTERNAL START/STOP
INPUT PROTECTION
ANALOG INPUT MULTIPLEXER
MULTIPLEXER PLUG IN EXPANDER
PROGRAMMABLE GAIN AMPLIFIER
S & H AMPLIFIER
+15V
-15V
DC TO DC CONVERTER
12 BIT A/D CONVERTER
COMPARATOR
(CR)
(MAR)
SR
(LAR)
OUTPUT DATA BUFFER
DECODING TIMING & CONTROL
COMMAND REGISTER
MULTIPLEXER ADDRESS REGISTER
STATUS REG
LAST ADDRESS REGISTER
ADDRESS
DATA
CONTROL
MULTIBUS
+5V

Figure 1. iSBC 711 Analog Input Board Block Diagram

Sequential Input Scan — This mode is initiated in the same manner as the repetitive single channel, except bit 1 of the command register (CR) is set to a "1" on the write command.

Random Input Scan — This mode is initiated in the same manner as repetitive single channel input; subsequent channels are selected by a write to the multiplexer address register (MAR) before a read of the current converted value from the ADCR register.

Addressing

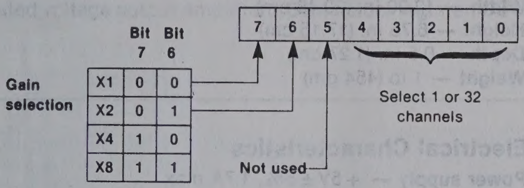
The iSBC 711 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the iSBC 711 interfaces as memory, any of the 8080's 16-bit memory reference instructions can be used. The A/D converter is addressed as memory: base plus specific address. The base address is factory set at F700H and is jumper selectable. Table 1 shows address:

Address	Command	Function
Base +0	Write	Write to command register
Base +0	Read	Read status register
Base +1	Write	Write to multiplexer address register
Base +1	Read	Read multiplexer address register
Base +2	Write	Write to last channel register
Base +3	Write	Clear interrupts
Base +4	Read	Read LS byte of A/D data
Base +5	Read	Read MS byte of A/D data

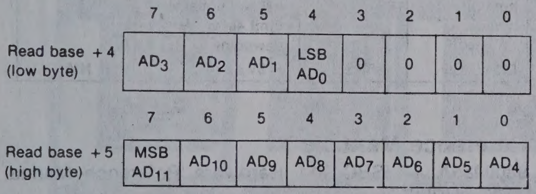
Table 1. Address Commands and Functions

SPECIFICATIONS

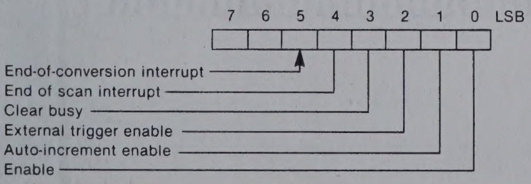
Multiplexer Address Register (MAR) (Write Base +1)


7 6 5 4 3 2 1 0
Bit 7
Bit 6
Gain selection
X1 0 0
X2 0 1
X4 1 0
X8 1 1
Select 1 or 32 channels
Not used

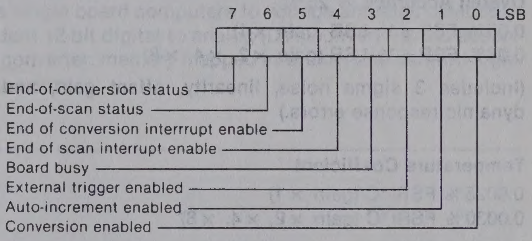
A/D Converter Register (ADCR)


7 6 5 4 3 2 1 0
Read base +4 (low byte)
AD_3 AD_2 AD_1 LSB AD_0 0 0 0 0
7 6 5 4 3 2 1 0
Read base +5 (high byte)
MSB AD_{11} AD_{10} AD_9 AD_8 AD_7 AD_6 AD_5 AD_4

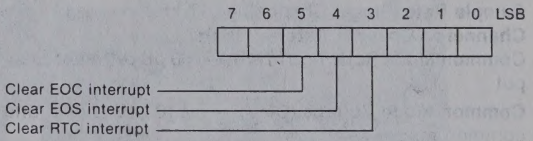
Command Register (CR) (Write Base +0)


7 6 5 4 3 2 1 0 LSB
End-of-conversion interrupt
End of scan interrupt
Clear busy
External trigger enable
Auto-increment enable
Enable

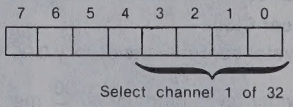
Status Register (Read Base +0)


7 6 5 4 3 2 1 0 LSB
End-of-conversion status
End-of-scan status
End of conversion interrrupt enable
End of scan interrupt enable
Board busy
External trigger enabled
Auto-increment enabled
Conversion enabled

Clear Interrrupt (Write Base +3)


7 6 5 4 3 2 1 0 LSB
Clear EOC interrupt
Clear EOS interrupt
Clear RTC interrupt

Last Address Register (LAR) (Write Base +2)


7 6 5 4 3 2 1 0
Select channel 1 of 32

Analog Input

Number of Input Channels — 8 differential or 16 single-ended (jumber selectable); expandable from 8/16 to 16/32 using two plug-in multiplexers (Part No. Harris H1818A).

Resolution — 12 bit bipolar or unipolar
Sample and Hold Aperture Time — <20 ns
Sample and Hold Uncertainty — 5 ns
Multiplexer Input Voltage Ranges

Gain X	A/D Input Range				Jumper selectable
	+ 5V	+ 10V	± 5V	± 10V	
1	+ 5V	+ 10V	± 5V	± 10V	Programmable
2	+ 2.5V	+ 5V	± 2.5V	± 5V	
4	1.25V	+ 2.5V	± 1.25V	± 2.5V	
8	0.625V	+ 1.25V	± 0.625V	± 1.25V	

Input Impedence
Power Off: 680 ohms
Power On: >100M ohms

Input Current Range — 0-20 mA using 250-ohm user installed resistors

Source Impedance
Balanced: <5000 ohms
Unbalanced: <1000 ohms

Overall Accuracy @ 25°C
0.05% FSR ± ½ LSB (gain × 1)
0.07% FSR ± ½ LSB (gain × 2, × 4, × 8)

(Includes 3 sigma noise, linearity, offset gain, and dynamic response errors.)

Temperature Coefficient
0.0025% FSR/°C (gain × 1)
0.0030% FSR/°C (gain × 2, × 4, × 8)

A/D Conversion Speed — 28 kHz

Throughput

Sample Rate (Single Channel) — 17 kHz

Channel to Channel Rate — 16kHz

Common Mode Rejection (CMR) — 60 dB differential input

Common Mode Voltage (CMV) — ± 10.24V (signal and common mode)

Input Over-Voltage Protection — ± 28V DC, peak AC continuous

External Trigger — TTL compatible, 1.5 μs (min) better than 50 ns risetime

Pacer Clock

Crystal controlled accuracy 0.05%

Divider gives range of $\frac{1000}{2^n}$ ms

n = 0 through 10

Connectors

Interface	Pins (qty)	Centers in.	Centers cm	Mating Connectors
P1 iSBC Bus	86	0.156		Viking 3KH43/9AMK12
P2 ± 15V Auxiliary power	60	0.1		
J1 Not used	50	0.1		3M3415-000 or TIH312125
J2 1st 8/16 input channels	50	0.1		3M3415-000 or TIH312125
J3 Expander 8/16 input channels	50	0.1		3M3415-000 or TIH312125

Compatible Boards and Systems

iSBC 80/05
iSBC 80/10
iSBC 80/20
System 80/10, and
System 80/20-4

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.5 in. (1.27 cm)
Weight — 1 lb (454 gm)

Electrical Characteristics

Power supply — + 5V ± 5%, 1.7A max

Environmental Characteristics

	Reference Operating Conditions	Operative Limits	Transportation and Storage Limits
Temperature	25 ± 0.2°C	0 to 55°C	− 25 to 85°C
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	+ 5V ± 5%	+ 5V ± 5%	N/A

Reference Manuals

9800485A — iSBC 711 Hardware Reference Manual (NOT SUPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 711	Analog Input Board

iSBC 724
ANALOG OUTPUT BOARD

Compatible with iSBC 80 series and MULTIBUS bus

Four independent 12-bit D/A converters

Short circuit protection on voltage output

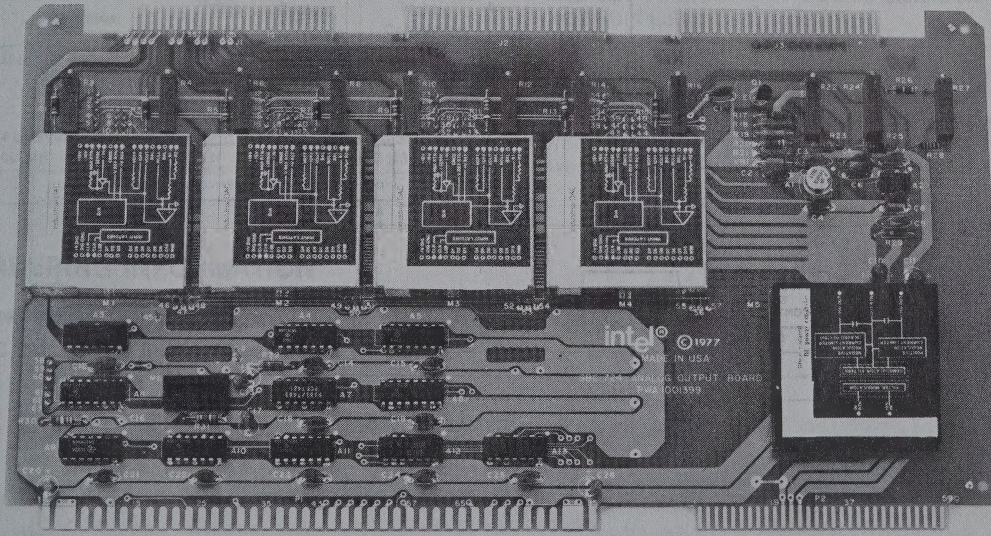
Memory mapped I/O

Accuracy: 0.05% FSR

Unipolar or bipolar with 0 to +10V, 0 to +5V, ±10V ranges

Single +5V supply

The iSBC 724 Analog Output Board is a complete single board analog output subsystem which allows easy interfacing of analog outputs from Intel's complete line of iSBC 80 series single board computers to voltage actuated devices or control elements. The iSBC 724 board contains four independent 12-bit digital to analog (D/A) converters and associated voltage output amplifiers, 8-bit holder register, DC to DC converter, memory mapped interface, and controil logic.



FUNCTIONAL DESCRIPTION

The iSBC 724 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the analog output provided on the iSBC 732 analog I/O board. Each individual D/A converter can be jumper selected for 0 to + 5V, 0 to + 10V, ± 5V, ± 10V. Short circuit protection for voltage outputs is a standard feature suitable for many display and control applications. A block diagram of the iSBC 724 analog output board is shown in Figure 1.

OPERATIONAL DESCRIPTION

Data Transfer

Data transfer to a 12-bit D/A converter is accomplished by a write of the least significant 4 bits to the holding register. When the 8 remaining bits of the upper byte are transferred, the 12 bits of data are immediately loaded into the specific D/A converter channel.

Addressing

The iSBC 724 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the iSBC 724 interfaces as memory, any of the 8080's memory reference instructions can be used. Each independent D/A converter is addressed as memory; base plus specific address. The base address is factory set at F708H which is jumper selectable. Table 1 shows addressing:

Address	Command	Function
Base + 0	Write	Write to DAC holding register
Base + 1	Write	Write to DAC 0
Base + 2	Write	Write to DAC holding register
Base + 3	Write	Write to DAC 1
Base + 4	Write	Write to DAC holding register
Base + 5	Write	Write to DAC 2
Base + 6	Write	Write to DAC holding register
Base + 7	Write	Write to DAC 3

Table 1. Address Commands and Functions

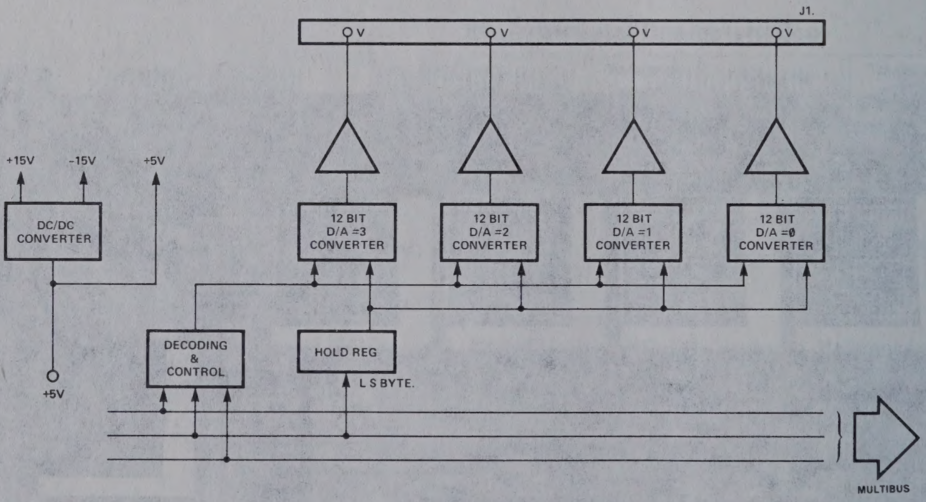
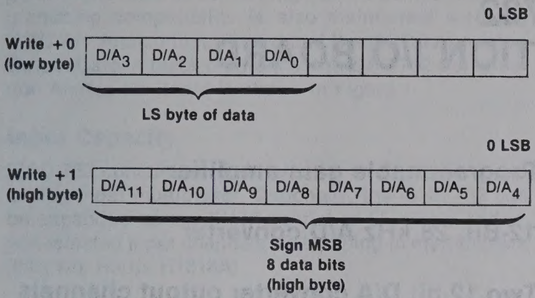


Figure 1. iSBC 724 Analog Output Board Block Diagram

SPECIFICATIONS

Registers



Analog Output

Number of Channels — 4 non-isolated

Resolution — 12 bits bipolar or unipolar (switch selectable)

Voltage Output Characteristics

Voltage Output Ranges — 0 to +5V, 0 to +10V, ±5V, ±10V (jumper selectable)

Output Current — ±5 mA @ ±10V

Output Impedance — 0.2 ohm

Slew Rage — 10V/μs

Accuracy @ 25°C — 0.05% FSR (includes linearity and noise)

Temperature Coefficient — 0.005/°C

Connectors

Interface	Pins (qty)	Centers in.	Centers cm	Mating Connectors
P1 iSBC Bus	86	0.156	0.396	Viking 3KH43/9AMK12
P2 ±15V auxiliary power	60	0.1	0.254	
J1 4 channels of analog output	50	0.1	0.254	3M 3415-000 or TI H312125

Compatible Boards and Systems

iSBC 80/05
iSBC 80/10
iSBC 80/20
System 80/10
System 80/20-4

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 1 lb, 2 oz (511 gm)

Electrical Characteristics

Power Supply — +5V ±5%, 2.0A max

Environmental Characteristics

	Reference Operating Conditions	Operative Limits	Transportation and Storage
Temperature	25±2.0°C	0 to 55°C	−25 to 85°C
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	+5±5%	+5V±5%	N/A

Reference Manuals

9800486A — iSBC 724 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 724	Analog Output Board

intel®

iSBC 732
ANALOG COMBINATION I/O BOARD

iSBC 80 and MULTIBUS compatible

Up to 16 differential/32 single ended non-isolated inputs

Fault protection on all inputs

Voltage or current loop input/output

Programmable gain amplifier

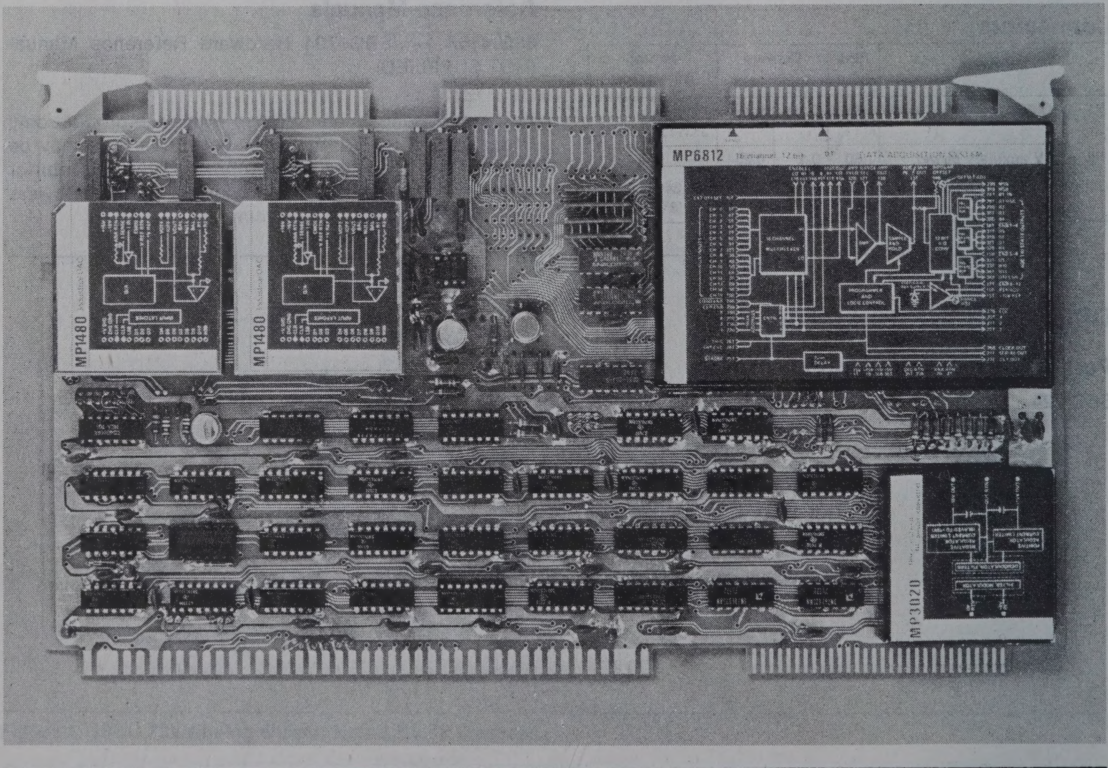
12-Bit, 28 kHz A/D converter

Two 12-bit D/A converter output channels

Memory mapped I/O

Single +5V supply

The iSBC 732 is a complete single board analog input/output subsystem which allows easy interfacing of high level analog input and output signals to Intel's complete line of iSBC 80 series single board computers. The iSBC 732 performs the basic functions of data acquisition of analog inputs and controlled analog output signals under microprocessor control.



FUNCTIONAL DESCRIPTION

The iSBC 732 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the iSBC 711 Analog Input Board and the iSBC 724 Analog Output Card. A block diagram of the iSBC 732 Combination Analog I/O Board is shown in Figure 1.

Input Capacity

iSBC 732 contains an 8 differential or 16 single ended analog input multiplexer. Optionally, the iSBC 732 can be expanded up to 16 differential or 32 single ended, non-isolated input channels via two plug-in multiplexers (Part No. Harris H1818A).

Fault Protection

All input channels are protected up to ±28V via diode clamping, together with fusible current limit resistors, limiting potentially destructive overloads under fault conditions.

Current Loop Input

The differential input channels have provisions for up to 16 user supplied 250-ohm resistors to accept 4 to 20 mA current loop inputs.

Programmable Gain Amplifier

The programmable gain amplifier allows gains of 1, 2, 4, and 8, to be specified under program control.

12-Bit A/D Converter

The A/D converter is a 12-bit, 34 μs successive approximation device with sample and hold amplifier which can be jumper selected for 0 to +5V, 0 to +10V, ±5V and ±10V input ranges. A/D conversion can be initiated by external trigger, pacer clock, or programmed I/O. Interrupt on conversion or end of scan is a standard feature. The external trigger is useful when the A/D conversion is to be synchronized to some external event. The internal pacer clock (10 ranges jumper selectable from 976 μs to 1 sec) allows precise, evenly spaced A/D conversions where signal reconstruction is required.

D/A Converter

The dual 12-bit non-isolated D/A converter can be configured for voltage or current loop outpout. Each D/A converter voltage output can be jumper selected for 0 to +5V, 0 to +10V, ±5V, ±10V, or optionally, 0 to 20 mA current loop output. Short circuit protection for voltage outputs is a standard feature and user supplied compliance voltage of up to 30V make the current loop output suitable for many control applications.

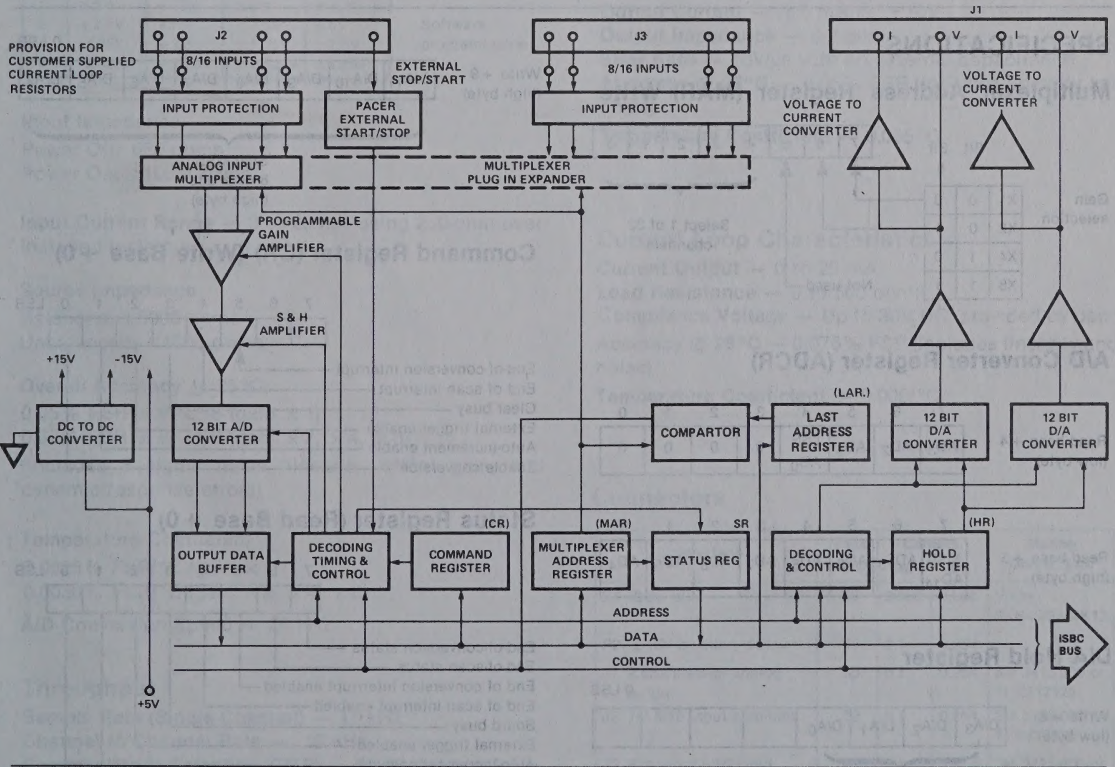

J2
PROVISION FOR CUSTOMER SUPPLIED CURRENT LOOP RESISTORS
8/16 INPUTS
EXTERNAL STOP/START
INPUT PROTECTION
PACER EXTERNAL START/STOP
J3
8/16 INPUTS
INPUT PROTECTION
J1
I
V
I
V
VOLTAGE TO CURRENT CONVERTER
VOLTAGE TO CURRENT CONVERTER
ANALOG INPUT MULTIPLEXER
MULTIPLEXER PLUG IN EXPANDER
PROGRAMMABLE GAIN AMPLIFIER
S & H AMPLIFIER
+15V
-15V
DC TO DC CONVERTER
12 BIT A/D CONVERTER
COMPARTOR
(LAR.)
LAST ADDRESS REGISTER
12 BIT D/A CONVERTER
12 BIT D/A CONVERTER
(CR)
(MAR)
SR
(HR)
OUTPUT DATA BUFFER
DECODING TIMING & CONTROL
COMMAND REGISTER
MULTIPLEXER ADDRESS REGISTER
STATUS REG
DECODING & CONTROL
HOLD REGISTER
ADDRESS
DATA
CONTROL
iSBC BUS
+5V

Figure 1. iSBC 732 Analog Combination I/O Board Block Diagram

OPERATIONAL DESCRIPTION

Analog Input

The iSBC 732 has three modes of operation for acquisition of analog inputs. These are:

1. Repetitive single channel input
2. Sequential input scan
3. Random channel input

Repetitive Single Channel Input — The channel is selected by a write to the multiplexer address register (MAR). The initiation of the first conversion is started by a write command to the command register (CR). Setting the appropriate bits in the command register allow stop/start, pacing, external trigger. Subsequent conversions are initiated by a read command of the A/D register (ADCR).

Sequential Input Scan — This mode is initiated in the same manner as the repetitive single channel, except bit 1 of the command register (CR) is set to a "1" on the write command.

Random Input Scan — This mode is initiated in the same manner as repetitive single channel input. Subsequent channels are selected by a write command to the multiplexer address register (MAR) before a read command of the current converted value from the ADCR register.

Analog Output

Data transfer to a D/A converter is accomplished by a write command of the least significant 4 bits to the holding register. When the upper byte is transferred, the 12 bits of data are immediately loaded to the specific D/A channel.

Addressing

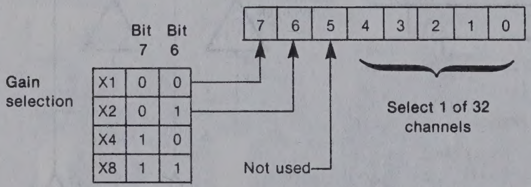
The iSBC 732 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the iSBC 732 interfaces as memory, any of the 8080's memory reference instructions can be used. The A/D and independent D/A converters are addressed as memory: base plus specific address. The base address is set at F700H which is jumper selectable. Table 1 shows addressing.

Address	Command	Function
Base +0	Write	Write to command register
Base +0	Read	Read status register
Base +1	Write	Write to multiplexer address register
Base +1	Read	Read multiplexer address register
Base +2	Write	Write to last channel register
Base +3	Write	Clear interrupts
Base +4	Read	Read LS byte of A/D data
Base +5	Read	Read MS byte of A/D data
Base +8	Write	Write to DAC holding register (low byte)
Base +9	Write	Write to DAC 0 (high byte)
Base +A	Write	Write to DAC holding register (low byte)
Base +B	Write	Write to DAC 1 (high byte)

Table 1. Address Commands and Functions

SPECIFICATIONS

Multiplexer Address Register (MAR) Write


7 6 5 4 3 2 1 0
Bit 7
Bit 6
Gain selection
X1 0 0
X2 0 1
X4 1 0
X8 1 1
Not used
Select 1 of 32 channels

A/D Converter Register (ADCR)

	7	6	5	4	3	2	1	0
Read base +4 (low byte)	AD$_3$	AD$_2$	AD$_1$	LSB AD$_0$	0	0	0	0
Read base +5 (high byte)	MSB AD$_{11}$	AD$_{10}$	AD$_9$	AD$_8$	AD$_7$	AD$_6$	AD$_5$	AD$_4$

D/A Hold Register

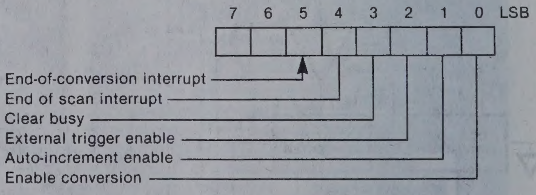
								0 LSB
Write +8 (low byte)	D/A$_3$	D/A$_2$	D/A$_1$	D/A$_0$				

LS byte of data

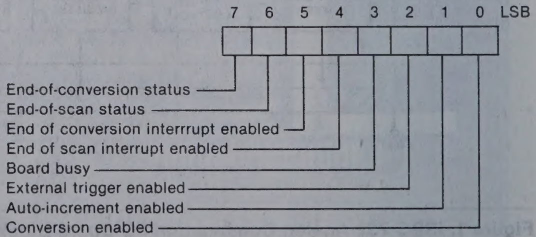
								0 LSB
Write +9 (high byte)	D/A$_{11}$	D/A$_{10}$	D/A$_9$	D/A$_8$	D/A$_7$	D/A$_6$	D/A$_5$	D/A$_4$

Sign MSB
8 data bits
(high byte)

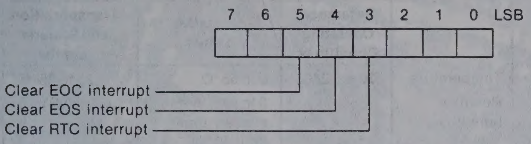
Command Register (CR) (Write Base +0)


7 6 5 4 3 2 1 0 LSB
End-of-conversion interrupt
End of scan interrupt
Clear busy
External trigger enable
Auto-increment enable
Enable conversion

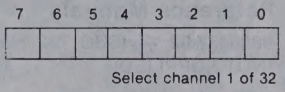
Status Register (Read Base +0)


7 6 5 4 3 2 1 0 LSB
End-of-conversion status
End-of-scan status
End of conversion interrrupt enabled
End of scan interrupt enabled
Board busy
External trigger enabled
Auto-increment enabled
Conversion enabled

Clear Interrrupt (Write Base + 3)



Last Address Register (LAR) (Write Base + 2)



Analog Input

Number of Input Channels — 8 differential or 16 single ended (jumper selectable); expandable from 8/16 to 16/32 using two plug-in multiplexers (Part No. Harris H1818A).

Resolution — 12-bit bipolar or unipolar
Sample and Hold Aperture Time — <20 ns
Sample and Hold Uncertainty — 5 ns
Multiplexer Input Voltage Ranges

Gain X	A/D Input Range			
	+5V	+10V	±5V	±10V
1	+5V	+10V	±5V	±10V
2	+2.5V	+5V	±2.5V	±5V
4	1.25V	+2.5V	±1.25V	±2.5V
8	0.625V	+1.25V	±0.625V	±1.25V

Jumper selectable

Software programmable

Input Impedance
Power Off: 680 ohms
Power On: >100M ohms

Input Current Range — 0 to 20 mA using 250-ohm user installed resistors

Source Impedance
Balanced: <5000 ohms
Unbalanced: <1000 ohms

Overall Accuracy @ 25°C
0.05% FSR ± ½ LSB (gain × 1)
0.07% FSR ± ½ LSB (gain × 2, × 4, × 8)
(Includes 3 sigma noise, linearity, offset gain, and dynamic response errors)

Temperature Coefficient
0.0025% FSR/°C (gain × 1)
0.0030% FSR/°C (gain × 2, × 4, × 8)

A/D Conversion Speed — 28 kHz

Throughput

Sample Rate (Single Channel) — 17 kHz
Channel to Channel Rate — 16 kHz
Common Mode Rejection (CMR) — 60 dB differential input

Common Mode Voltage (CMV) — ±10.24V (signal and common mode)

Input Over-Voltage Protection — ±28V DC, peak AC continuous

External Trigger — TTL compatible, 1.5 μs (min) better than 50 ns risetime

Pacer Clock
Crystal controlled accuracy 0.05%

Divider gives range of $\frac{1000}{2^n}$ ms

n = 0 through 10

Analog Output

Number of Channels — 2 Non-isolated
Resolution — 12 bits bipolar or unipolar (switch selectable)

Voltage Output Characteristics

Voltage Output Ranges — 0 to +5V, 0 to +10V, ±5V, ±10V (jumper selectable)
Output Current — ±5 mA @ ±10V
Output Impedance — 0.2 ohm
Slew Rate — 10V/μs with no external capacitance
Accuracy @ 25°C — 0.05% FSR (includes linearity and noise)
Temperature Coefficient — 0.005°C

Current Loop Characteristics

Current Output — 0 to 20 mA
Load Resistance — 0 to 500 ohms
Compliance Voltage — Up to 30V DC (provided by user)
Accuracy @ 25°C — 0.075% FSR (includes linearity and noise)
Temperature Coefficient — 0.005/°C

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		in.	cm	
P1 iSBC Bus	86	0.156	0.396	Viking 3KH43/9AMK12
P2 ±15V auxiliary power	60	0.1	0.254	
J1 2 channels of analog output	50	0.1	0.254	3M 3415-000 or TI H312125
J2 1st 8/16 input channels	50	0.1	0.254	3M 3415-000 or TI H312125
J3 Expander 8/16 input channels	50	0.1	0.254	3M 3425-000 or TI H312125

Compatible Boards and Systems

iSBC 80/05
iSBC 80/10
iSBC 80/20
System 80/10
System 80/20-4

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.5 in. (1.27 cm)
Weight — 1 lb 4 oz (568 gm)

Electrical Characteristics

Power Supply — +5V ± 5%, 2.3A max

Environmental Characteristics

	Reference Operating Conditions	Operative Limits	Transportation and Storage Limits
Temperature	25 ± 0.2°C	0 to 55°C	−25 to 85°C
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	+5V ± 5%	+5V ± 5%	N/A

Reference Manuals

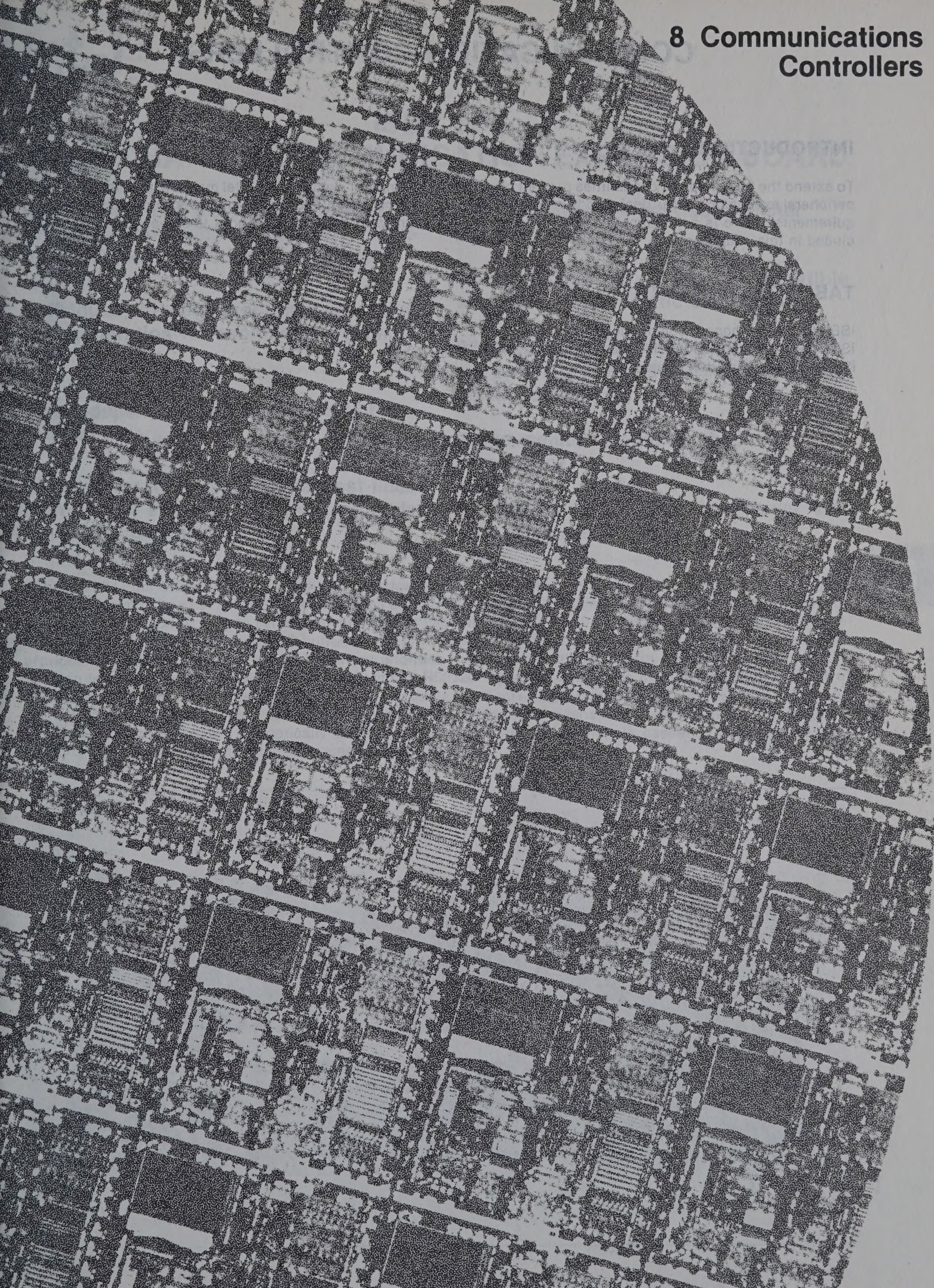
9800487-02 — iSBC 732 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 732	Analog Combination I/O Board

8 Communications Controllers



COMMUNICATION CONTROLLERS

INTRODUCTION

To extend the full computer capabilities present on each iSBC computer even further, Intel makes available a variety of peripheral expansion boards designed to meet the need of those manufacturers having increased communications requirements. There is a 4-channel board, an intelligent communications controller, and a teletypewriter adapter included in this chapter.

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iSBC 544 Intelligent Communications Board 8-6
iSBC 530 Teletypewriter Adapter 8-13

iSBC 534
FOUR CHANNEL COMMUNICATION EXPANSION BOARD

iSBC 80 serial I/O expansion through four programmable synchronous and asynchronous communications channels

Individual software programmable baud rate generation for each serial I/O channel

Two independent programmable 16-bit interval timers

Sixteen maskable interrupt request lines with priority encoded and programmable interrupt algorithms

Jumper selectable interface register addresses

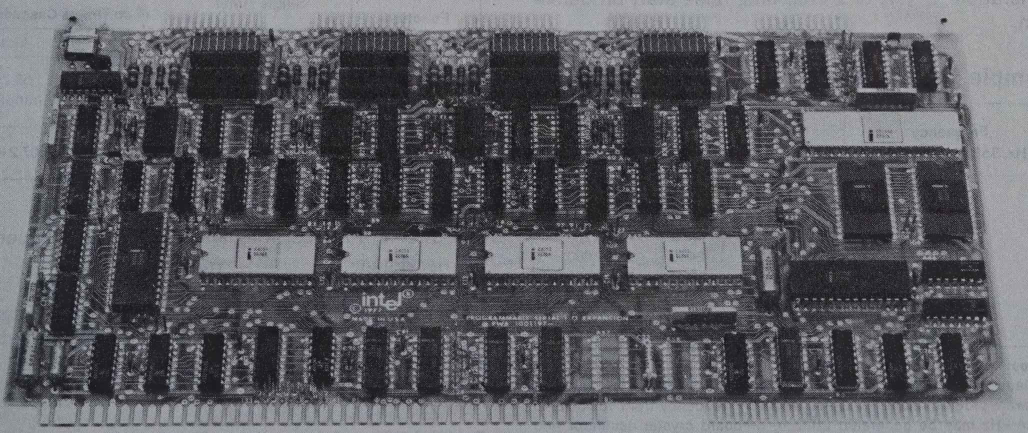
16-Bit parallel I/O interface compatible with Bell 801 automatic calling unit

RS232C/CCITT V.24 interfaces plus 20 mA optically isolated current loop interfaces (sockets)

Programmable digital loopback for diagnostics

Interface control for auto answer and auto originate modems

The iSBC 534 Four Channel Communication Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 534 interfaces directly to any iSBC 80 single board computer via the system bus to provide expansion of system serial communications capability. Four fully programmable synchronous and asynchronous serial channels with RS232C buffering and provision for 20 mA optically isolated current loop buffering are provided. Baud rates, data formats, and interrupt priorities for each channel are individually software selectable. In addition to the extensive complement of EIA Standard RS232C signals provided, the iSBC 534 provides 16 lines of RS232C buffered programmable parallel I/O. This interface is configured to be directly compatible with the Bell Model 801 automatic calling unit. These capabilities provide a flexible and easy means for interfacing iSBC 80 and System 80 based systems to RS232C and optically isolated current loop compatible terminals, cassettes, asynchronous and synchronous modems, and distributed processing networks.



output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus.

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.

Table 2. Interrupt Priority Options

Interrupt Request Generation — As shown in Table 3, interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests (8 total) can be automatically generated by each USART when a character is ready to be transferred to the iSBC 80 system bus (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). Jumper selectable requests can be generated by two of the programmable timers (PITs), and six lines are routed directly from peripherals to accept carrier detect (4 lines), ring indicator, and the Bell 801 present next digit request lines.

Interrupt Request Line	PIC 0	PIC 1
0	PORT 0 R_X RDY	PIT 1 counter 1
1	PORT 0 T_X RDY	PIT 2 counter 2
2	PORT 1 R_X RDY	Ring indicator (all ports)
3	PORT 1 T_X RDY	Present next digit
4	PORT 2 R_X RDY	Carrier detect port 0
5	PORT 2 T_X RDY	Carrier detect port 1
6	PORT 3 R_X RDY	Carrier detect port 2
7	PORT 3 T_X RDY	Carrier detect port 3

Table 3. Interrupt Assignments

Systems Compatibility

The iSBC 534 provides 16 RS232C buffered parallel I/O lines implemented utilizing an Intel 8255 programmable peripheral interface (PPI) configured to operate in mode 0.* These lines are configured to be directly compatible with the Bell 801 automatic calling unit (ACU). This capability allows the iSBC 534 to interface iSBC 80 and System 80-based systems to Bell 801 type ACUs and up to four modems or other serial communications devices. For systems not requiring interface to an ACU, the parallel I/O lines may also be used as general purpose RS232C compatible control lines in system implementation.

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*Complete operational details on the Intel 8251 USART, the Intel 8253 Programmable Interval Timer, the Intel 8255 Programmable Peripheral Interface, and the Intel 8259 Programmable Interrupt controller are contained in the Intel 8080 Microcomputer System User's Manual and 8085 Microcomputer System User's Manual.

SPECIFICATIONS

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Sample Baud Rates[1]

Frequency[2] (kHz, Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Notes:

1. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit programmable interval timer (used here as frequency divider).
2. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

Interval Timer and Baud Rate Generator Frequencies

Input Frequency (On-Board Crystal Oscillator) — 1.2288 MHz ± 10% (0.813 μs period, nominal)

Function	Single Timer		Dual/Timer Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt Interval	1.63 μs	53.3 ms	3.26 μs	58.25 minutes
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.0029 Hz	307.2 kHz

Interfaces — RS232C Interfaces

EIA Standard RS232C Signals provided and supported:

Carrier detect
Clear to send
Data set ready
Data terminal ready
Request to send
Receive clock
Receive data
Ring indicator
Secondary receive data
Secondary transmit data
Transmit clock
Transmit data

Parallel I/O — 8 input lines, 8 output lines, all signals RS232C compatible

Bus — All signals iSBC 80 bus compatible

I/O Addressing

The USART, interval timer, interrupt controller, and parallel interface registers of the iSBC 534 are configured as a block of 16 I/O address locations. The location of this block is jumper selectable to begin at any 16-byte I/O address boundary (i.e., 00H, 10H, 20H, etc.).

I/O Access Time

400 ns	USART registers
400 ns	Parallel I/O registers
400 ns	Interval timer registers
400 ns	Interrupt controller registers

Compatible Connectors/Cable

Interface	Pins (qty)	Centers (in.)	Mating Connectors	Cable
Bus	86	0.156	Viking 3KH43/9AMK12	N/A
Serial and parallel I/O	26	0.1	3M 3462-000 or TI H312113	Intel iSBC 955

Compatible Opto-Isolators

Function	Supplier	Part Number
Driver	Fairchild General Electric Monsanto	4N33
Receiver	Fairchild General Electric Monsanto	4N37

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (398 gm)

Electrical Characteristics

Average DC Current

Voltage	Without Opto-Isolators	With Opto-Isolators[1]
V_{CC} = +5V	1.9 A, max	1.9 A, max
V_{DD} = +12V	275 mA, max	420 mA, max
V_{AA} = −12V	250 mA, max	400 mA, max

Note

1. With four 4N33 and four 4N37 opto-isolator packages installed in sockets provided to implement four 20 mA current loop interfaces.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800450-12 — iSBC 534 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 534	Four Channel Communication Expansion Board

iSBC 544
INTELLIGENT COMMUNICATIONS CONTROLLER

iSBC Communication Controller acting as a single board communications computer or an intelligent slave for communications expansion.

On Board Dedicated 8085A Microprocessor providing communications control and buffer management for four programmable Synchronous/Asynchronous Channels.

Sockets for up to 8K bytes of read only memory.

16K-bytes of dual port dynamic read/write memory with on-board refresh.

Extended Multibus addressing permits iSBC 544 board partitioning into 16K byte segments in a 1-megabyte address space.

Ten programmable parallel I/O lines compatible with Bell 801 Automatic Calling Unit.

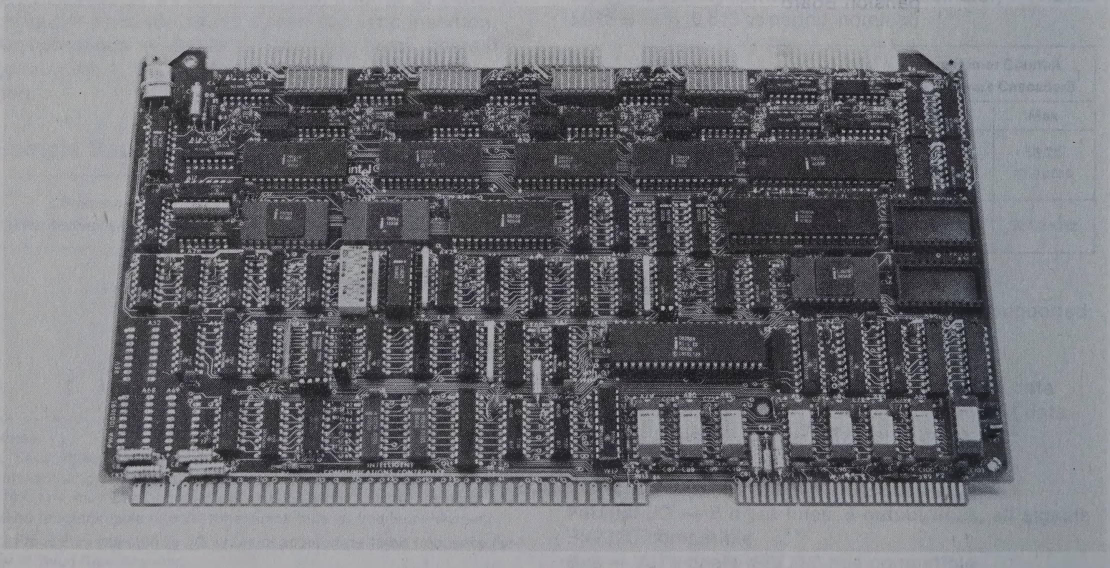
12 levels of programmable interrupt control.

Individual software programmable baud rate generation for each serial I/O channel.

Three independent programmable interval timer/counters.

Interface control for auto answer and auto originate modem.

The iSBC 544 Intelligent Communications Controller is a member of Intel's family of single-board computers, memory, I/O, and peripheral controller boards. The iSBC 544 board is a complete communications controller on a single 6.75 × 12.00 inch printed circuit card. The on-board 8085A CPU may perform local communications processing by directly interfacing with on-board read/write memory, nonvolatile read only memory, four synchronous/asynchronous serial I/O ports, RS366 compatible parallel I/O, programmable timers, and programmable interrupts.



FUNCTIONAL DESCRIPTION

Intelligent Communications Controller

Two Mode Operation — The iSBC 544 board is capable of operating in one of two modes: 1) as a single board communications computer with all computer and communications interface hardware on a single board; 2) as an "intelligent bus slave" that can perform communications related tasks as a peripheral processor to one or more bus masters. The iSBC 544 may be configured to operate as a stand-alone single board communications computer with all MPU, memory and I/O elements on a single board. In this mode of operation, the iSBC 544 may also interface with expansion memory and I/O boards (but no additional bus masters). The iSBC 544 performs as an intelligent slave to the bus master by performing all communications related tasks. Complete synchronous and asynchronous I/O and data management are controlled by the on-board 8085A CPU to coordinate up to four serial channels. Using the iSBC 544 as an intelligent slave, multichannel serial transfers can be managed entirely on-board, freeing the bus master to perform other system functions.

Architecture — The iSBC 544 board is functionally partitioned into three major sections: I/O, central computer, and shared dual port RAM memory (Figure 1). The I/O hardware is centered around the four Intel 8251A USART devices providing fully programmable serial interfacing. Included here as well is a 10-bit parallel interface compatible with the Bell 801 automatic calling unit, or equivalent. The I/O is under full control of the on-board CPU and is protected from access by system bus masters. The second major segment of the intelligent communications controller is a central computer, with an 8085A CPU providing powerful processing capability. The 8085A together with on-board EPROM / ROM, static RAM, programmable timers/counters, and program-

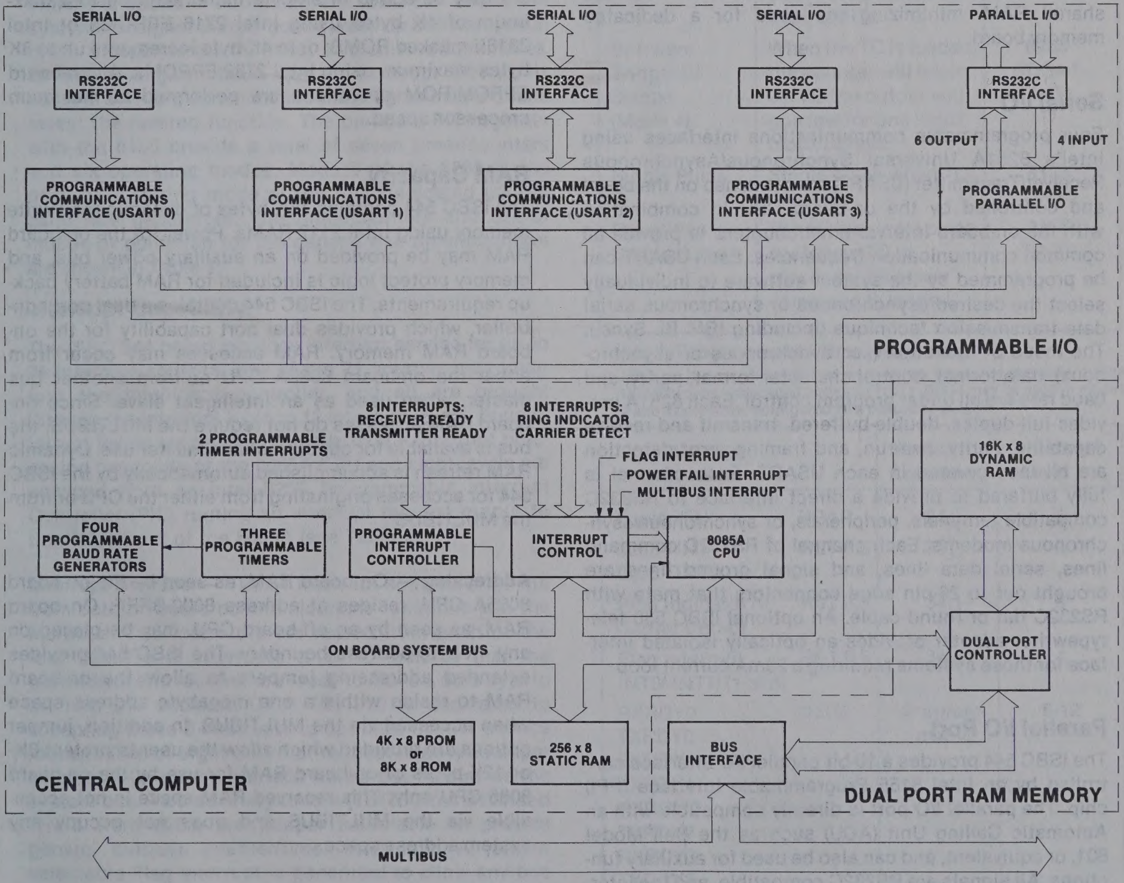

SERIAL I/O
SERIAL I/O
SERIAL I/O
SERIAL I/O
PARALLEL I/O
RS232C INTERFACE
RS232C INTERFACE
RS232C INTERFACE
RS232C INTERFACE
RS232C INTERFACE
6 OUTPUT
4 INPUT
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART 0)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART 1)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART 2)
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART 3)
PROGRAMMABLE PARALLEL I/O
PROGRAMMABLE I/O
2 PROGRAMMABLE TIMER INTERRUPTS
8 INTERRUPTS: RECEIVER READY TRANSMITTER READY
8 INTERRUPTS: RING INDICATOR CARRIER DETECT
FLAG INTERRUPT
POWER FAIL INTERRUPT
MULTIBUS INTERRUPT
16K x 8 DYNAMIC RAM
FOUR PROGRAMMABLE BAUD RATE GENERATORS
THREE PROGRAMMABLE TIMERS
PROGRAMMABLE INTERRUPT CONTROLLER
INTERRUPT CONTROL
8085A CPU
DUAL PORT CONTROLLER
ON BOARD SYSTEM BUS
4K x 8 PROM or 8K x 8 ROM
256 x 8 STATIC RAM
BUS INTERFACE
CENTRAL COMPUTER
DUAL PORT RAM MEMORY
MULTIBUS

Figure 1. iSBC 544 INTELLIGENT COMMUNICATIONS CONTROLLER BLOCK DIAGRAM

mable interrupt control provide the intelligence to manage sophisticated communications operations on-board the iSBC 544 board. The timer/counters and interrupt control are also common to the I/O area providing programmable baud rates to the USARTs and prioritizing interrupts generated from the USARTs. The central computer functions are protected for access only by the on-board 8085A. Likewise, the on-board 8085A may not gain access to the system bus when being used as an intelligent slave. When the iSBC 544 is used as a bus master, the on-board 8085A CPU controls complete system operation accessing on-board functions as well as memory and I/O expansion. The third major segment, dual port RAM memory, is the key link between the iSBC 544 intelligent slave and bus masters managing the system functions. The dual port concept allows a common block of dynamic memory to be accessed by the on-board 8085A CPU and off-board bus masters. The system program can, therefore, utilize the shared dual port RAM to pass command and status information between the bus masters and on-board CPU. In addition, the dual port concept permits blocks of data transmitted or received to accumulate in the on-board shared RAM, minimizing the need for a dedicated memory board.

Serial I/O

Four programmable communications interfaces using Intel's 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) are contained on the board and controlled by the on-board CPU in combination with the on-board interval timer/counters to provide all common communication frequencies. Each USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi. Sync.). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. Each 8251A provides full duplex, double-buffered, transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in each USART. Each channel is fully buffered to provide a direct interface to RS232C compatible terminals, peripherals, or synchronous/asynchronous modems. Each channel of RS232C command lines, serial data lines, and signal ground lines are brought out to 26-pin edge connectors that mate with RS232C flat or round cable. An optional iSBC 530 teletypewriter adapter provides an optically isolated interface for those systems requiring a 20mA current loop.

Parallel I/O Port

The iSBC 544 provides a 10-bit parallel I/O interface controlled by an Intel 8155 Programmable Interface (PPI) chip. The parallel I/O port is directly compatible with an Automatic Calling Unit (ACU) such as the Bell® Model 801, or equivalent, and can also be used for auxiliary functions. All signals are RS232C compatible, and the interface cable signal assignments meet RS366 specifications. For systems not requiring an ACU interface, the parallel I/O port can be used for any general purpose interface requiring RS232C compatibility.

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 544. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of iSBC 544 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory are provided on the iSBC 544 board. Read only memory may be added in 2K-byte increments up to a maximum of 4K bytes using Intel 2716 EPROMs or Intel 2316E masked ROMS; or in 4K-byte increments up to 8K bytes maximum using Intel 2732 EPROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

RAM Capacity

The iSBC 544 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 544 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the on-board 8085A CPU or from another bus master, when used as an intelligent slave. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for concurrent bus master use. Dynamic RAM refresh is accomplished automatically by the iSBC 544 for accesses originating from either the CPU or from the MULTIBUS.

Addressing — On board RAM, as seen by the on-board 8085A CPU, resides at address 8000-BFFF. On-board RAM, as seen by an off-board CPU, may be placed on any 4K-byte address boundary. The iSBC 544 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to protect 8K- or 12K-bytes of on-board RAM for use by the on-board 8085 CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

Static RAM — The iSBC 544 board also has 256 bytes of static RAM located on the Intel 8155 PPI. This memory is only accessible to the on-board 8085A CPU and is located address $7F00_H$-$7FFF_H$.

Programmable Timers

The iSBC 544 board provides seven fully programmable and independent interval timer/counters utilizing two Intel 8253 Programmable Interval Timers (PIT), and the Intel 8155. The two Intel 8253 PITs provide six independent BCD or binary 16-bit interval timer/counters and the 8155 provides one 14-bit binary timer/counter. Four of the PIT timers (BDG0-3) are dedicated to the USARTs providing fully independent programmable baud rates.

Three General Use Timers — The fifth timer (BDG4) may be used as an auxiliary baud rate to any of the four USARTs or may alternatively be cascaded with timer six to provide extended interrupt intervals. The sixth PIT timer/counter (TINT1) can be used to generate interrupt intervals to the on-board 8085A. In addition to the timer/counters on the 8253 PITs, the iSBC 544 has a 14-bit timer available on the 8155 PPI providing a third general use timer/counter (TINT0). This timer output is jumper selectable to the interrupt structure of the on-board 8085A CPU to provide additional timer/counter capability.

Timer Functions — In utilizing the iSBC 544 board, the systems designer simply configures, via software, each timer independently to meet systems requirements. Whenever a given baud rate or interrupt interval is needed, software commands to the programmable timers select the desired function. The on-board PIT together with the 8155 provide a total of seven timer/counters and six operating modes. Mode 3 of the 8253 is the primary operating mode of the four dedicated USART baud rate generators. The timer/counters and useful modes of operation for the general use timer/counters are shown in Table 1.

Interrupt Capability

The iSBC 544 board provides interrupt service for up to 21 interrupt sources. Any of the 21 sources may interrupt the intelligent controller, and all are brought through the interrupt logic to 12 interrupt levels. Four interrupt levels are handled directly by the interrupt processing capability of the 8085A CPU and eight levels are serviced from an Intel 8259 Programmable Interrupt Controller (PIC) routing an interrupt request output to the INTR input of the 8085A (see Table 2).

Interrupt Sources — The 21 interrupt sources originate from both on-board communications functions and the Multibus. Two interrupts are routed from each of the four USARTs (8 interrupts total) to indicate that the transmitter and receiver are ready to move a data byte to or from the on-board CPU. The PIC is dedicated to accepting these 8 interrupts to optimize USART service request. One of eight interrupt request lines are jumper selectable for direct interface from a bus master via the system bus. Two auxiliary timers (TINT0 from 8155 and TINT1 from 8253) are jumper selectable to provide general purpose counter/timer interrupts. A jumper selectable Flag Interrupt is generated to allow any bus master to interrupt the iSBC 544 by writing into the base address of the shared dual port memory accessable to the system. The Flag Interrupt is then cleared by the iSBC 544 when the on-board processor reads the base address. This interrupt provides an interrupt link between

Function	Operation	Counter
Interrupt on Terminal Count (Mode 0)	When terminal count is reached, an interrupt request is generated. This function is useful for generation of real-time clocks.	**8253** TINT1
Rate Generator (Mode 2)	Divide by N counter. The output will go low for one input clock cycle and high for N-1 input clock periods.	**8253** BDG4 *
Square-Wave Rate Generator (Mode 3)	Output will remain high until one-half the TC has been completed, and go low for the other half of the count. This is the primary operating mode used for generating Baud rate clocked to the USARTs.	**8253** BDG0-4 TINT1
Software Triggered Strobe (Mode 4)	When the TC is loaded, the counter will begin. On TC the output will goe low for one input clock period.	**8253** BDG4 * TINT1
Single Pulse	Single pulse when TC reached.	**8155** TINT0
Repetitive Single Pulse	Repetitive single pulse each time TC is reached until a new command is loaded.	**8155** TINT0

Table 1. Programmable Timer Functions

* BDG4 is jumper selectable as an auxiliary baud rate generator to the USARTs or as a cascaded output to TINT1. BDG4 may be used in modes 2 and 4 only when configured as a cascaded output.

Interrupt Source		Vector Location	Interrupt Level
Power Fail	TRAP	24_H	1
8253 TINT1 8255 TINT0	RST 7.5	$3C_H$	2
Ring Indicator (1) Carrier Detect	RST 6.5	34_H	3
Flag Interrupt INT0/-INT7/ (1 of 8)	RST 5.5	34_H	4
RXRDY0 TXRDY0 RXRDY1 TXRDY1 RXRDY 2 TXRDY2 RXRDY3 TXRDY3	INTR	Programmable	5-12

Table 2. Interrupt Vector Memory Locations

(1) Four ring indicator interrupts and four carrier detect interrupts are summed to the RST 6.5 input. The 8155 may be interrogated to inspect any one of the eight signals.

a bus master and intelligent slave (See System Programming). Eight inputs from the serial ports are monitored to detect a ring indicator and carrier detect from each of the four channels. These eight interrupt sources are summed to a single interrupt level of the 8085A CPU. If one of these eight interrupts occur, the 8155 PPI can then be interrogated to determine which port caused the interrupt. Finally, a jumper selectable Power Fail Interrupt is available from the Multibus to detect a power down condition.

8085 Interrupt — Thirteen of the twenty-one interrupt sources are available directly to four interrupt inputs of the on-board 8085A CPU. Requests routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5 and RST 5.5 have a unique vector memory address. An 8085A jump instruction at each of these addresses then provides software linkage to interrupt service routines located independently anywhere in the Memory. All interrupt inputs with the exception of the TRAP may be masked via software.

8259 Interrupts — Eight interrupt sources signaling transmitter and receiver ready from the four USARTs are channeled directly to the Intel 8259 PIC. The PIC then provides vectoring for the next eight interrupt levels. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts transmitter and receiver interrupts from the four USARTs. It then determines which of the incoming requests is of highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. The output of the PIC is applied directly to the INTR input of the 8085A. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. When the 8085A responds to a PIC interrupt, the PIC will generate a CALL instruction for each interrupt level. These addressses are equally spaced at intervals of 4 or 8 (software selectable) bytes. Interrupt response to the PIC is software programmable to a 32- or 64-byte block of memory. Interrupt sequences may be expanded from this block with a single 8085A jump instruction at each of these addresses.

Interrupt Output — In addition, the iSBC 544 board may be jumper selected to generate an interrupt from the on-board serial output data (SOD) of the 8085A. The SOD signal may be jumpered to any one of the 8 MULTIBUS interrupt lines (INT0/-INT7/) to provide an interrupt signal directly to a bus master.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 Power Supply or equivalent.

Expansion Capabilities

When the iSBC 544 board is used as a single board communications controller, memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS™ compatible expansion boards. In this mode, no other bus masters may be configured in the system. Memory may be expanded to a 65K byte capacity by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Furthermore, multiple iSBC 544 boards may be included in an expanded system using one iSBC 544 board as a single board communications computer and additional controllers as intelligent slaves.

System Programming

In the system programming environment, the iSBC 544 board appears as an additional RAM memory module when used as an intelligent slave. The master CPU communicates with the iSBC 544 board as if it were just an extension of system memory. Because the iSBC 544 board is treated as memory by the system, the user is able to program into it a command structure which will allow the iSBC 544 board to control its own I/O and memory operation. To enhance the programming of the iSBC 544 board, the user has been given some specific tools. The tools are: 1) the flag interrupt, 2) an on-board RAM memory area that is accessible to both an off-board CPU and the on-board 8085A through which a communications path can exist, and 3) access to the bus interrupt line.

Flag Interrupt — The Flag Interrupt is generated anytime a write command is performed by an off-board CPU to the base address of the iSBC 544 board's RAM. This interrupt provides a means for the master CPU to notify the iSBC 544 board that it wishes to establish a communications sequence. In systems with more than one intelligent slave, the flag interrupt provides a unique interrupt to each slave outside the normal eight MULTIBUS interrupt lines (INT0/-INT7/).

On-Board RAM — The on-board 16K byte RAM area that is accessible to both an off-board CPU and the on-board 8085A can be located on any 4K boundary in the system. The selected base address of the iSBC 544 RAM will cause a flag interrupt when written into by an off-board CPU.

Bus Access — The third tool to improve system operation as an intelligent slave is access to the Multibus interrupt lines. The iSBC 544 board can both respond to interrupt signals from an off-board CPU, and generate an interrupt to the off-board CPU via the MULTIBUS.

System Development Capability

The development cycle of iSBC 544 board based products may be significantly reduced using the Intellec series microcomputer development systems. The Intellec resident macroassembler, text editor, and system monitor greatly simplify the design, development and debug of iSBC 544 system software. An optional ISIS-II diskette operating system provides a linker, object code locater, and library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 544 board.

SPECIFICATIONS

Serial Communications Characteristics

Synchronous — 5-8 bit characters; automatic sync insertion; parity.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; break character detection.

Baud Rates

Frequency (KHz)[1] (Software Selectable)	Baud Rate (Hz)[2]		
	Synchronous	Asynchronous	
		÷16	÷64
307.2		19200	4800
153.6	——	9600	2400
76.8	——	4800	1200
55.8	55800	3500	870
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	——	110

Notes:

1) Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

2) Baud rates shown here are only a sample subset of possible software programmable rates available. Any frequency from 18.75 Hz to 614.4 KHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as a frequency divider).

8085A CPU

Word Size — 8, 16 or 24 bits/instruction; 8 bits of data

Cycle Time — 1.45/usec ± .1% for fastest executable instruction; i.e. four clock cycles.

Clock Rate — 2.76 MHz ± .1%

System Access Time

Dual port memory — 740 nsec

Note: Assumes no refresh contention

Memory Capacity

On-Board ROM/PROM — 4K, or 8K bytes of user installed ROM or PROM.

On-Board Static RAM — 256 bytes on 8155.

On-Board Dynamic RAM (on-board access) — 16K bytes. Integrity maintained during power failure with user-furnished batteries (optional).

On-Board Dyanmic RAM (MULTIBUS access) — 4K, 8K, or 16K-bytes available to bus by switch selection.

Memory Addressing

On-Board ROM/PROM — 0-0FFF (using 2716 EPROMs or 2316E ROMs); 0-1FFF (using 2732 EPROMs)

On-Board Static Ram — 256 bytes: 7F00-7FFF

On-Board Dynamic RAM (on-board access) — 16K bytes: 8000-BFFF.

On-Board Dynamic RAM (MULTIBUS access) — any 4K increment 00000-FF000 which is switch and jumper selectable. 4K- 8K- or 16K-bytes can be made available to the bus by switch selection.

I/O Capacity

Serial — 4 programmable channels using four 8251A USARTs.

Parallel — 10 programmable lines available for Bell 801 ACU, or equivalent use. Two auxiliary jumper selectable signals.

I/O Addressing

On-Board Programmable I/O

Port	Data	Control
USART 0	D0	D1
USART 1	D2	D3
USART 2	D4	D5
USART 3	D6	D7
8155 PPI	E9 (Port A) EA (Port B) EB (Port C)	E8

Interrupts

Addresses for 8259 Registers (Hex notation, I/O address space)

E6	Interrupt request register
E6	In-service register
E7	Mask register
E6	Command register
E7	Block address register
E6	Status (polling register)

Note: Several registers have the same physical address: Sequence of access and one data bit of the control word determines which register will respond.

Interrupt levels routed to the 8085 CPU automatically vector the processor to unique memory locations:

24	TRAP
3C	RST 7.5
34	RST 6.5
2C	RST 5.5

Timers

Addresses for 8253 Registers (Hex notation, I/O address space)

Programmable Interrupt Timer One

D8	Timer 0	BDG0
D9	Timer 1	BDG1
DA	Timer 2	BDG2
DB	Control register	

Programmable Interrupt Timer Two

DC	Timer 0	BDG3
DD	Timer 1	BDG4
DE	Timer 2	TINT1
DF	Control register	

Address for 8155 Programmable Timer

E8	Control	
EC	Timer (MSB)	TINT0
ED	Timer (LSB)	TINT0

Input frequencies — Jumper selectable reference 1.2288 MHz ± .1% (.814 usec period nominal) or 1.843 MHz ± .1% crystal (0.542 usec period, nominal)

Output Frequencies (at 1.2288 MHz)

Function	Single timer/counter		Dual timer/counter (two timers cascaded)	
	Min	Max	Min	Max
Real-time interrupt interval	1.63 usec	53.3 usec	3.26 usec	58.25 min
Rate Generator (frequency)	18.75 Hz	614.4 KHz	0.00029 Hz	307.2 KHz

Interfaces

Serial I/O — EIA Standard RS232C signals provided and supported:

Carrier Detect
Clear to Send
Data Set Ready
Data Terminal Ready
Request to Send
Receive Clock
Receive Data
Ring Indicator
Secondary Receive Data *
Secondary Transmit Data *
Transmit Clock
Transmit Data
DTE Transmit Clock

* Optional if parallel I/O port is not used as Automatic Calling Unit.

Parallel I/O — Four inputs and eight outputs (includes two jumper selectable auxiliary outputs). All signals compatible with EIA Standard RS232C. Directly compatible with Bell Model 801 Automatic Calling Unit, or equivalent.

MULTIBUS — Compatible with iSBC MULTIBUS.

On-Board Addressing

All communications to the parallel and serial I/O ports, to the timers, and to the interrupt controller, are via read and write commands from the on-board 8085A CPU.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during the system power-down sequences.

Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	15
Commands	Tri-state	32

Note: Used as a master in the single board communications computer mode.

Physical Characteristics

Width: 30.48 cm (12.00 inches)
Depth: 17.15 cm (6.75 inches)
Thickness: 1.27 cm (0.50 inch)
Weight: 3.97 gm (14 ounces)

Electrical Characteristics

DC Power Requirements

Configuration	Current Requirements			
	$V_{CC} = +5V$ ± 5% (max)	$V_{DD} = \pm 12V$ ± 5% (max)	$V_{BB} = -5V$(3) ± 5% (max)	$V_{AA} = -12V$ ± 5% (max)
With 4K EPROM (using 2716)	$I_{CC} = 3.4$ max max	$I_{DD} = 350mA$ max	$I_{BB} = 5mA$ max	$I_{AA} = 200mA$ max
Without EPROM	3.3A max	350 mA max	5 mA max	200 mA max
RAM only (1)	390 mA max	176 mA max	5 mA max	—
RAM(2) refresh only	390 mA max	20 mA max	5 mA max	

Notes: 1. For operational RAM only, for AUX power supply rating.
2. For RAM refresh only. Used for battery backup requirements. No RAM accessed.
3. V_{BB} is normally derived on-board from V_{AA}, eliminating the need for a V_{BB} supply. If it is desired to supply V_{BB} from the bus, the current requirement is as shown.

Environmental Characteristics

Operating Temperature: 0 °C to 55 °C (32 °F to 131 °F)
Relative Humidity: To 90% without condensation

Reference Manual

9800616B — iSBC 544 Intelligent Communication Controller Board Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 544	Intelligent Communications Controller

intel®

iSBC 530
TELETYPEWRITER ADAPTER

Compact, easily mounted package with standard connectors

Compatibility with iSBC 80 and iSBC 86 Single Board Computers

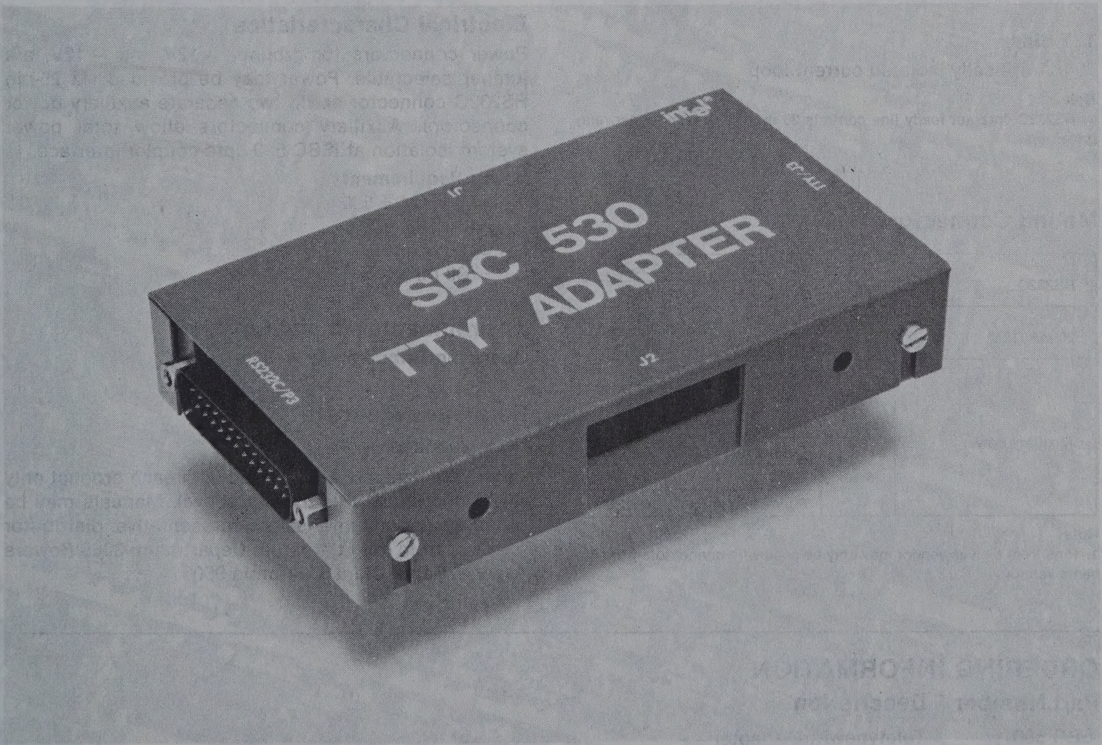
Compatibility with iSBC 80 combination boards

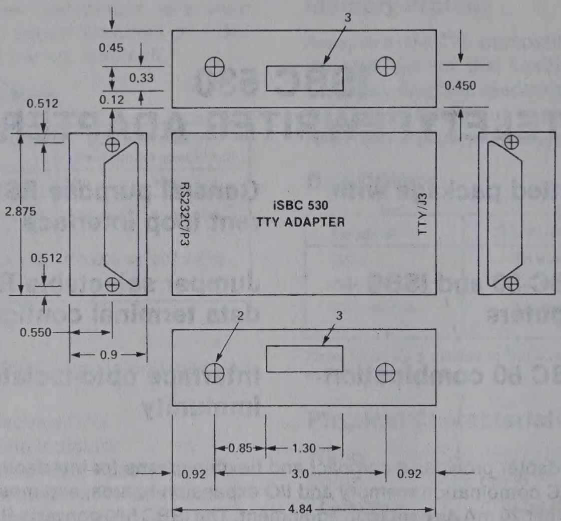
General purpose RS232C to 20 mA current loop interface

Jumper selectable RS232C data set or data terminal configuration

Interface opto-isolated for high noise immunity

The iSBC 530 Teletypwriter Adapter provides a compact and flexible means for interfacing Intel iSBC 80 and iSBC 86 Single Board Computers, iSBC combination memory and I/O expansion boards, and most RS232C compatible equipment to teletypewriters and other 20 mA current loop equipment. The iSBC 530 converts RS232C signal levels to an optically isolated 20 mA current loop interface. The iSBC 530 provides signal translation for transmitted data (Txd), received data (RcD), and a teletypewriter paper tape reader relay. The RS232C interfaces are jumper selectable, and may be configured to accept signals from an RS232C data terminal or data set. Threaded holes have been incorporated in the iSBC 530 for ease in system chassis design and multiple units may be mounted together to support multiple serial channels. The units are mountable in any of three planes. When used with an iSBC Single Board Computer, power is provided to the iSBC 530 directly through its RS232C connector. Power may also be provided through either of two auxiliary power connectors for standard current loop interfacing. The noise immunity benefits of total intersystem power isolation may be achieved through the use of both auxiliary power connectors on the iSBC 530.





NOTES: 1. ALL DIMENSIONS IN INCHES.
2. ALL FOUR MOUNTING HOLES THREADED FOR 6-32 MACHINE SCREWS.
3. CUTOUTS FOR AUXILIARY POWER CONNECTORS

Figure 1. iSBC 530 Dimensions

SPECIFICATIONS

Interface Characteristics

RS232C Side

RS232C signal levels in/out[1]

TTY Side

20 mA optically isolated current loop

Note

1. RS232C data set ready line controls 20 mA paper tape reader relay driver line.

Mating Connectors

RS232C	Cinch		DB-25S
	ITT Cannon		DB-25S
20 mA (TTY)	Cinch		DB-25P
	ITT Cannon		DB-25P
Auxiliary power	AMP	Connector	87159-7
		Pin	87023-1
		Polarizing key	87116-2
	Molex	Connector	09-50-7071
		Pin	08-50-0106
		Polarizing key	15-04-0219

Note

1. Pins from a given vendor may only be used with connectors from the same vendor.

Physical Characteristics

Width — 2.876 in. max (7.31 cm)
Height — 4.850 in. max (12.32 cm)
Depth — 0.920 in. max (2.34 cm)
Weight — 9 oz (255.4 gm)

Electrical Characteristics

Power connectors for ground, +12V and −12V, are jumper selectable. Power may be provided via 25-pin RS232C connector or via two separate auxiliary power connectors. Auxiliary connectors allow total power system isolation at iSBC 530 opto-coupler interface.

Power Requirements

V_{DD} = +12V ±5%
V_{AA} = −12V ±5%
I_{DD} = 98 mA max
I_{AA} = 98 mA max

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

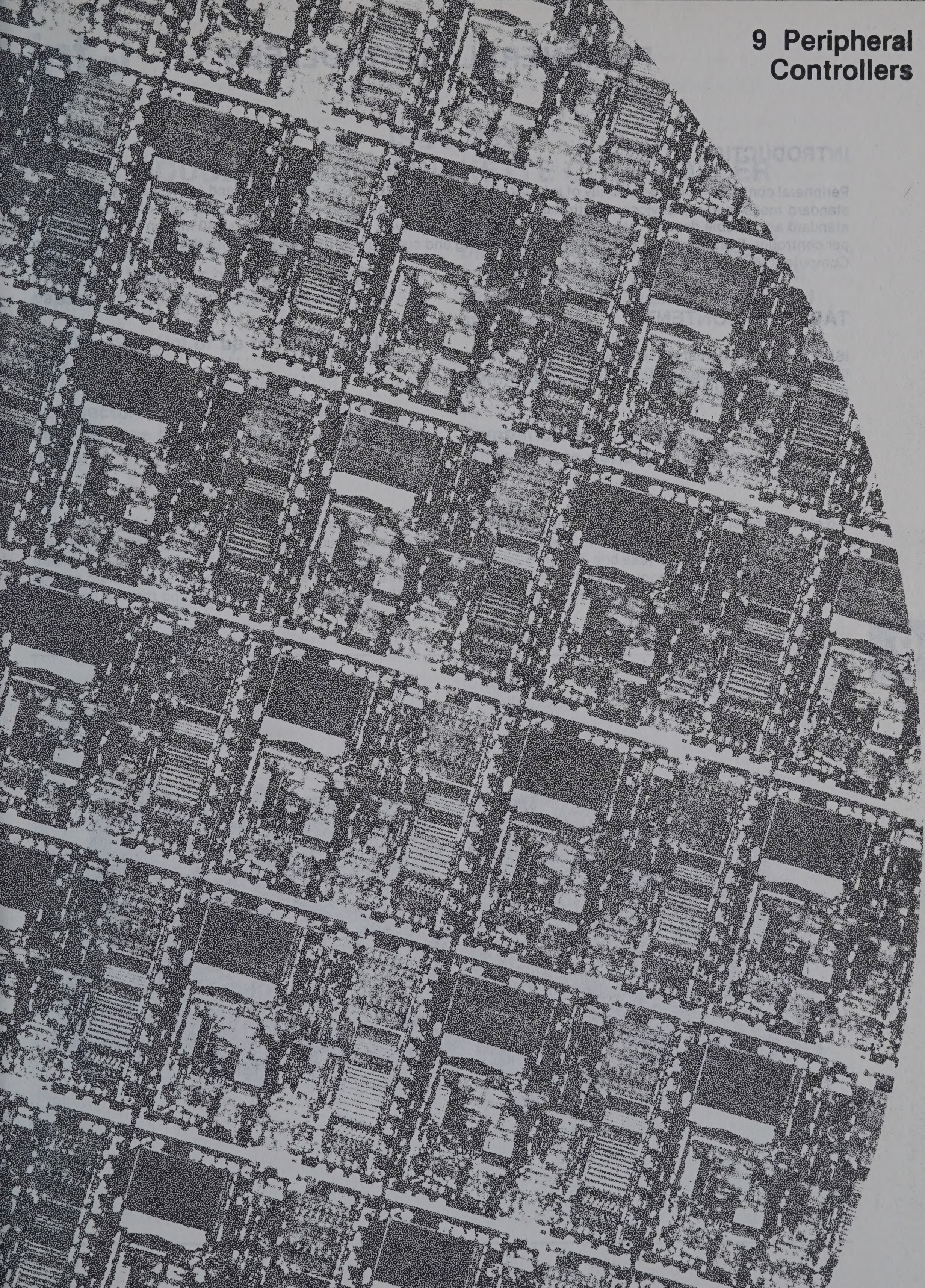
None supplied.

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 530	Teletypewriter adapter

9 Peripheral Controllers



PERIPHERAL CONTROLLERS

INTRODUCTION

Peripheral controllers provide a family of interfaces between the MULTIBUS system bus and a wide variety of industry-standard mass memory devices. Controllers are available for rotating storage ranging from mini-diskettes through standard and double density diskette drives up to 5440 type drives, providing as much as 40 million bytes of storage per controller. Features include disk/diskette formatting and complete software support for the iSBC 80 Single Board Computers through RMX/80.

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iSBC 202
DOUBLE DENSITY DISKETTE CONTROLLER

iSBC 80 compatible interface, control and DMA logic for high speed, high capacity random access bulk storage

Provides control of up to four flexible diskette drives

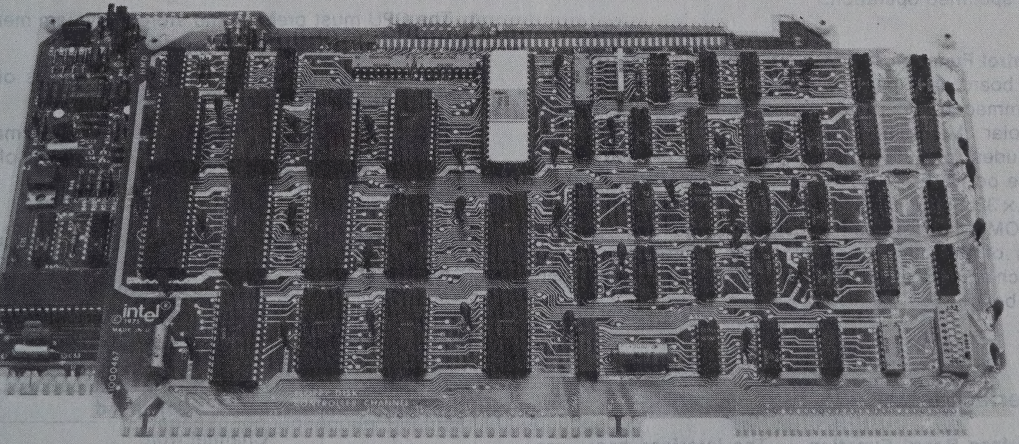
Soft-sectored format allows 500K-byte data storage capacity per double density diskette

DMA channel allows single board computer to process in parallel with block transfer between diskettes and memory

Complete CRC data checking

Compatible with Shugart SA 800-1 and other double density diskette drives

The iSBC 202 Double Density Diskette Controller is an interface between the MULTIBUS system bus and double density flexible diskette drives via a direct bus interface. Designed with Intel's powerful 3000 Series of microprogrammable bit-slice microprocessors, the iSBC 202 provides a high speed, efficient, and easy to use high capacity random access bulk storage interface to Intel's family of single board computers. Software support for the iSBC 80 Series of 8-bit single board computers is provided through RMX/80, the Real-Time Multitasking Executive.



FUNCTIONAL DESCRIPTION

The iSBC 202 Double Density Diskette Controller provides an easy to use interface for OEM use of Intel single board computers and other manufacturers' flexible diskette drives. All DMA logic is provided so no additional boards or circuitry are required, and up to four double density flexible diskette drives may be interfaced with each iSBC 202. The controller facilitates recording of all data in soft-sector format. The controller consists of two boards which may reside in System Chassis, the iSBC 604 or 614 Modular Cardcage/Backplane, or in an OEM custom designed iSBC 80 bus-compatible with a majority of double density specified flexible diskette drives. The microprogrammed track format consists of 52 records with 128 bytes per record. The Shugart SA 800-1 drive is fully compatible with this dense track format due to its "straddle-erase" magnetic head. Use of other manufacturers' flexible disk drives is accommodated also, with the limitation that after any "write data" operation, the CPU must delay 500 μs before issuing another read or write command (due to the "delayed-erase" magnetic head). Therefore, use of multi-sector "write data" commands is only possible with the SA 800-1 drive.

Channel Board

Channel Board Function — The channel board is the primary control module within the diskette controller. It receives, decodes, and responds to channel commands from the central processor unit (CPU) on the Intel iSBC single board computer. The channel board can access a block of system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

Control Function — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512×32 bit of 3604 programmable read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the channel board.

Interface Board

Interface Board Function — The interface board provides the iSBC 202 Double Density Diskette Controller with a means of communicating with the diskette drives, as well as with the system bus. Under control of the microprogram being executed on the channel board, the interface board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The interface board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board. The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write dta, write deleted data, read data, and verify CDC.

Write Operations — During write operations, the interface board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

Memory Operations — When the diskette controller requires access to the system memory, the interface board requests and maintains DMA transfer control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the MULTIBUS system bus.

Programming Capability

IOPB Function — The I/O Parameter Block (IOPB) has been designed to allow simplified I/O programming where necessary, and to facilitate a high level of sophistication in system-level I/O drivers in more complex systems. All diskette operations are initiated by an Intel single board computer with standard I/O commands. Once initiated, however, the diskette controller completes the specified operation without further intervention on the part of the CPU. Only three general steps are performed by the CPU to complete any diskette operation:

1. The CPU must prepare and store in system memory an IOPB for each operation to be performed.
2. The CPU then passes the memory address of the IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation.

IOPB Format — In preparing the IOPB, the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared, utilizing the following format for the 7-byte parameter block:

Byte	Command
1	Channel word
2	Diskette instruction
3	Number of records
4	Track address
5	Sector address
6	Buffer address (lower)
7	Buffer address (upper)

SPECIFICATIONS

Media

Flexible diskette
One recording surface
77 tracks/diskette
52 sectors/track
128 bytes/sector

Physical Characteristics

Mounting — Occupies two slots of System 80 chassis or iSBC 604/614 cardcage

Height — 6.75 in. (17.15 mm)
Width — 12.00 in. (30.48 mm)
Depth — 0.50 in. (1.27 mm)

Electrical Characteristics

DC Power Requirements

Channel Board: 5V @ 3.75A typ, 5A max

Interface Board: 5V @ 1.5A typ, 2.5A max; −5V @ 0.1A typ, 0.2A max

Environmental Characteristics

Temperature

Operating: 0°C to 55°C
Non-Operating: −55°C to +85°C

Humidity

Operating: Up to 90% relative humidity without condensation

Non-Operating: All conditions without condensation of water or frost

Equipment Supplied

DDFDC channel board
DDFDC interface board
Dual auxiliary board connector (P2 socket)

Reference Manuals

9800420 — iSBC 202 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 202	Double Density Diskette Controller

intel®

iSBC 204
UNIVERSAL FLEXIBLE DISKETTE CONTROLLER

Full compatibility with iSBC 80 and iSBC 86 Single Board Computers

Direct compatibility with most single-density, soft-sectored standard- and mini-size flexible diskette drives

Software supported by RMX/80 Real-Time Multitasking Executive disk file system

DMA input/output allows single board computers to process in parallel with diskette transfer operations

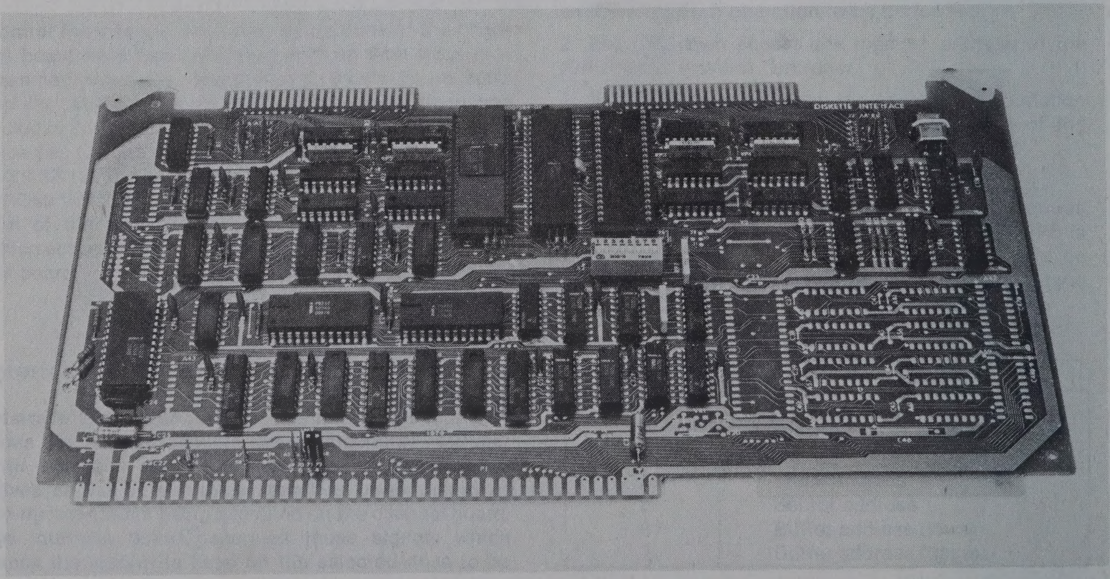
Programmable track-to-track access, head-settling, and head-load times

On-board data separation logic

Read, write, verify, and search on single or multiple sectors

Single +5V supply

The Intel iSBC 204 Universal Flexible Diskette Controller is a single board universal diskette controller capable of supporting virtually any software-sectored, single density diskette drive. The standard iSBC 204 Controller can control two drive surfaces (two single sided drives or one doubled sided drive). With the addition of a second (optional) Intel 8271 circuit, up to four drives can be supported. In addition to the standard IBM 3740 formats, the controller supports sector lengths of up to 4096 bytes plus mini-size drive formats. The iSBC 204's wide range of drive compatibility is achieved without compromising performance. The operating characteristics (track-to-track access, head-load, and head-settling times) are specified under user program control. The controller can read, write, verify, and search either single or multiple sectors.



FUNCTIONAL DESCRIPTION

Intel's 8271 Floppy Disk Controller (FDC) circuit is the heart of the iSBC 204 Controller. On-board data separation logic performs standard FM encoding and decoding, obviating external separation circuitry at the drive. Diskette data transfers are DMA (direct memory access) through an on-board Intel 8257 DMA controller circuit which manages DMA transfers and signals the master iSBC processor on completion of the transfer. A block diagram of the iSBC 204 Controller is shown in Figure 1.

Universal Drive and MULTIBUS Compatibility

Because the iSBC 204 Controller has universal drive compatibility, it can be used to control virtually any standard- or mini-sized single density diskette drive. Moreover, the iSBC 204 Controller fully supports the microcomputer industry standard MULTIBUS system bus and can be used with any single board computer or system compatible with Intel's bus. Because the iSBC 204 Controller is programmable, its performance is not compromised by its universal drive compatibility. The track-to-track access, head-load, and head-settling characteristics of the selected drive model are program specified. Data may be organized in a fully compatible IBM 3740 sector format, in sectors up to 4096 bytes in length, or in formats compatible with the mini-sized diskette drives.

Interface Characteristics

Expandability — Each standard iSBC 204 Controller includes a single 8271 FDC circuit capable of supporting two drive surfaces. Optionally the iSBC 204 may be expanded to support four single-sided (or two double-sided) drives with the insertion of a second 8271 circuit into an on-board socket.

Simplified Interface — The cables between the iSBC 204 Controller and the drive(s) may be either low cost, flat ribbon cable with mass termination connectors or twisted pair conductors with individually wired connectors. An on-board, cross-connect matrix allows optional drive control and status signals to be connected while maintaining pin-to-pin compatibility.

Programming

The powerful 8271 FDC circuit is capable of executing high-level commands that simplify system software development. The device can read, write, and verify both single and multiple sectors. CRC characters are generated and checked automatically. Up to two tracks on each surface may be designated "bad" and logically removed from the diskette.

Sector Scanning — Scan commands permit sectors to be searched for a specified data pattern or "key". During scan operations the pattern image from memory is continuously compared with a sector or multiple sectors

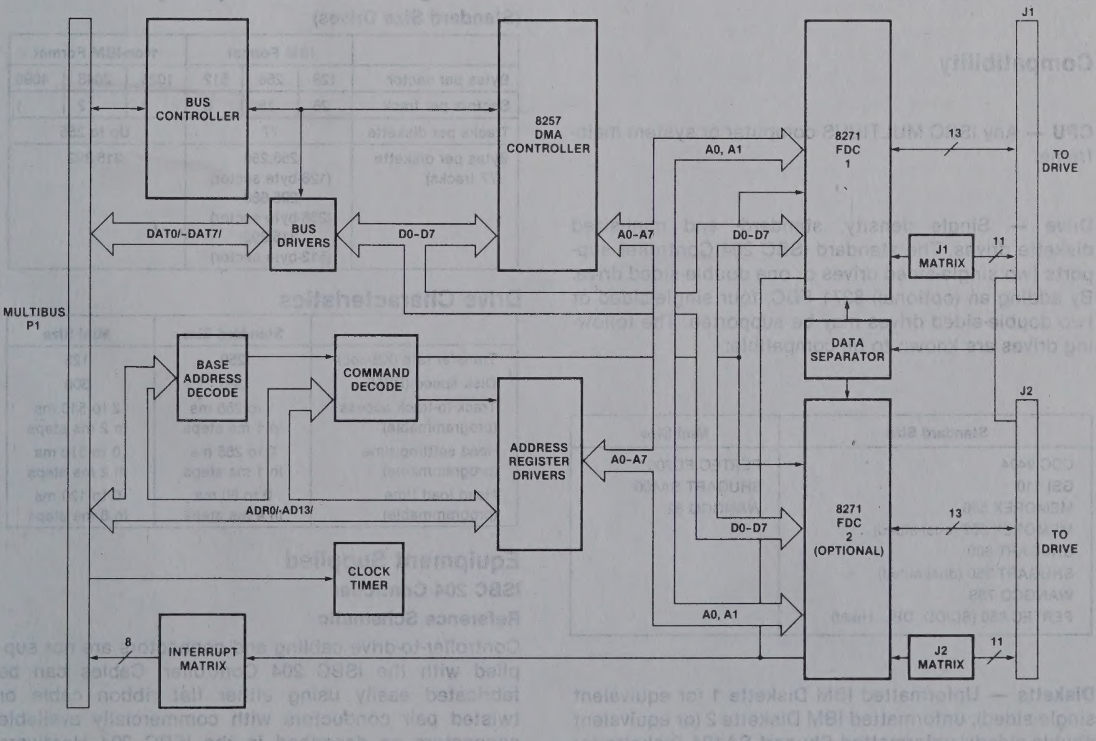

MULTIBUS P1
BUS CONTROLLER
8257 DMA CONTROLLER
DAT0/-DAT7/
BUS DRIVERS
D0-D7
A0, A1
A0-A7
D0-D7
8271 FDC 1
13
TO DRIVE
J1
J1 MATRIX
11
DATA SEPARATOR
BASE ADDRESS DECODE
COMMAND DECODE
ADDRESS REGISTER DRIVERS
A0-A7
ADR0/-AD13/
D0-D7
8271 FDC 2 (OPTIONAL)
13
TO DRIVE
J2
CLOCK TIMER
A0, A1
8
INTERRUPT MATRIX
J2 MATRIX
11

Figure 1. iSBC 204 Universal Flexible Diskette Controller Block Diagram

read from the diskette. No CPU intervention is required until a match is found or all specified sectors have been searched.

Program Initiation — All diskette operations are initiated by standard input/output (I/O) port operations through an iSBC single board computer. System software first initializes the controller with the operating characteristics of the selected drive. The diskette is then formatted under program control. For subsequent transfers, the starting memory address and transfer mode are specified for the DMA controller. Data transfers occur in response to commands output by the CPU.

Data Transfer — Once a diskette transfer operation has been initiated, the controller acts as a bus master and transfers data over the MULTIBUS at high speed. No CPU intervention is required until the transfer is complete as indicated either by the generation of an interrupt on the bus or by examination of a "done" bit by the CPU.

RMX/80 Real-Time Executive Software Support

The iSBC 204 Controller is supported by the disk file system of RMX/80, Intel's real-time executive. Files are named symbolically and may be created, deleted, or changed. Data may be accessed sequentially or directly. An unlimited number of files can be open simultaneously and multiple tasks may read the same file concurrently. A listing of service functions included under RMX/80 is shown in Table 1. Since RMX/80 is a modular system which allows functions to be implemented selectively, memory requirements are reduced considerably. Diskettes processed under RMX/80 are compatible with Intel's ISIS-II system supervisor.

Function	Operation
Open	Prepares a file for processing.
Read	Transfers data from open file to memory.
Write	Transfers data from memory to open file.
Seek	Enables direct access.
Close	Terminates processing of file.
Delete	Removes file from directory, releases its space.
Rename	Changes name of file.
Attrib	Changes attribute of a file.
Format	Initializes a new disk.
Load	Reads a file of executable code into memory.
Disk I/O	Performs basic I/O operations.

Table 1. Services Available Under RMX/80

SPECIFICATIONS

Compatibility

CPU — Any iSBC MULTIBUS computer or system mainframe.

Drive — Single density, standard- and mini-sized diskette drives. The standard iSBC 204 Controller supports two single-sided drives or one double-sided drive. By adding an (optional) 8271 FDC, four single-sided or two double-sided drives may be supported. The following drives are known to be compatible:

Standard Size	Mini Size
CDC 9404 GSI 110 MEMOREX 550 MEMOREX 552 (dual-sided) SHUGART 800 SHUGART 850 (dual-sided) WANGCO 76S PERTEC 650 (SD/DD, DBL. Head)	PERTEC FD200 SHUGART SA400 WANGCO 82

Diskette — Unformatted IBM Diskette 1 (or equivalent single-sided); unformatted IBM Diskette 2 (or equivalent double-sided); unformatted Shugart SA104 Diskette (or equivalent mini).

Data Organization and Capacity

(Standard Size Drives)

	IBM Format			Non-IBM Format		
Bytes per sector	128	256	512	1024	2048	4096
Sectors per track	26	15	8	4	2	1
Tracks per diskette	77			Up to 255		
Bytes per diskette (77 tracks)	256,256 (128-byte sector) 295,680 (256-byte sector) 315,392 (512-byte sector)			315,392		

Drive Characteristics

	Standard Size	Mini Size
Transfer rate (KB/sec)	250	125
Disk speed (RPM)	360	300
Track-to-track access (programmable)	1 to 255 ms in 1 ms steps	2 to 510 ms in 2 ms steps
Head settling time (programmable)	0 to 255 ms in 1 ms steps	0 to 510 ma in 2 ms steps
Head load time (programmable)	0 to 60 ms in 4 ms steps	0 to 120 ms in 8 ms steps

Equipment Supplied

iSBC 204 Controller

Reference Schematic

Controller-to-drive cabling and connectors are not supplied with the iSBC 204 Controller. Cables can be fabricated easily using either flat ribbon cable or twisted pair conductors with commercially available connectors as described in the iSBC 204 Hardware Reference Manual.

Optional Equipment

8271 Flexible Diskette Controller Circuit — Adding a second 8271 device to the fully tested circuit on the iSBC 204 Controller allows four drive surfaces to be supported.

Physical Characteristics

Width — 6.75 in. (17.15 cm)
Height — 0.5 in. (1.27 cm)
Length — 12.0 in. (30.48 cm)
Shipping Weight — 1.75 lb (0.80 kg)
Mounting — Occupies one slot of iSBC system chassis or iSBC 604/614 cardcage.

Electrical Characteristics

Power Requirements — 5.0V (±5%), 2.5A max

Environmental Characteristics

Temperature — 0°C to 55°C (operating); −55°C to +85°C (non-operating)

Humidity — Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating)

Reference Manuals

9800568 — iSBC 204 Diskette Controller Hardware Reference Manual (NOT SUPPLIED).

9800522 — RMX/80 User's Guide (NOT SUPPLIED).

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 204	Universal Flexible Diskette Controller

iSBC 206 DISK CONTROLLER

Full compatibility with Intel iSBC 80 and iSBC 86 Single Board Computer Systems

Interfaces directly with the Intel MULTIBUS architecture

Controls up to four 5440-type disk drives, providing up to 40 million bytes of storage

Full on-board buffering of all data transfers

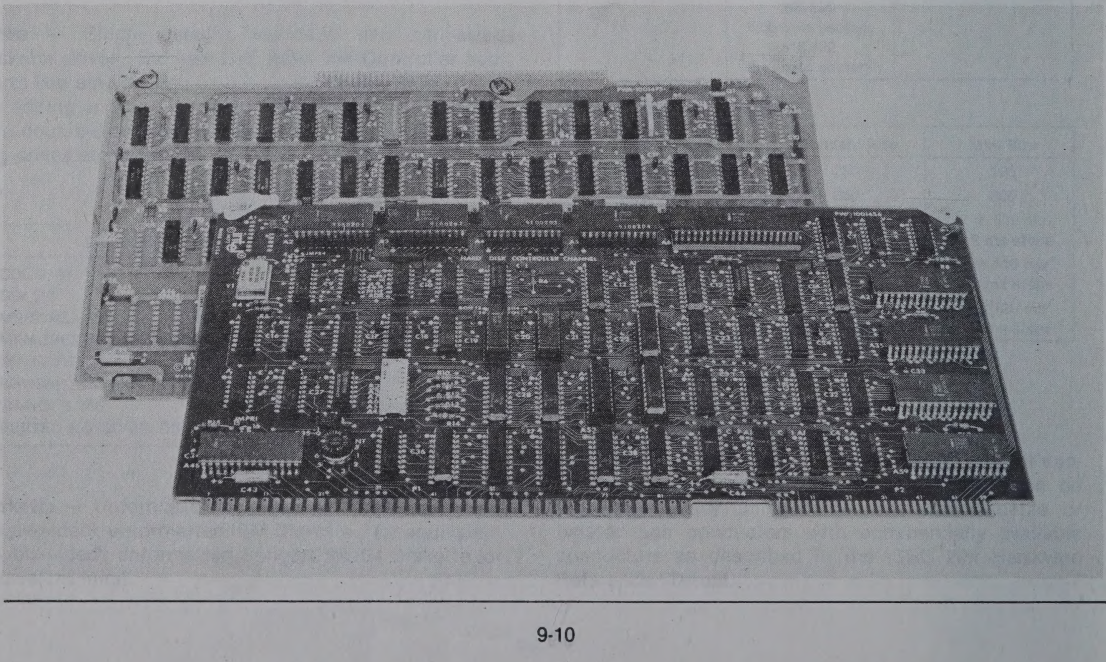
Self-diagnostics for the controller resident in on-board ROM

Software support for iSBC 80 Single Board Computers is provided through RMX/80 Real-Time Multitasking Executive

All data transfers are carried out through DMA operations.

Single +5VDC supply

The iSBC 206 Disk Controller provides an interface to a wide selection of industry-standard disk drives which meet the general specifications of the IBM 5440 type. With 5 million bytes removable on a cartridge and an additional 5 million bytes fixed on the spindle, each drive stores up to 10M bytes of data and programs. Up to four drives may be connected to the controller by means of daisy-chain cabling, which yields a total of 40M bytes per controller. The OEM and volume end user now has available a high volume, high speed data storage mechanism. Drives are available from several manufacturers, many of whom have world-wide field service organizations. The controller itself interfaces to the iSBC 80 8-bit and iSBC 86 16-bit single board computers through the Multibus system bus, Intel's industry standard bus architecture, which provides a structure and protocol for interchange of data between CPU, controller, and memory boards in the system. iSBC 80 software support for the iSBC 206 controller is provided under RMX/80, Intel's Real-Time Multitasking Executive software system, which includes a Disk File System providing disk controller-independent file handling.



FUNCTIONAL DESCRIPTION

The iSBC 206 Disk Controller is a two-board set. Commands are sent by a Multibus master single board computer to the controller, where they are analyzed and executed under control of an Intel® 3000 Series Bipolar Microprocessor system. Following the controller's receipt of the disk command, status is available to the single board computer and data are transferred by DMA between memory and the controller.

A block diagram of the iSBC 206 Disk Controller is shown in Figure 1.

Channel Board

The Channel board is the interface to the Multibus system bus; it contains the microprocessor system, the command decode circuitry and DMA control. The ROM which contains the microprocessor's program also contains a self-diagnostic program for the controller which can be invoked by command from the single board computer. The Channel board also contains a 1K byte RAM buffer, used for data buffering and for storage of the I/O Parameter Block (IOPB) which controls data transfers. The Channel board passes data and commands to the Interface board, and receives status and data from it.

Interface Board

The Interface board, under command of the Channel board, serializes/deserializes parallel data for write/read operations as well as carrying out CRC error detection calculations and driving all other control and status lines to and from the drives themselves.

Data Buffering — All data transfers to and from the disks are buffered, on a sector-by-sector basis, through the Channel board's 1K byte RAM. This minimizes the amount of bus time used by the iSBC 206 controller, because it eliminates the possibility of data overruns and subsequent repeated I/O operations. The buffer also allows the iSBC 206 Disk Controller to be placed below higher priority time-critical parts of the system (e.g., analog inputs or communications processors) in bus access priority.

Diagnostic — A comprehensive diagnostic package is resident in ROM on the Channel board. A special diagnostic connector (supplied with the Controller) is attached to the Interface board, and the single board computer invokes the diagnostic. Less than one second later, the diagnostic responds with Pass or Fail. If the result is Fail, one of 44 error codes pinpoints the fault, reducing the time required to service the Controller.

Programming

The iSBC 206 Disk Controller minimizes the number of CPU operations required to operate it. An I/O Parameter Block (IOPB) containing disk instructions and data addresses is built in memory by CPU operations, and the IOPB's address is passed to the Controller. From that time on the CPU is free to process other tasks, and is notified by interrupt when the Controller has completed its operation.

iSBC 80 and iSBC 86 Compatibility — The Controller accepts 16-bit or 20-bit addresses as pointers to the IOPB. The width of this address indicates to the controller the memory address length to be used in the I/O transfer. In addition, the IOPB will designate that either 8- or 16-bit data transfers will be used during DMA cycles. These features allow iSBC 80 and iSBC 86 single board computers to share a single iSBC 206 Disk Controller on the same Multibus system bus.

Interface Characteristics

The iSBC 206 Disk Controller supports a subset of the Diablo Series 40 drive interface. A 100-pin edge connector, designed for round twisted-pair cable, is included for interfacing the first drive; subsequent drives are connected in a daisy-chain fashion with cables available from the manufacturers.

A typical controller and disk subsystem is shown in Figure 2.

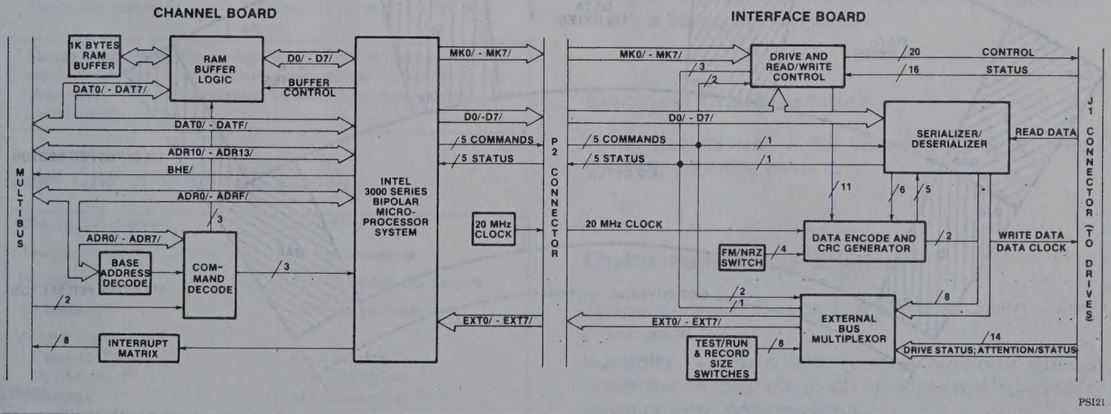

CHANNEL BOARD
INTERFACE BOARD
MULTIBUS
1K BYTES RAM BUFFER
RAM BUFFER LOGIC
D0/ - D7/
BUFFER CONTROL
DAT0/ - DAT7/
DAT0/ - DATF/
ADR10/ - ADR13/
BHE/
ADR0/- ADRF/
ADR0/ - ADR7/
BASE ADDRESS DECODE
COM-MAND DECODE
3
3
2
8
INTERRUPT MATRIX
INTEL 3000 SERIES BIPOLAR MICRO-PROCESSOR SYSTEM
MK0/ - MK7/
D0/-D7/
5 COMMANDS
5 STATUS
20 MHz CLOCK
EXT0/ - EXT7/
P2 CONNECTOR
MK0/ - MK7/
DRIVE AND READ/WRITE CONTROL
3
2
20
CONTROL
16
STATUS
D0/ - D7/
SERIALIZER/ DESERIALIZER
READ DATA
5 COMMANDS
5 STATUS
1
1
11
6
5
20 MHz CLOCK
DATA ENCODE AND CRC GENERATOR
FM/NRZ SWITCH
4
2
WRITE DATA
DATA CLOCK
2
1
8
EXTERNAL BUS MULTIPLEXOR
EXT0/ - EXT7/
TEST/RUN & RECORD SIZE SWITCHES
8
14
DRIVE STATUS; ATTENTION/STATUS
J1 CONNECTOR (TO DRIVES)
PSI21

Figure 1. iSBC 206 Disk Controller Block Diagram

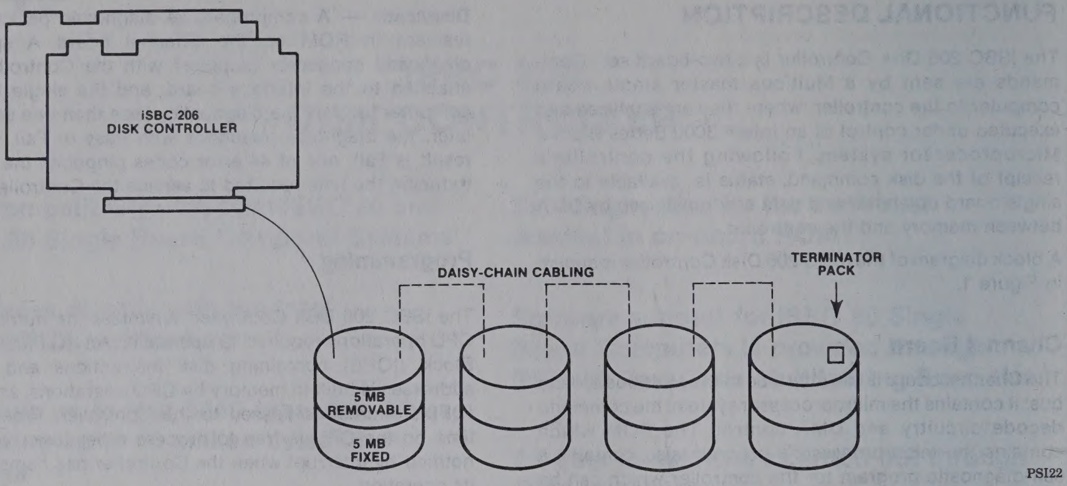

iSBC 206
DISK CONTROLLER
DAISY-CHAIN CABLING
TERMINATOR
PACK
5 MB
REMOVABLE
5 MB
FIXED
PSI22

Figure 2. iSBC 206 Disk Controller and Drives — Typical Subsystem

Table 1 shows a set of drives known to be compatible with the iSBC 206 Controller. The Controller's Hardware Reference Manual details the cabling required to connect these drives to the Controller.

Manufacturer	Model Number
Caelus	306R
CDC "Hawk"	9427H
Diablo	44B
Pertec	D3422
Wangco (Perkin-Elmer)	ST2222

Table 1. Disk Drives Compatible with iSBC 206 Disk Controller

Other drives exhibiting the required interface may also be compatible with the iSBC 206 Controller.

Record Size — The controller supports two different sector sizes: 512 bytes per sector and 128 bytes per sector. A comparison of the sectoring techniques is shown in Figure 3.

Data Formats — The iSBC 206 Disk Controller supports both double-frequency encoding (FM) and Non-return to Zero (NRZ) formats.

Option Selection — The controller allows format and record size selection at the drive level; for example, one drive on a controller could be at 512 bytes per sector, FM format, and another could be set to 128 bytes per sector, NRZ format, with no hardware conflicts.

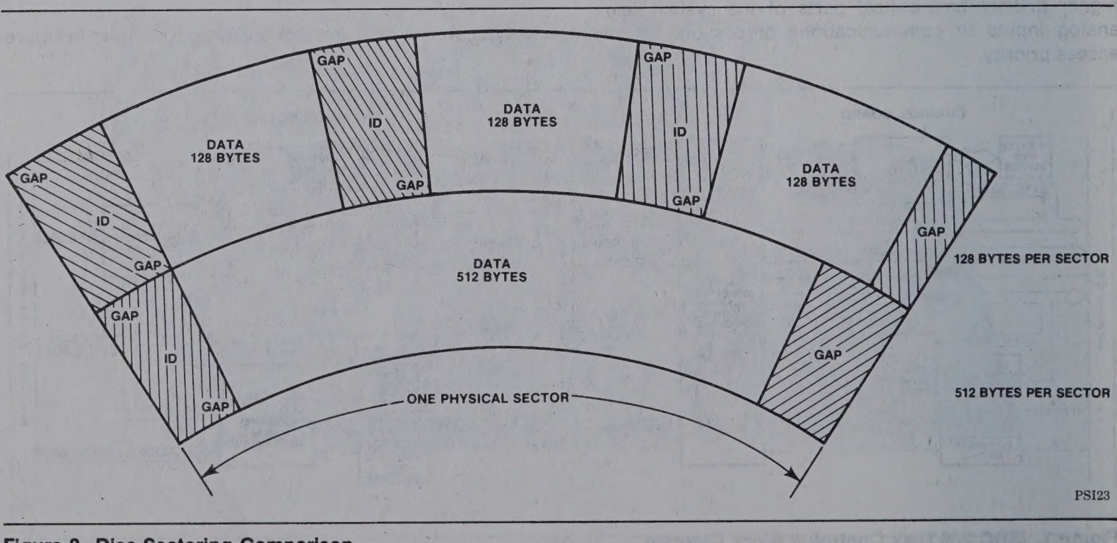

GAP
ID
GAP
DATA
128 BYTES
GAP
ID
GAP
DATA
128 BYTES
GAP
ID
GAP
DATA
128 BYTES
GAP
128 BYTES PER SECTOR
GAP
GAP
ID
GAP
DATA
512 BYTES
GAP
512 BYTES PER SECTOR
ONE PHYSICAL SECTOR
PSI23

Figure 3. Disc Sectoring Comparison

RMX/80 Real-Time Multitasking Executive for iSBC 80 Based Systems

The iSBC 206 Disk Controller is supported by both the Disk File and DISKIO levels of RMX/80's Disk File System. Files are named symbolically and may be created, deleted, or updated. Data may be accessed sequentially or directly through the file structure, with the number of open files limited only by the memory space devoted by the user to file buffers. A list of the Disk File System services available under RMX/80 is shown in Table 2.

Since RMX/80 is a modular system which allows functions to be implemented selectively, the memory requirement is reduced to that required to support only those RMX/80 modules needed in the application.

Function	Operation
Open	Prepares a file for processing.
Read	Transfers data from open file to memory.
Write	Transfers data from memory to open file.
Seek	Direct access file positioning
Close	Terminates processing of file.
Delete	Removes file from directory, releases its space.
Rename	Changes name of file.
Attrib	Changes attribute of a file.
Format	Initializes a new disk.
Load	Reads a file of executable code into memory.
Disk I/O	Performs basic I/O operations.

Table 2. Services Available Under RMX/80

SPECIFICATIONS

Compatibility

CPU — Any Intel CPU compatible with the Multibus system bus. The controller can operate with either 16- or 20-bit addresses and with either 8- or 16-bit data bus widths.

Disk Drive — Top- or front-load, cartridge type disk drive with a controller-drive interface that is compatible with a subset of the Diablo 40 Series drive interface.

Disk Cartridge — IBM style 5440 (top loading) or IBM style 2315 (front loading) or equivalent, mechanically sectioned for 12 sectors.

Data Organization and Capacity

Bytes per Sector	128 or 512 (switch selectable)
Sectors per Track	12 (512 bytes/sector) or 36 (128 bytes/sector)
Tracks per Cylinder	Up to four*
Cylinders per Drive	404 to 408 (typical)
Drives per Controller	Up to four (daisy-chained)
Total Capacity per Drive (One fixed, one removable platter)	9.830 million bytes (512 bytes per sector) 7.373 million bytes (128 bytes per sector)

* Standard two-platter disk configurations. The Controller allows up to eight tracks, available on four-platter drives (three fixed, one removable). Capacity increases to 19.660 MB per drive with the four-platter configurations.

Drive Characteristics (Typical)

Disk (Spindle) speed	2400 RPM
Average Rotational Latency	12.5 milliseconds
Bit Rate	2.5 million bits per second
Bit Density	2200 bits per inch
Access (Seek) Time	
Track-to-Track	8 milliseconds
Full Stroke	70 milliseconds
Average	38 milliseconds

Equipment Supplied

iSBC 206 Disk Controller — Channel Board, Interface Board.

Controller-to-Drive Cable Mating Connector and Hood.

Dual Auxiliary Connector (P2 Socket).

Diagnostic Connector.

Reference Schematics and Assembly Drawings — Channel Board, Interface Board.

(Connector-to-drive cabling is not supplied with the iSBC 206 Disk Controller - Cables can be fabricated using the supplied connector as described in the Hardware Reference Manual.)

Physical Characteristics

Length — 12.0 inches (30.48 cm) (Each board)

Width — 6.75 inches (17.15 cm) (Each board)

Height — 0.5 inches (1.27 cm) (Each board)

Shipping Weight — 3.5 pounds (1.6 kg)

Mounting — Occupies two adjacent card slots in iSBC 604/614 Modular Cardcage/Backplane or equivalent Multibus backplane connectors.

Electrical Characteristics

Power Requirement — 5.0 Volts DC (±5%), 5.5 Amps (typical), 6.5 Amps (maximum)

Environmental Characteristics

Temperature — 0°C to 55°C (operating); -55°C to 85°C (non-operating).

Humidity — Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating).

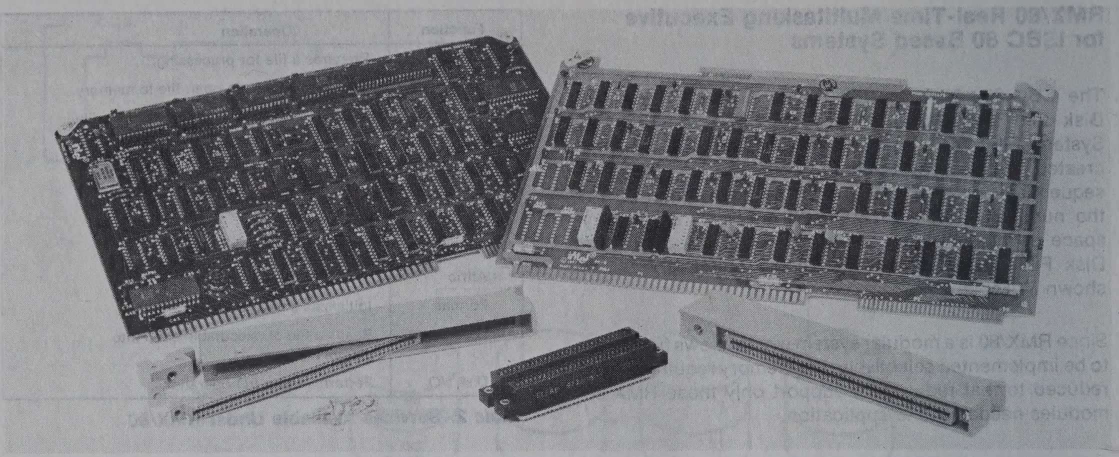


Figure 4. iSBC 206 Hardware

Reference Manuals

9800567 — iSBC 206 Disk Controller Hardware Reference Manual (NOT SUPPLIED)

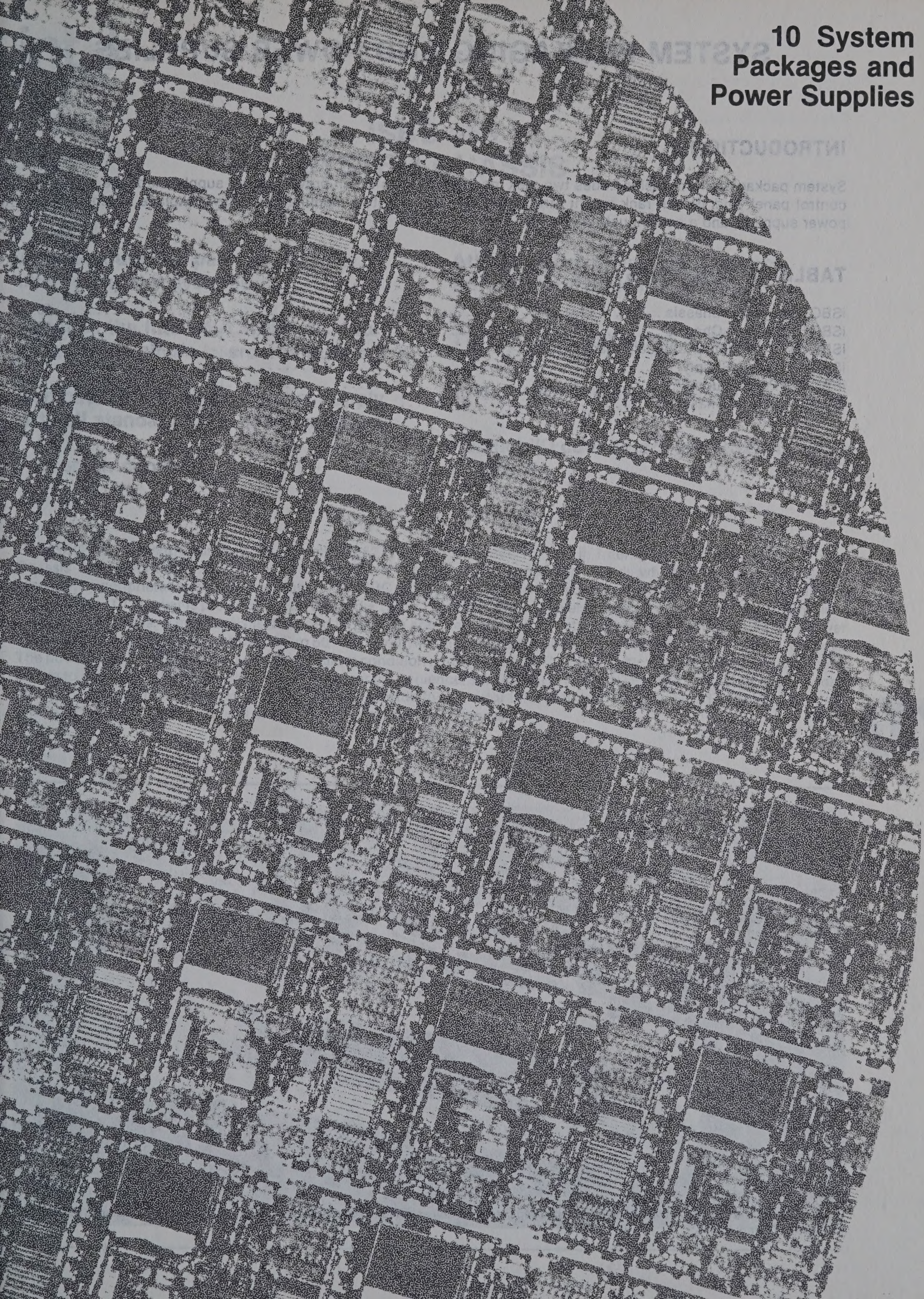
9800522 — RMX/80 User's Guide (NOT SUPPLIED)

Reference Manuals are shipped with each product only if designates SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 206	Disk Controller

10 System Packages and Power Supplies



SYSTEM PACKAGING AND POWER SUPPLIES

INTRODUCTION

System packaging from Intel includes two rack mounted chassis which provide power supply, cardcage, backplane, control panel, and 19-inch rack mount structure. There are also two modular cardcage/backplane assemblies, two power supplies, and a new industrial chassis.

TABLE OF CONTENTS

iSBC 655 System Chassis 10-3
iSBC 660 System Chassis 10-5
iSBC 604/614 Modular Cardcage/Backplane 10-8
iSBC 635 Power Supply* 10-10
iSBC 640 Power Supply* 10-13
iCS 80 Industrial Chassis* 10-15

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*The iSBC 635 and iSBC 640 Power Supplies are sold separately, as well as being included with the iCS 80 Industrial Chassis, as parts of Intel's iCS Industrial Control Series.

iSBC 655
SYSTEM CHASSIS

A rack-mountable package for Intel microcomputer systems

Provides the Intel MULTIBUS structure used on the single board computers

Compact single chassis power supply with all standard iSBC board voltages

Forced air cooling

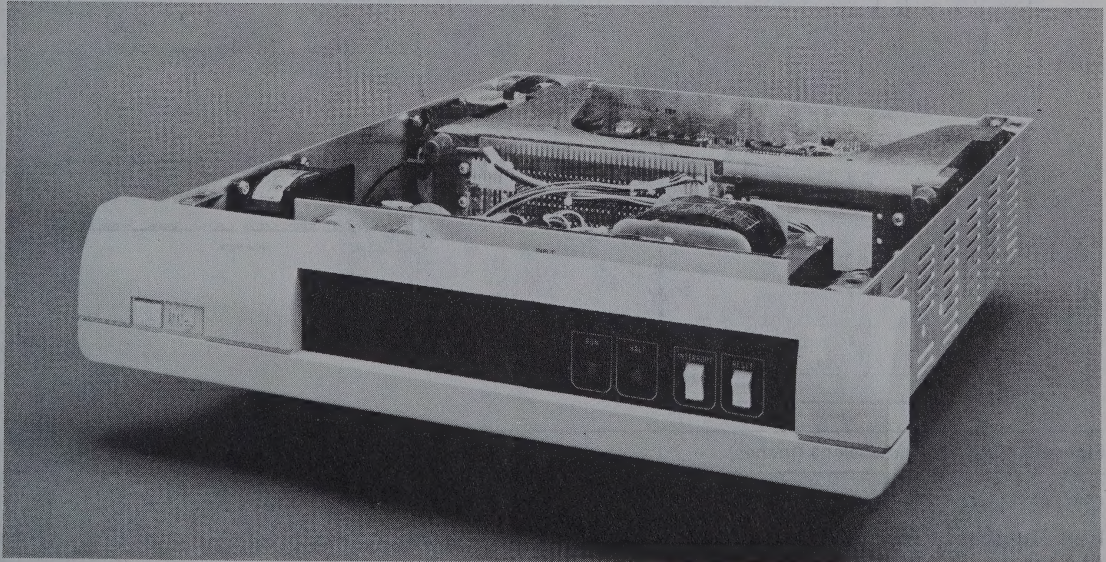
Attractive front panel with control switches and indicator lights

110V or 220V operation at 50/60 Hz

19-inch rack mountable

Parallel I/O connectors and RS232C cable included

The iSBC 655 System Chassis is an attractive 3.5″ high unit designed for use in Intel Microcomputer Systems. The Chassis' four slots accommodate both single board computers and expansion boards which provide additional I/O, memory, or peripheral controller functions. The iSBC 655 System Chassis will accept all Intel boards using the Multibus architecture. DC power is provided at ±5VDC and ± 12VDC levels, at current levels commensurate with typical combinations of four boards. The chassis is designed to provide adequate cooling to both power supply and circuit boards over external temperatures ranging from 0°C to 50°C. Current limiting and over-voltage protection are provided on all outputs. The power supply recognizes an AC power failure condition and provides a TTL signal sufficiently in advance of DC power failure to allow orderly system shut-down. For user convenience, system RESET and INTERRUPT switches are provided on the front panel to facilitate system restarts and provide for operator intervention. RUN and HALT LED indicators are driven to indicate the operational status of the single board computer.



SPECIFICATIONS

Electrical Characteristics

Input Power — Frequency: 47 - 63 Hz. Voltage (Nominal) (Single Phase): 100, 115, 215, or 230 VAC +10%

Output Power:

Nominal Voltage	Current (AMPS)(MAX)	Current Limit Range (AMPS)	Max Short Circuit (AMPS)	Over-Voltage Protection
+12	2.0	2.1-3.0	1.0 (Foldback)	+14 to +16 V
+ 5	14.0	14.7-21.0	7.0 (Foldback)	+5.8 to +6.6 V
- 5	0.9	0.9-1.4	1.4	-5.8 to -6.6 V
-12	0.8	0.8-1.2	1.2	-14 to -16 V

Combined Line/Load Regulation — ±1% at ±10% static line change and ±50% static load change, measured at the output connector (±0.2% measured at the power supply under the same conditions).

Remote Sensing — Provided for +5 VDC output line regulation.

Output Ripple and Noise — 10 mv peak-to-peak maximum (DC to 500 KHz)

Output Transient Response — Less than 50 μsec for ±50% load change

Output Transient Deviation — Less than ±5% of initial voltage for ±50% load change.

Power Failure Indication (AC Low) — A TTL open collector high signal is provided when the input voltage drops below 90% of its nominal value. DC voltages will remain within 5% of their nominal values for 3.0 milliseconds (minimum, 7.5 ms typical) after AC LOW goes true.

Physical Characteristics

Height — 3.5 inches (8.9 cm)

Width — 19 inches (48.3 cm) at Front Panel, 17 inches (43.2 cm) behind Front Panel

Depth — 20 inches (50.8 cm) with all protrusions

Weight — 37 pounds (17 Kg)

Environmental Characteristics

Temperature — Operating: 0°C to 50°C. Non-Operating: -40°C to 85°C

Relative Humidity — Up to 90%, non-condensing

Equipment Supplied

iSBC 655 System Chassis with iSBC 635 Power Supply, iSBC Cardcage/Backplane, dual fans, pop-off front panel

Connector Pack with RS232C Cable (terminal/modem interface to Single Board Computers), Two 50-pin parallel I/O connectors for Single Board Computers

Schematics for Cardcage/Backplane, Chassis

Outline Drawing

Reference Manuals (Not Supplied)

9800709 — iSBC 655 System Chassis Hardware Reference Manual

9800298 — iSBC 635 Power Supply Hardware Reference Manual

9800708 — iSBC 604/614 Cardcage Hardware Reference Manual

Manuals may be ordered from any Intel Sales Representative, Distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051

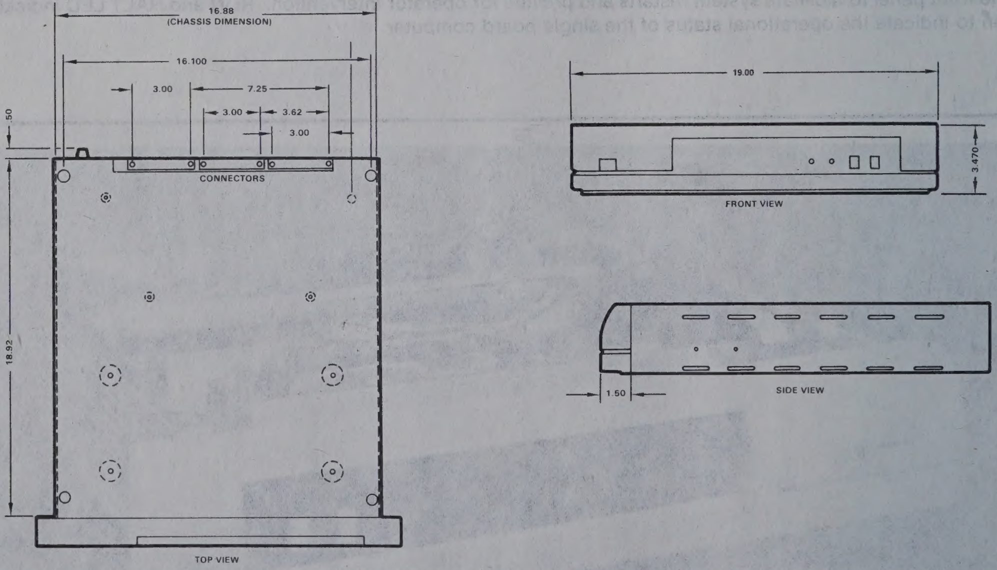


Figure 1. iSBC 655 Dimensions (Inches)

ORDERING INFORMATION

Part Number	Description
SBC 655	iSBC 655 System Chassis

iSBC 660 SYSTEM CHASSIS

Eight-slot cardcage and backplane for iSBC computers and expansion boards

Heavy duty power supply with all standard iSBC voltages

Compatible with all Intel single board computers

Forced air cooling

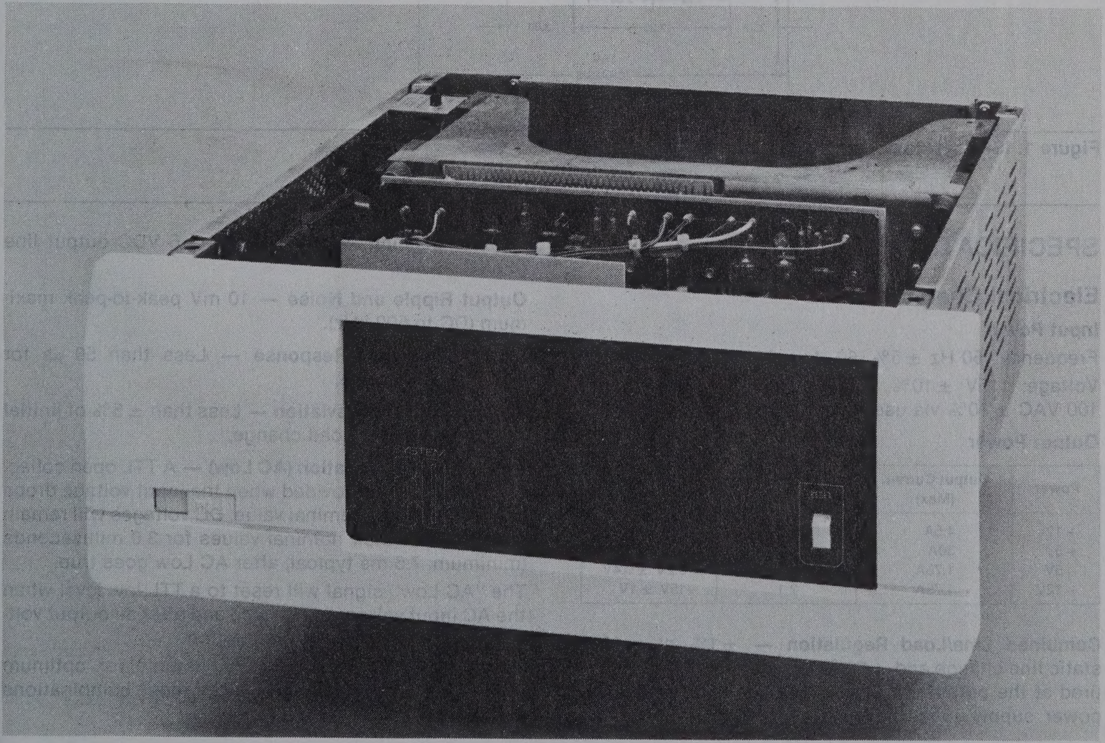
Attractive, versatile pop-off front panel

19-inch wide rack mountable chassis

Horizontal board mounting for compactness

110/220V, 50/60 Hz operation

The iSBC 660 System Chassis is an attractive, 7-inch high system chassis designed for use with Intel OEM computers. It has eight slots for single board computers, memory, I/O, or other expansion modules. The iSBC 660 is ideal for applications requiring multiple board solutions. DC power output is provided at +12V, +5V, −12V, and −5V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to 50°C temperature range for the majority of applications requiring combinations of computers, memories, peripherals, and other I/O capabilities. Current limiting and over-voltage protection is provided at all outputs. Standard logic recognizes a system AC power failure and generates a TTL signal for use in power-down control. For user convenience, a reset switch is provided on the front panel. The reset signal generated and sent to the system bus can be used for external system control.



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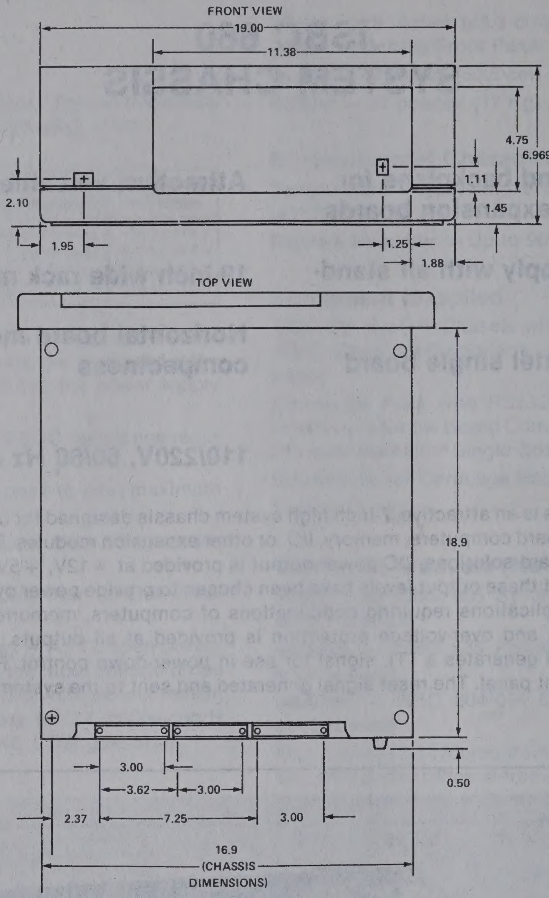


Figure 1. iSBC System Chassis Dimensions

SPECIFICATIONS

Electrical Characteristics

Input Power

Frequency: 50 Hz ±5%, 60 Hz ±5%

Voltage: 115V ±10%, 230V ±10%, 215 VAC ±10%, 100 VAC ±10% via user configured wiring options

Output Power

Power	Output Current (Max)	Current Limit (Amps)	Over-Voltage Protection
+12V	4.5A	5.4	15V ±1V
+5V	30A	3.6	6.2V ±0.4V
−5V	1.75A	2.1	-6.2V ±0.4V
−12V	1.75A	2.1	-15V ±1V

Combined Line/Load Regulation — ±1% at ±10% static line change and ±50% static load change, measured at the output connector (±0.2% measured at the power supply under the same conditions).

Remote Sensing — Provided for +5 VDC output line regulation.

Output Ripple and Noise — 10 mV peak-to-peak maximum (DC to 500 kHz).

Output Transient Response — Less than 50 μs for ±50% load change.

Output Transient Deviation — Less than ±5% of linitial voltage for ±50% load change.

Power Failure Indication (AC Low) — A TTL open collector high signal is provided when the input voltage drops below 90% of its nominal value. DC voltages will remain within 5% of their nominal values for 3.0 milliseconds (minimum, 7.5 ms typical) after AC Low goes true.

The "AC Low" signal will reset to a TTL low level when the AC input voltage is restored and after all output voltages are within specified regulation.

The "AC Low" threshold is adjustable for optimum power-down performance at other input combinations (i.e. 100 VAC, 215 VAC, 50 Hz).

Humidity — Up to 90% relative, non-condensing

Physical Characteristics

Height — 7 in. (17.8 cm)

Width

At Front Panel: 19 in. (48.3 cm)
Behind Front Panel: 17 in. (43.2 cm)

Depth — 20 in. (50.8 cm) with all protrusions

Environmental Characteristics

Temperature

Operating: 0°C to 50°C
Non-Operating: − 40°C to + 85°C

Equipment Supplied

iSBC 660 System Chassis with iSBC 640 Power Supply, iSBC 604/614 Cardcage/Backplane, dual fans, pop-off front panel

Connector pack with RS232C cable (terminal/modem interface to single board computers), two 50-pin parallel I/O connectors for single board computers

Schematics for cardcage/backplane, chassis

Outline drawing

Reference Manuals

9800505A — iSBC 660 Hardware Reference Manual (NOT SUPPLIED)

9800505 — iSBC 660 System Chassis Hardware Reference Manual (NOT SUPPLIED)

9800803 — iSBC 640 Power Supply Hardware Reference Manual (NOT SUPPLIED)

9800708 — iSBC 604/614 Cardcage Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 660	iSBC 660 system chassis

iSBC 604/614
MODULAR CARDCAGE/BACKPLANE

Interconnection on MULTIBUS system bus and housing for up to four Intel iSBC boards

Strong cardcage structure helps protect installed iSBC single board computers and expansion boards against warping and physical damage

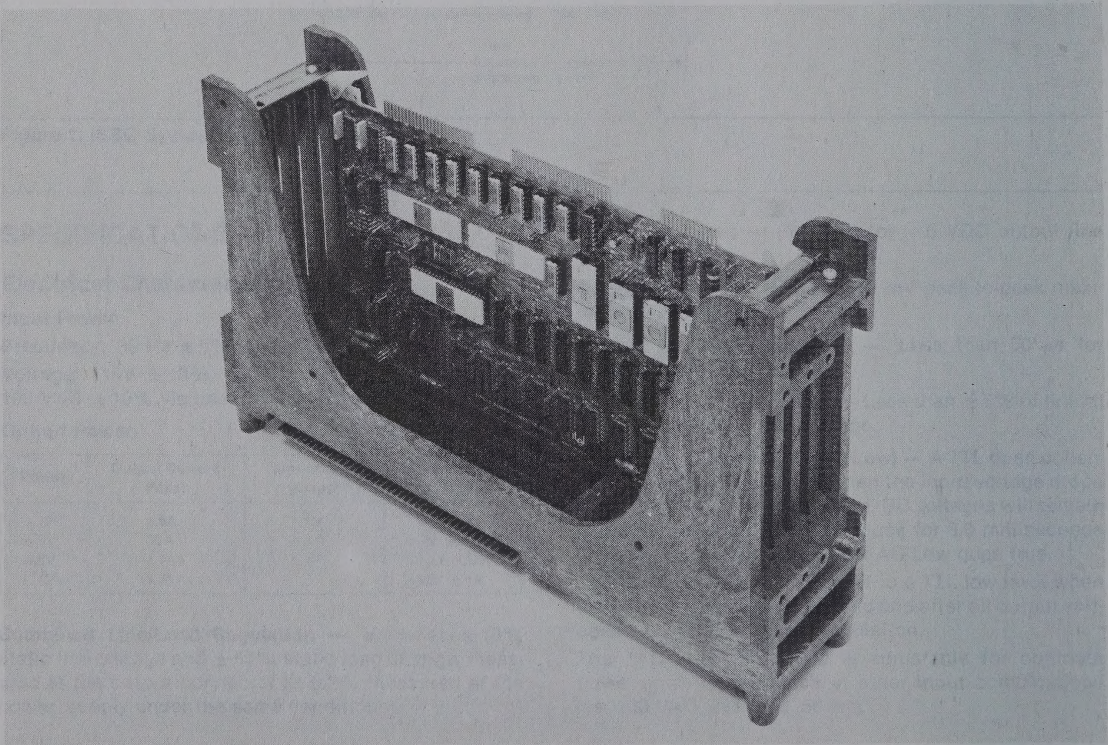
Connectors allow interconnection of two or more cardcage/backplane assemblies

Cardcage mounting holes facilitate interconnection of units

Compatible with 3.5-inch RETMA rack mount increments

Dual backplane power supply connectors and signal line termination circuits on iSBC 604 Cardcage/Backplane

The iSBC 604 and iSBC 614 Modular Cardcage/Backplane units provide low-cost, off-the-shelf housing for OEM products using two or more Intel single board computers. Each unit interconnects and houses up to four boards. The base unit, the iSBC 604 Cardcage/Backplane, contains a male backplane PC edge connector and bus signal termination circuits, plus power supply connectors. It is suitable for applications requiring a single unit, or may be interconnected with the iSBC 614 Cardcage/Backplane when more then one cardcage/backplane unit is needed. The iSBC 614 Cardcage/Backplane contains both male and female backplane connectors, and may be interconnected with iSBC 604/614 Cardcage/Backplane units. Both units are identical, with the exception of the power connectors and bus signal terminator features. A single unit may be packaged in a 3.5-inch RETMA rack enclosure, and two interconnected units may be packaged in a 7-inch enclosure. The units are mountable in any of three planes.



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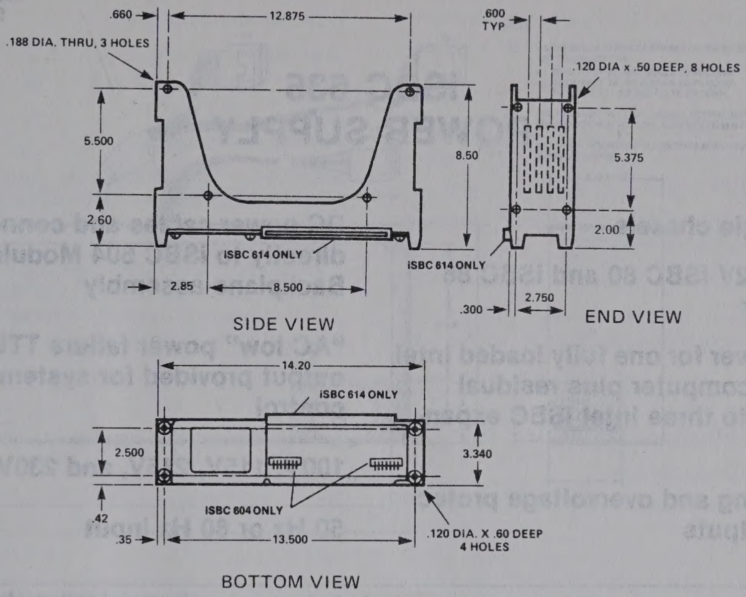

.660
12.875
.188 DIA. THRU, 3 HOLES
5.500
2.60
iSBC 614 ONLY
2.85
8.500
SIDE VIEW
.600 TYP
.120 DIA x .50 DEEP, 8 HOLES
8.50
5.375
2.00
iSBC 614 ONLY
.300
2.750
END VIEW
14.20
iSBC 614 ONLY
2.500
3.340
iSBC 604 ONLY
.42
.35
13.500
.120 DIA. X .60 DEEP 4 HOLES
BOTTOM VIEW

Figure 1. iSBC 604/614 Modular Backplane and Cardcage Dimensions

SPECIFICATIONS

Backplane Characteristics

Bus Lines — All MULTIBUS system bus address, data, and command bus lines are bussed to all four connectors on the printed circuit backplane

Power Connectors — for ground, +5V, −5V, +12V, −12V, −10V power supply lines

iSBC 604 — Bus signal terminators, backplane male PC edge connector only, and power supply headers

iSBC 614 — Backplane male and female connectors

Mating Power Connectors

AMP	Connector	87159-7
	Pin	87023-1
	Polarizing key	87116-2
Molex	Connector	09-50-7071
	Pin	08-50-0106
	Polarizing key	15-04-0219

Note

1. Pins from a given vendor may only be used with connectors from the same vendor.

Physical Dimensions

Height — 8.5 in. (21.59 cm)
Width — 14.2 in. (36.07 cm)
Depth — 3.34 in. (8.48 cm)
Weight — 35 oz (992.23 gm)

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manual

9800708 — iSBC 604/614 Cardcage Hardware Reference Manual (NOT SUPPLIED)

ORDERING INFORMATION

Part number	Description
SBC 604	Modular Cardcage/Backplane (Base Unit)

Part Number	Description
SBC 614	Modular Cardcage/Backplane (Expansion Unit)

iSBC 635 POWER SUPPLY

Compact single chassis

± 5V and ± 12V iSBC 80 and iSBC 86 system power

Sufficient power for one fully loaded Intel single board computer plus residual power for up to three Intel iSBC expansion boards

Current limiting and overvoltage protection on all outputs

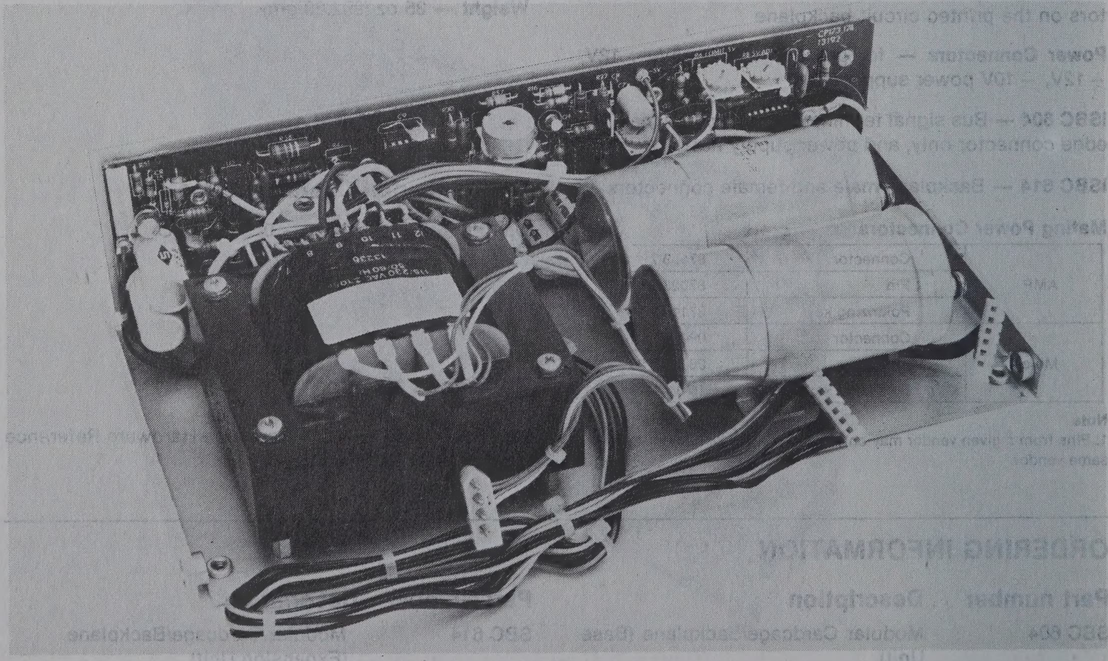
DC power cables and connectors mate directly to iSBC 604 Modular Cardcage/Backplane assembly

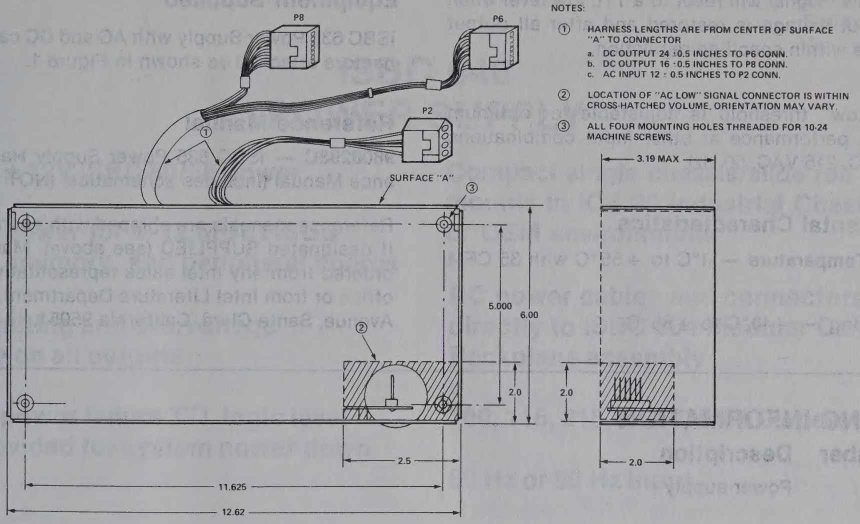
"AC low" power failure TTL Logic level output provided for system power-down control

100V, 115V, 215V, and 230V AC operation

50 Hz or 60 Hz input

The iSBC 635 Power Supply provides low cost, off-the-shelf, single chassis power generation for OEM Products using Intel single board computers. The iSBC 635 supply provides regulated DC output power at +12V, +5V, −5V, and −12V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to +55°C temperature range for one Intel single board computer fully loaded with I/O line terminators and drivers and EPROMs, plus residual capability for most combinations of up to three iSBC memory, I/O, or combination expansion boards. Current limiting and overvoltage protection is provided on all outputs. Access for AC input is provided via a standard 4-pin keyed connector. DC output power levels are provided on cables with keyed connectors directly compatible with the iSBC 604 Modular Cardcage/Backplane assembly. The iSBC 635 supply includes logic whose purpose is to sense system AC power failure and generate a TTL signal for clean system power-down control.





NOTES:

① HARNESS LENGTHS ARE FROM CENTER OF SURFACE "A" TO CONNECTOR
- a. DC OUTPUT 24 ±0.5 INCHES TO P6 CONN.
- b. DC OUTPUT 16 ±0.5 INCHES TO P8 CONN.
- c. AC INPUT 12 ± 0.5 INCHES TO P2 CONN.

② LOCATION OF "AC LOW" SIGNAL CONNECTOR IS WITHIN CROSS-HATCHED VOLUME, ORIENTATION MAY VARY.

③ ALL FOUR MOUNTING HOLES THREADED FOR 10-24 MACHINE SCREWS.

Figure 1. iSBC 635 Mounting Information

SPECIFICATIONS

Mating Connectors[1]

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output[2]

Header	Molex	09-66-1071
	AMP	87194-6

"AC Low" Control

Connector	Molex	09-50-7071
	AMP	87159-7
Polarizing key	Molex	15-04-0219
	AMP	87116-2
Pin	Molex	08-50-0106 (18 to 22 gauge wire)
	AMP	87023-1 (18 to 22 gauge wire)

Notes

1. Pins from a given vendor may only be used with connectors from the same vendor.

2. iSBC 635 DC output connectors are directly compatible with power input power connectors on iSBC 604 Modular Cardcage/Backplane assembly. Two connectors are provided.

Physical Characteristics

Height — 3.19 in. max (8.11 cm)
Width — 6.03 in. max (15.32 cm)
Depth — 12.65 in. max (32.12 cm)
Weight — 13 lb (5.90 kgm)

Electrical Characteristics

Input Power — Frequency: 47 - 63 Hz. Voltage (Nominal) (Single Phase): 100, 115, 215, or 230 VAC +10%

Output Power:

Nominal Voltage	Current (AMPS)(MAX)	Current Limit Range (AMPS)	Max Short Circuit (AMPS)	Over-Voltage Protection
+12	2.0	2.1-3.0	1.0 (Foldback)	+14 to +16 V
+ 5	14.0	14.7-21.0	7.0 (Foldback)	+5.8 to +6.6 V
- 5	0.9	0.9-1.4	1.4	-5.8 to -6.6 V
-12	0.8	0.8-1.2	1.2	-14 to -16V

Combined Line/Load Regulation — ±1% at ±10% static line change and ±50% static load change, measured at the output connector (±0.2% measured at the power supply under the same conditions).

Remote Sensing — Provided for +5VDC output line regulation.

Output Ripple and Noise — 10 mV peak-to-peak maximum (DC to 500 KHz)

Output Transient Response — Less than 50 μsec for ±50% load change

Output Transient Deviation — Less than ±5% of initial voltage for ±50% load change.

Power Failure Indication (AC Low) — A TTL open collector high signal is provided when the input voltage drops below 90% of its nominal value. DC voltages will remain within 5% of their nominal values for 3.0 milliseconds (minimum, 7.5 ms typical) after AC Low goes true.

The "AC Low" signal will reset to a TTL low level when the AC input voltage is restored and after all output voltages are within specified regulation.

The "AC Low" threshold is adjustable for optimum powerdown performance at other input combinations (i.e. 100 VAC, 215 VAC, 50 Hz).

Environmental Characteristics

Operating Temperature — 0°C to +55°C with 35 CFM moving air

Non-Operating — −40°C to +85°C

Equipment Supplied

iSBC 635 Power Supply with AC and DC cables and connectors attached as shown in Figure 1.

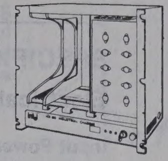
Reference Manual

9800298C — iSBC 635 Power Supply Hardware Reference Manual (includes schematics) (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 635	Power supply



iSBC 640 POWER SUPPLY

± 5V and ± 12V iSBC 80/86 power

Sufficient power for 8-12 MULTIBUS computer, memory, and peripheral boards

Current limiting and overvoltage protection on all outputs

"AC low" power failure TTL logic level output provided for system power-down control

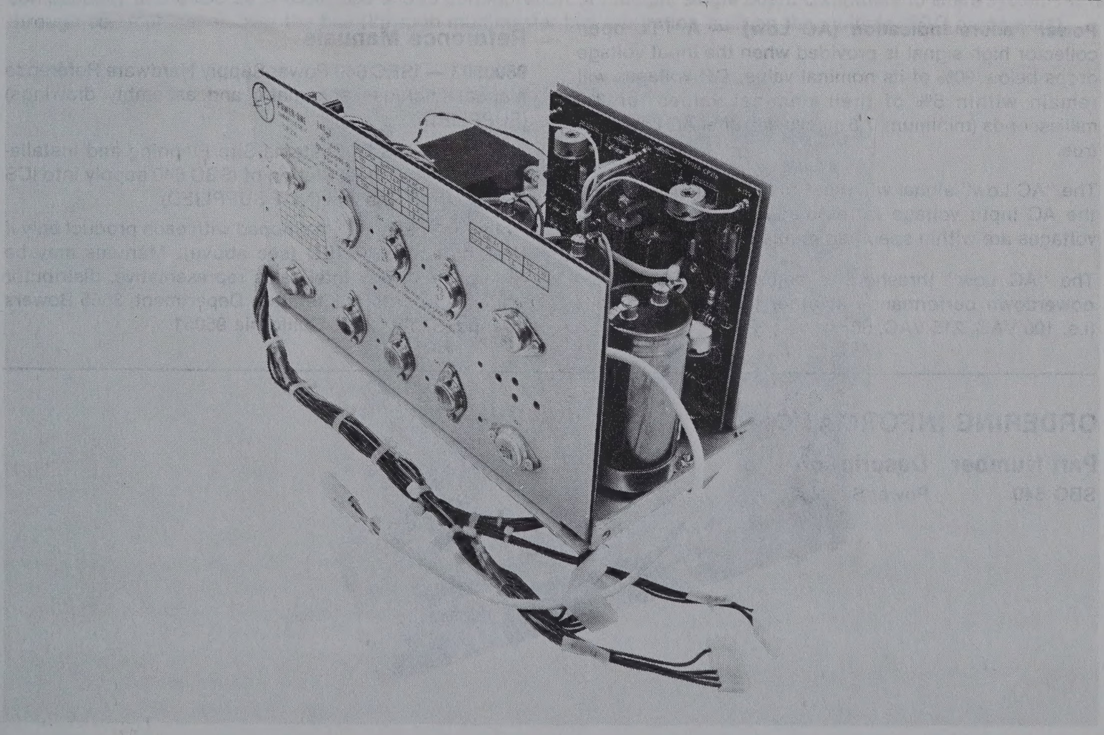
Compact single chassis/slide rail mounts in iCS 80 Industrial Chassis or OEM environments

DC power cables and connectors mate directly to iSBC 604 Modular Cardcage/ Backplane assembly

100, 115, 215, and 230V AC operation

50 Hz or 60 Hz input

The iSBC 640 Power Supply provides low cost, off-the-shelf, single chassis power generation for OEM and industrial system products using Intel single board computers. The iSBC 640 supply provides regulated DC output power at +12V, +5V, -5V and -12V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to +55°C temperature range for one fully loaded Intel single board computer, plus residual capability for most combinations of up to eleven iSBC memory, I/O, or combination expansion boards. Current limiting and overvoltage protection is provided on all outputs. Access for AC input is provided via a standard 4-pin keyed connector. DC output power levels are provided on cables with keyed connectors directly compatible with the iSBC 604 Modular Backplane/Cardcage assembly. The iSBC 640 supply includes logic whose purpose is to sense system AC power failure and generate a TTL signal for clean system power-down control.



SPECIFICATIONS

Electrical Characteristics

Input Power

Frequency: 50 Hz ± 5%, 60 Hz ± 5%

Voltage: 115V ± 10%, 230V ± 10%, 215VAC ± 10%, 100VAC ± 10%

Via user configured wiring options

Output Power

Nominal Voltage	Current (Amps) (Max)	Current Limit Range (Amps)	Short Circuit (Amps) (Max)	Overvoltage Protection
+ 12V	4.5A	4.7- 6.8	2.3	15V ± 1V
+ 5V	30A	31.5-45.0	15.0	6.2V ± 0.4V
− 5V	1.75A	1.8- 3.2	0.9	− 6.2V ± 0.4V
− 12V	1.75A	1.8- 3.2	0.9	− 15V ± 1V

Combined Line/Load Regulation — ±1% at ±10% static line change and ±50% static load change, measured at the output connector (±0.2% measured at the power supply under the same conditions).

Remote Sensing — Provided for +5 VDC output line regulation.

Output Ripple and Noise — 10 mV peak-to-peak maximum (DC to 500 KHz)

Output Transient Response — Less than 50 μsec for ±50% load change.

Output Transient Deviation — Less than ± 10% of initial voltage for ± 50% load change.

Power Failure Indication (AC Low) — A TTL open collector high signal is provided when the input voltage drops below 90% of its nominal value. DC voltages will remain within 5% of their nominal values for 3.0 milliseconds (minimum, 7.5 ms typical) after AC Low goes true.

The "AC Low" signal will reset to a TTL low level when the AC input voltage is restored and after all output voltages are within specified regulation.

The "AC Low" threshold is adjustable for optimum powerdown performance at other input combinations (i.e. 100 VAC, 215 VAC, 50 Hz).

Mating Connectors[1]

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output[2]

Header	Molex	09-66-1071
	AMP	87194-6

Notes

1. Pins from given vendor may only be used with connectors from the same vendor.
2. iSBC 640 DC output connectors are directly compatible with input power connectors on iSBC 604 Modular Cardcage/Backplane assembly. Four connectors are provided.

Physical Characteristics

Height — 6.66 in. max. (16.92 cm)
Width — 8.19 in. max. (20.80 cm)
Depth — 12.65 in. max. (32.12 cm)
Weight — 30 lbs. max (13.63 kg)

Environmental Characteristics

Temperature — 0°C to 55°C with 55 CFM moving air
Non-Operating — − 40°C to + 85°C

Equipment Supplied

iSBC 640 Power Supply with AC and DC cables with keyed connectors.

Reference Manuals

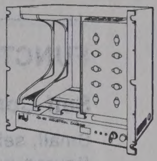
9800803 — iSBC 640 Power Supply Hardware Reference Manual (includes schematic and assembly drawings) (SUPPLIED)

9800798 — iCS 80 Systems Site Planning and Installation Manual (for installation of iSBC 640 supply into iCS 80 Industrial Chassis (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 640	Power Supply



iCS 80 INDUSTRIAL CHASSIS

MULTIBUS standard 4-slot backplane, expandable to 12 slots

Vertical board orientation for convection cooling

19-inch wide RETMA rack mounting or NEMA type backwall mounting brackets

Four fans for forced air cooling

Submitted for approval as a UL recognized component

110/230V, 50/60 Hz operation

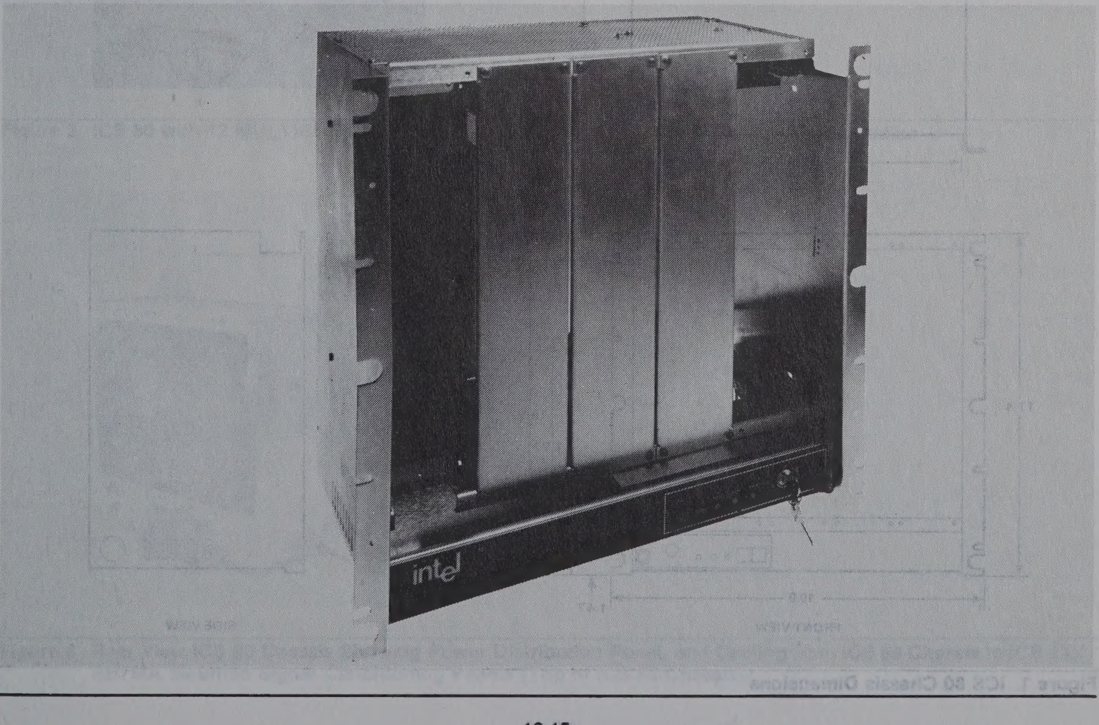
Slide in/out mounting rails for iSBC power supplies
- **Quick disconnect cabling for serviceability**
- **Your choice of supply**

Lockable service panel

All front access serviceability
- **iSBC boards**
- **Power supplies**
- **Interrupt and reset buttons**
- **Operation indicators and fuse**

Recessed mounting space for signal conditioning/wire termination panels

The iCS 80 Industrial Chassis provides industrially oriented mounting space for Intel single board computer (iSBC) products, associated iSBC power supplies, and related iCS 9XX analog and digital signal conditioning/termination panels. The base unit provides a 4-slot MULTIBUS backplane (iSBC 604) with expansion space and cabling to expand to 12 MULTIBUS backplane slots by adding additional 4-slot iSBC 614s as needed (up to two). All of the 25-plus Intel MULTIBUS bus-compatible iSBC boards can be inserted into any one of the 12 slots. In addition, over 50 products from 30 independent manufacturers have been designed for mounting into the MULTIBUS backplane. Full MULTIBUS compatibility in the iCS 80 chassis also allows configuration of multiple single board computers to share system tasks through communication over the bus (through multimaster bus arbitration built on the multiple iSBC processors).



FUNCTIONAL DESCRIPTION

Self Contained Low Cost Controllers

Small, self contained industrial controllers can be configured with the 4-slot cardcage and iSBC 635 power supply. As shown in Figure 2, this packaging can also accommodate the iCS 9XX series signal conditioning/termination panels

Or Large Power and Point Counts in a Small Package

At the high end of performance for the iCS 80 chassis, a user can build a 12-slot configuration with the Intel iSBC 640 Power Supply. This iCS 80 chassis can support the iSBC 86/12 16-bit computer with 112K bytes memory (96K RAM, 16K ROM), 64 differential analog inputs, 180 digital inputs, 52 isolated digital outputs, and 8 analog outputs (four current loops); in total a 304-channel, mixed analog and isolated digital, input and output controller, large enough for most dedicated applications (see Figure 3).

Engineered for Industrial Applications

The MULTIBUS slots are mounted vertically to improve convection cooling and the top, bottom and sides are engineered to allow maximum air flow over the boards. Four fans are provided as standard to increase air flow, allowing users to eliminate or minimize the need for supplementary fans or air conditioning.

Power Supply Flexibility

To provide a modular base on which to build a variety of configurations, no power supply is provided in the iCS 80 Industrial Chassis. Users choose one of the low cost Intel iSBC 635 (14-amp) or iSBC 640 (30-amp) power supplies based on their application. Slide in/out mounting rails are provided to match the iSBC 635 and iSBC 640 supplies, and quick disconnect cabling and connectors are provided for rapid service replacement. An AC wiring barrier strip allows simple wiring connections for integration into larger systems (see Figure 4).

Industrial Rack Mounting

The chassis mounts directly into 19-inch standard width RETMA (Radio-Electronics-Television Manufacturers Association) customer provided rack. Alternately, mounting brackets and power cabling access are provided for mounting directly on a backwall, such as the backwall panel of a NEMA-type (National Electrical Manufacturers Association), front-access-only cabinet.

Front Access Serviceability

To simplify serviceability, front access is provided for all iSBC boards, the power supply, operation indicator lights, interrupt and reset buttons, and the AC power fuse.

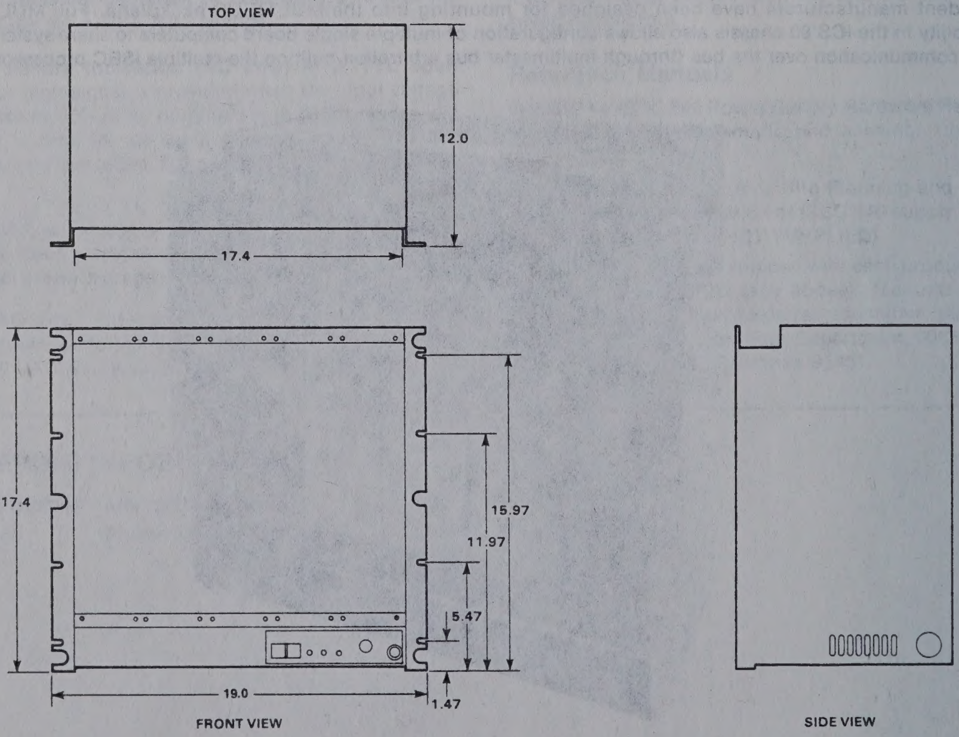
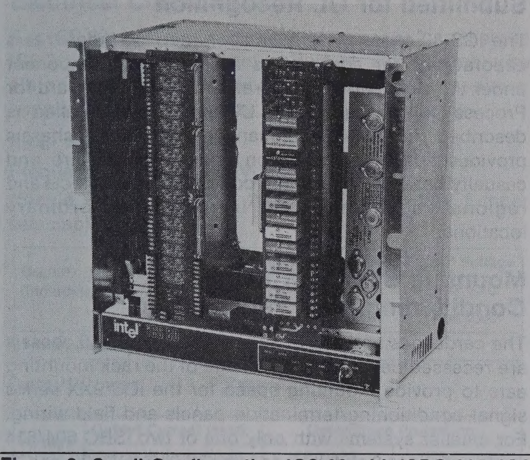


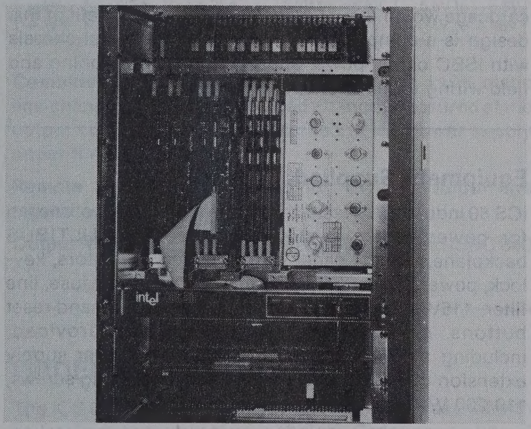
Figure 1. iCS 80 Chassis Dimensions



Typical Small Configuration

- 8-bit 8080 processor (iSBC 80/20-4)
- 2K bytes RAM
- 8K bytes ROM/EPROM
- 16 analog inputs
- 2 analog outputs
- 8 isolated digital inputs
- 8 isolated digital outputs
- 12 TTL outputs
- 12 TTL inputs

Figure 2. Small Configuration iCS 80 with iSBC 635, iCS 910 and iCS 930 Signal Conditioning/Termination Panels



Typical Maximum Configuration

- 16-bit 8086 processor (iSBC 86/12)
- 96K bytes RAM
- 16K bytes EPROM
- 64 analog inputs
- 4 analog voltage outputs
- 4 analog current outputs (4-20 mA)
- 132 isolated digital inputs
- 48 TTL digital inputs
- 52 isolated digital outputs

(All iCS 9XX Signal Conditioning/Termination Panels are not shown)

Figure 3. iCS 80 with 12 MULTIBUS Card Slots and iSBC 640 Power Supply, Large Configuration

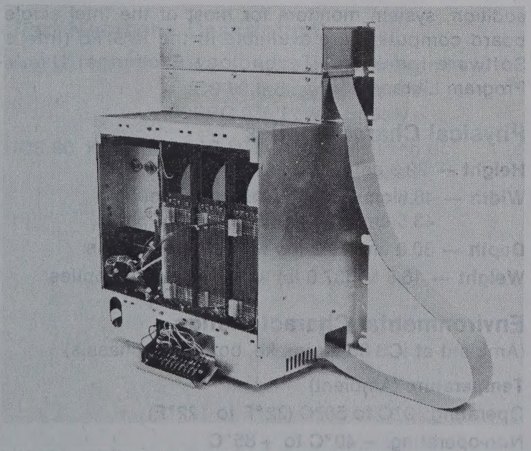


Figure 4. Rear View iCS 80 Chassis Showing Power Distribution Panel, and Cabling from iCS 80 Chassis to iCS 9XX RETMA Mounted Signal Conditioning Panels (Top of iCS 80 Chassis)

Lockable Service Panel

To assist in development, checkout and service, two pushbuttons are provided. The RESET button pulls low the initialize line ($\overline{\text{INIT}}$) on the MULTIBUS backplane. The INTERRUPT button pulls low one interrupt line on the MULTIBUS backplane ($\overline{\text{INT1}}$). Logic within the iCS 80 ensures that these buttons function with all versions of Intel single board computers. From the front of the iCS 80 chassis, without a CRT or other panel, an operator or service person can reset or interrupt on-going iCS 80 system operations to get attention, signal an alarm, or start a self-test operation.

A front panel key provides three positions: OFF (AC power off and key removable), ON (AC power on, pushbuttons enabled, key unremovable), and LOCK (AC power on, pushbuttons disabled, key removable).

Three indicator light emitting diodes record basic chassis status. POWER ON (GREEN); RUN (GREEN); and HALT (RED); the RESET or INTERRUPT buttons will remove the HALT state.

Submitted for UL Recognition

The iCS 80 chassis has been submitted to Underwriters Laboratories for approval as a U.L. listed component under the Underwriters Laboratories Safety Standard for Process Control Equipment, UL1092. When installed as described in the iCS 80 manual, the iCS 80 chassis provides adequate protection against shock, fire and casualty hazards, and should comply with most local and regional requirements for installation in ordinary locations.

Mounting Space for Signal Conditioning/Wire Terminations

The cardcages and power supplies in the iCS 80 chassis are recessed behind the front edge of the rack mounting ears to provide mounting space for the iCS 9XX series signal conditioning/termination panels and field wiring. For smaller systems with only one or two iSBC 604/614 cardcages (4 to 8 slots), up to two iCS 910, iCS 920, or iCS 930 signal conditioning/termination panels can be mounted vertically over the area where the second or third cardcage would mount (see Figure 2). The benefit of this design is a completely self-contained industrial chassis with iSBC cards, power supply, signal conditioning and field wiring terminations, all in one enclosure.

SPECIFICATIONS

Capacity

Four slots for MULTIBUS compatible single board computers, memory, I/O or other expansion boards

Expandable to 12 slots using customer plug-together iSBC 614 cardcages

Front Panel Controls

Pushbuttons

RESET: Connected to Initialize/ on MULTIBUS backplane

INTERRUPT: Connected to Interrupt 1/ line on MULTIBUS backplane.

Panel Indicator Lights (LEDs)

POWER ON (green): +5V power exists on the MULTIBUS backplane

RUN (green): CPU is executing an instruction. Light goes out if CPU is in WAIT or HALT state

HALT (red): CPU has executed a HALT instruction

Keylock

OFF: AC power off, key removable

ON: AC power on, pushbuttons enabled, key unremovable

LOCK: AC power on, pushbuttons disabled, key removable

Fuse — AC power (6A)

Equipment Supplied

iCS 80 industrial chassis, three fans for cardcages, one fan for power supply, 4-slot cardcage with MULTIBUS backplane, control panel with switches, indicators, keylock, power distribution barrier strip, AC power fuse, line filter, 115V power cable, and logic for interrupt and reset buttons. An installation package is also provided, including a NEMA cabinet mounting kit, power supply extension cables, and RETMA cabinet mounting screws, 110/230 VAC operation.

Software

See the RMX/80 Real-time Multitasking Executive specifications for industrial related applications. In addition, system monitors for most of the Intel single board computers are available in the INSITE (Intel's Software Index and Technology Exchange) User's Program Library.

Physical Characteristics

Height — 39.3 cm (15.7 in.)
Width — 48.5 cm (19.0 in.) at front panel
43.5 cm (17.4 in.) behind front panel
Depth — 30.0 cm (12.0 in.) with all protrusions
Weight — 16.8 kg (37.0 lb) without power supplies

Environmental Characteristics

(Ambient at iCS-80 air intake, bottom of chassis)

Temperature (Ambient)
Operating: 0°C to 50°C (32°F to 122°F)
Non-operating: −40°C to +85°C

Humidity — Up to 90% relative, noncondensing at 40°C

Electrical Characteristics

The iCS 80 chassis provides mounting space for either the iSBC 635 or iSBC 640 power supply. Unless otherwise stated, electrical specifications apply to both power supplies when installed by user in iCS 80 chassis.

Input Power

Frequency: 47 to 63 Hz. Voltage (Nominal)

(Single Phase): 100, 115, 215, or 230 VAC +10%, jumper selectable.

Current: (Including fans)	**With iSBC 635**	**With iSBC 640**	**Input Voltage**
	3.0A max	5.6A max	103 VAC
	1.5A max	2.8A max	206 VAC
Power, max:	315 watts	580 watts	

Output Power

Voltage	**Output Current (max)**		**Overvoltage Protection**	
	iSBC 635	**iSBC 640**	**iSBC 635**	**iSBC 640**
+12V	2.0A	4.5A	+14V to +16V	+14V to +16V
+5V	14.0A	30.0A	+5.8V to +6.6V	+5.8V to +6.6V
−5V	0.9A	1.75A	−5.8V to −6.6V	−5.8V to −6.6V
−12V	0.8A	1.75A	−14V to −16V	−14V to −16V

Combined Line/Load Regulation — ±1% at ±10% static line change and ±50% static load change, measured at the output connector (±0.2% measured at the power supply under the same conditions).

Remote Sensing — Provided for +5 VDC output line regulation.

Output Ripple and Noise — 10 mV (iSBC 635 and iSBC 640 supply) peak-to-peak, max (DC to 500 kHz)

Output Transient Response — Less than 50 μsec for ±50% load change.

Maximum Watts Dissipation (load plus losses) — 500W (iSBC 640 supply), 250W (iSBC 635 supply)

Installation

Complete instructions for installation are contained in the iCS 80 Site Planning and Installation Guide, including RETMA and NEMA cabinet mounting, and field signal, ground wiring and cooling suggestions.

Warranty

The iCS 80 Industrial Chassis is warranted to be free from defects in materials and workmanship under normal use and service for a period of 90 days from date of shipment.

Reference Manuals

9800799A — iCS 80 Industrial Chassis Hardware Reference Manual (SUPPLIES)

9800798 — iCS 80 Industrial Systems Site Planning and Installation Guide (SUPPLIED)

9800708A — iSBC 604/614 Cardcage Hardware Reference Manual (SUPPLIED)

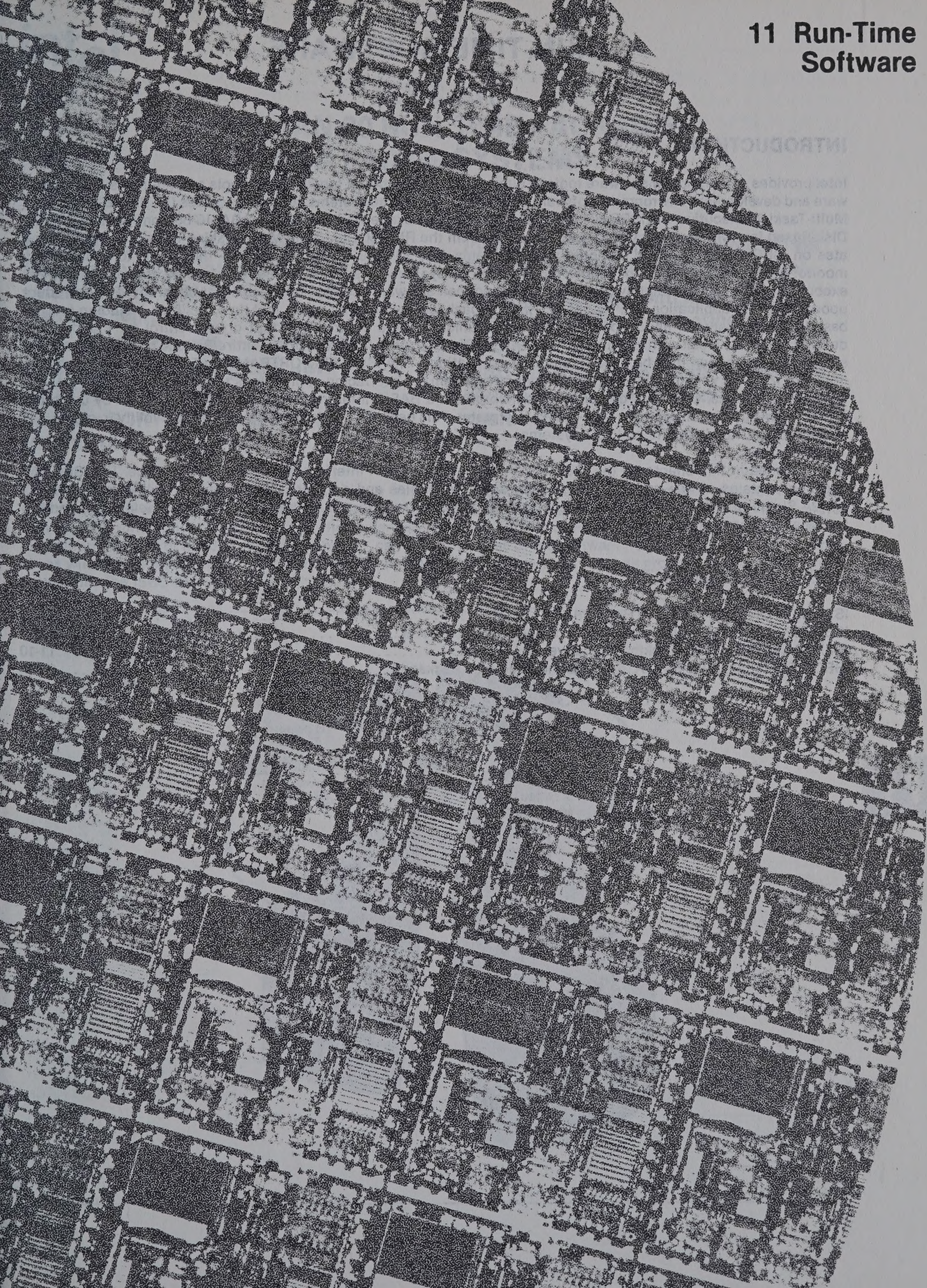
Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

The iCS 80 Industrial Chassis must be ordered as a kit with an Intel power supply of your choice. Ordering as a kit will ensure shipment of the power supply and iCS 80 chassis at the same time. Typical configurations and ordering instructions are:

Part Number	**Description**
ICS 80 Kit 635	iCS 80 system consisting of: iCS 80 Industrial Chassis iSBC 635 Power Supply
ICS 80, Kit 640	iCS 80 system consisting of: iCS 80 Industrial Chassis iSBC 640 Power Supply

11 Run-Time Software



RUN-TIME SOFTWARE

INTRODUCTION

Intel provides a full range of software tools to support the iSBC product family. These tools are run-time systems software and development environment software products. The run-time systems software includes the RMX/80 Real-Time Multi-Tasking Executive, the iSBC 801 FORTRAN Run-Time Package, and the iSBC 802 BASIC-80 Configurable RMX/80 Disk-Based Interpreter. Many OEMs have benefited from the RMX/80 Real-Time Multi-Tasking Executive, which operates on iSBC 80 single board computers and systems. The RMX/80 executive provides the means to concurrently monitor and control multiple external events occurring asynchronously in real-time. When users choose the RMX/80 executive, they may immediately begin implementing their software and then later select the specific iSBC 80 product upon which the application will be based. RMX/80 package contains all major real-time facilities including priority based system resource allocation, intertask communication and control, interrupt driver control for standard I/O devices, real-time clock control, interrupt handling, and many other features. Often, entire RMX/80 programs from one structured application may be used in multiple applications. The iSBC 801 FORTRAN Run-Time Package provides a library of routines which make up a convenient mechanism for interfacing applications tasks written in FORTRAN-80 to RMX/80 services. Or, OEMs can choose to incorporate a BASIC interpreter in their end user system by using the iSBC 802 BASIC-80 Configurable Disk-Based Interpreter. This package provides users with the capability to create and execute BASIC applications on iSBC systems.

Also included in this chapter is the iSBC 957 Intellec–iSBC 86/12A Interface and Execution Package. The iSBC 957 package contains all the necessary hardware, software, cables and documentation required to interface an iSBC 86/12A Single Board Computer to an Intellec Microcomputer Development System for software development and full speed execution.

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iSBC 801
FORTRAN-80 RUN-TIME PACKAGE FOR RMX/80 SYSTEMS

The ideal iSBC 80 Single Board Computer run-time environment for programs written in Intel's ANS FORTRAN 77 standard compiler.

Fully compatible with Intel's RMX/80 Real-Time Multitasking Executive Software.

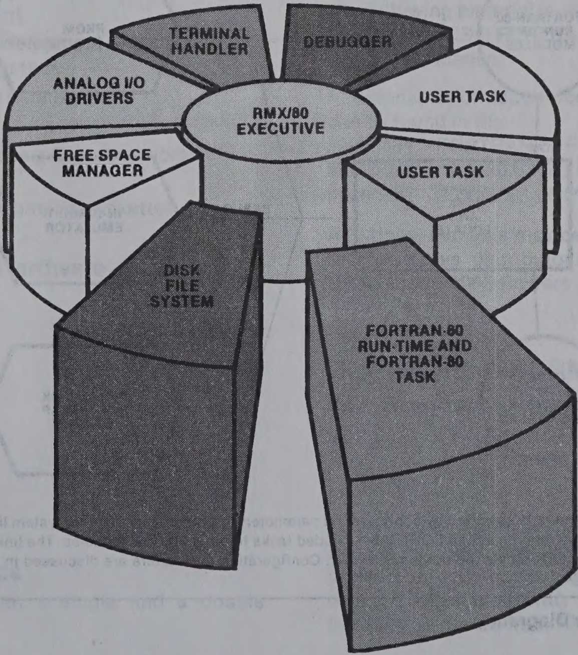
Includes FORTRAN-80 disk I/O via RMX/80 Disk File System.

Includes FORTRAN-80 terminal I/O via RMX/80 mini or full Terminal Handler.

Software floating point libraries are compatible with Intel floating point standard.

iSBC 310 High Speed Math Unit drivers allow acceleration of floating point operations.

The iSBC 801 FORTRAN-80 Run-Time Package is a complete, ready-to-use set of linkable object modules which are fully compatible with RMX/80 systems. The modules, when combined with the FORTRAN-80 coded application, provide the appropriate interfaces to the disk file system and terminal handler of RMX/80. The FORTRAN-80 application, in addition to usage of the disk file or terminal I/O, can take advantage of the software floating point routines. In those cases where accelerated operations are necessary, the FORTRAN-80 Run-Time Package provides the necessary interface to use the iSBC 310 High Speed Math Unit.


TERMINAL HANDLER
DEBUGGER
ANALOG I/O DRIVERS
RMX/80 EXECUTIVE
USER TASK
FREE SPACE MANAGER
USER TASK
DISK FILE SYSTEM
FORTRAN-80 RUN-TIME AND FORTRAN-80 TASK

FUNCTIONAL DESCRIPTION

The FORTRAN-80 Run-Time Package is a complete, ready-to-use set of linkable object module libraries on both a single and a double density diskette. it can be combined with the RMX/80 modules and user-supplied application software modules on the Intellec Development System. The FORTRAN-80 Run-Time Package for RMX/80 systems is the ideal environment for executing the FORTRAN-80 code in an iSBC 80 system. It provides full data formatting and storage capability through the RMX/80 Disk File System. The package allows utilization of the RMX/80 Terminal Handler for entry and display of information on a TTY or CRT. In addition, the FORTRAN-80 Run-Time Package facilitates effective use of the iSBC 310 High Speed Math board to optimize floating point calculations.

Features and Benefits of the FORTRAN-80 Run-Time Package

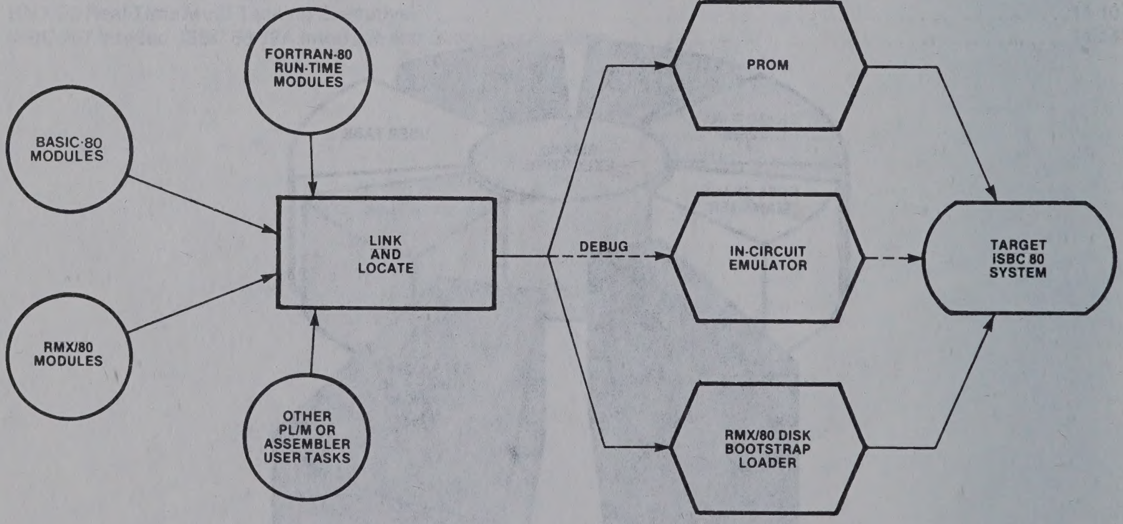
The modules included on the diskettes are readily usable by linking with the user-coded FORTRAN-80 relocatable object modules for operation in the RMX/80 environment. Advantages for the iSBC user include:

Direct communication with the mini or full Terminal Handler and Disk File System by using the formatted I/O facility in FORTRAN-80 coded application tasks. The user is able to specify the external format of data (integer, floating point, and character) as either input or output on those devices. The universality of formatted data statements in FORTRAN-80 facilitates storing relevant data for later retrieval, as well as summary display of the information. For example, to read two variables:

```
READ (5,88) X, Y
88 FORMAT (F10.3, F6.2)
```

The run-time software support modules are built for selective utilization at link time with FORTRAN-80 coded tasks. Selective linking can be profitably used to insure that only those modules which exactly match FORTRAN-80 application requirements are included in the run time systems. This insures that the minimum memory is required in the final system.

Software modules provided with the package are conveniently linkable with the RMX/80 library modules. This allows use of the right software tool (whether 8080/8085 Assembler, PL/M-80, or FORTRAN-80) for the right job. The user is also able to combine all the software elements into a highly effective RMX/80 based applica-



The RMX/80 executive based environment is specified by configuration parameters supplied at the time of system linking. These parameters define expected system characteristics and the relationship of FORTRAN-80 coded tasks to other RMX/80 modules. The linker output is the object code which may be placed in PROM or loaded into RAM via the bootstrap loader. Configuration parameters are discussed in detail in the RMX/80 User's Guide, Chapter 3.

Figure 1. Configuration Flow Diagram

tion. FORTRAN routines can be interfaced to PL/M or assembler coded routines so portable software can be run on all RMX/80 based systems.

Application writing with the floating point algorithms of FORTRAN-80 is enhanced thru the accuracy insured by FORTRAN-80 adherence to the Intel Floating Point Standard. Accuracy is insured thru software; it can be duplicated and accelerated thru the interface modules for the iSBC 310 High Speed Math Board. The iSBC customer now can effectively perform high speed, accurate computations with pre-coded and debugged mathematical functions.

Generation Considerations

The FORTRAN-80 Run-Time Package consists of several relocatable library modules. The modules are configurable with the RMX/80 supplied library modules and user coded FORTRAN-80, PL/M-80 or 8080/8085 system. Through the proper linkage and location of the appropriate modules, a complete software solution for the target iSBC 80 system can be generated. This software then can be quickly loaded into the target iSBC 80 system through ICE-80 or 85 during debug. The final application code is placed in EPROM or loaded directly from disk via the RMX/80 boostrap loader.

Description and Capabilities Summary

To run FORTRAN-80 programs under RMX/80, libraries are selected from two packages: the RMX/80 Real-Time Multitasking Executive and the FORTRAN-80 Run-Time Package for RMX/80 systems. The FORTRAN-80 Run-Time Package provides libraries to support FORTRAN-80 coded programs running under RMX/80:

F80RMX.LIB	FORTRAN-80 input/output formatting and interface routines for the RMX/80 environment.
FPSFTX.LIB	Software floating point arithmetic routines for the RMX/80 environment.
FPHRDX.LIB	Software interface routines for the iSBC 310 facilitate floating point calculations in the RMX/80 environment of an iSBC 80/20 or iSBC 80/30 hardware based system. FPHX10.LIB is another library provided specifically for the iSBC 80/10 based RMX/80 system.

SPECIFICATIONS

Generation Environment

Intellec Microcomputer Development System with ISIS-II Diskette Operating System.

Minimum of 64K bytes RAM memory.

Dual Floppy Diskettes.

RMX/80 Real-Time Multi-Tasking Executive library diskettes.

FORTRAN-80 (V2.0 or later) Compiler diskettes.

Compatible Run-Time Hardware

Single Board Computers:

- iSBC 80/10A
- iSBC 80/20-4
- iSBC 80/30

Disk Controllers:

- iSBC 202
- iSBC 204
- iSBC 206

Other:

- iSBC 310 Math Unit

Physical Characteristics

Product distributed on both a single and a double density diskette.

Reference Manuals

The following material is shipped with the product:

#9800480	ISIS-II FORTRAN-80 Compiler Operator's Manual

Additional information for FORTRAN-80 and RMX/80 can be found in the

#9800481	FORTRAN-80 Programming Manual
#9800522	RMX/80 User's Guide
#9800547	8080/8085 FORTRAN-80 Reference Card

Additional manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 801	FORTRAN-80 Run-Time Package for RMX/80 Systems

FORTRAN-80 Run-Time Package is copyrighted and licensed by Intel Corporation. It can be purchased only under a required license agreement with Intel. Software may be developed with the FORTRAN-80 Run-Time Package to run on Intel RMX/80 based systems.

iSBC 802
BASIC-80 CONFIGURABLE RMX/80 DISK BASED INTERPRETER

Resident BASIC interpreter for iSBC 80 Single Board Computers

Sequential or random access diskette storage for programs and data

Single and double precision software floating point arithmetic

Direct port I/O instructions for special input and output requirements

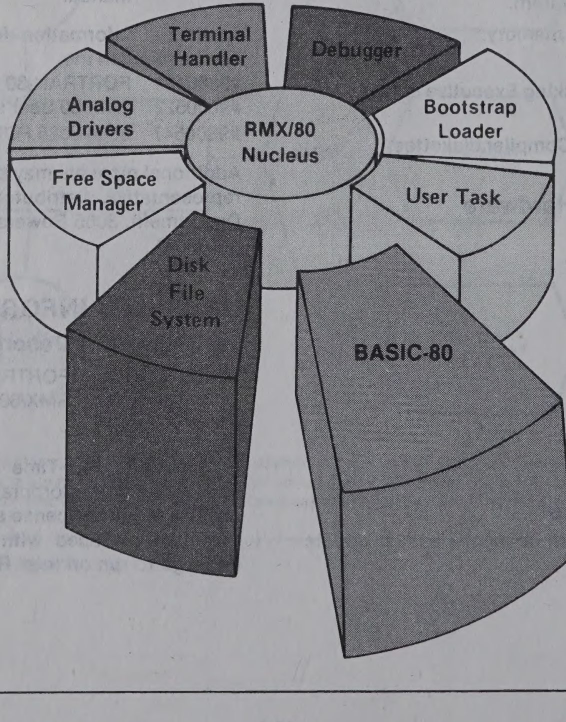
Interface up to 25 user defined software functions written in 8080/8085 assembler, PL/M-80, or FORTRAN-80

Totally compatible with Intel's RMX/80™ Real-Time Multitasking Executive software

Exceeds the ANS X3.60-1978 and the ECMA-55 minimal BASIC standard

Interpreter supplied in two forms:
- **—A relocatable module for tailoring systems to exact requirements**
- **—A predefined version which incorporates the RMX/80™ Nucleus, Terminal Handler, and Disk File System for an iSBC 80/30 and iSBC 204 based system**

The iSBC 802 BASIC-80 Configurable RMX/80 Disk Based Interpreter has a complete ready-to-use set of linkable object modules which are fully compatible with Intel's RMX/80 Real-Time Multitasking Executive Software. The modules combine with RMX/80 to provide a BASIC-80 interactive interpreter system. BASIC-80 programs may be created, stored, and interpreted on the iSBC 80 based system. These programs may use the disk file and terminal I/O, software floating point, or interface to other routines provided by the user to tailor the BASIC-80 system.



FUNCTIONAL DESCRIPTION

The RMX BASIC-80 Interpreter provides a high level language interpreter with extended disk capabilities which operates under the RMX/80 Real-Time Multitasking Executive and translates BASIC-80 source programs into an internally executable form. This universally accepted language is designed for the OEM who requires a pass through programming language suitable for usage by both beginners and experienced programmers. BASIC-80 offers users an expedient method of utilizing the powerful computational and input/output capabilities of an iSBC 80 microcomputer system and applying them to solving a wide range of application problems. The BASIC-80 language has a rich complement of statements, functions, and commands to program applications requiring a full range of 1) string manipulation and disk I/O for data processing, 2) single and double precision floating point and array handling for numeric analysis, or 3) port I/O with mask operations controlled through bitwise Boolean logical operators. In addition, Intel's BASIC-80 meets and exceeds the requirements of ANS X3.60-1978 Minimal BASIC Standard and, similarly, the Standard ECMA-55 Minimal BASIC.

Dual Solution

The iSBC 802 provides BASIC-80 to the OEM in two forms. First, the product is supplied as a set of linkable object modules on both a single and a double density diskette which can readily be combined with RMX/80 library and user application modules. The Intellec Development System is used to form a complete software solution for the iSBC 80 based system from this configurable version. Second, for users who want an "instant-on" BASIC system and have no need to add additional software routines for their end product, a predefined BASIC-80 software system has been included in the iSBC 802. The predefined system includes 1) the RMX/80 and BASIC-80 software modules configured into an executable object module (RMXSYS) which is supplied on the same single and double density diskettes as the relocatable BASIC-80 modules, 2) a set of bootstrap PROMs that will load the executable RMXSYS module from the diskette into the iSBC main memory, and 3) a cable that connects the iSBC 204 Floppy Diskette Controller to the bulkhead connector on any Intellec diskette drive chassis. The predefined system offers an "instant-on" software capability for the user's supplied hardware system consisting of the following items:

iSBC 80/30 Single Board Computer
iSBC 204 Universal Flexible Diskette Controller
32K bytes additional RAM memory (either iSBC 032 or
  two iSBC 016s)
Compatible teletypewriter terminal
Compatible diskette drives

RMX/80 BASIC-80 FEATURES AND BENEFITS

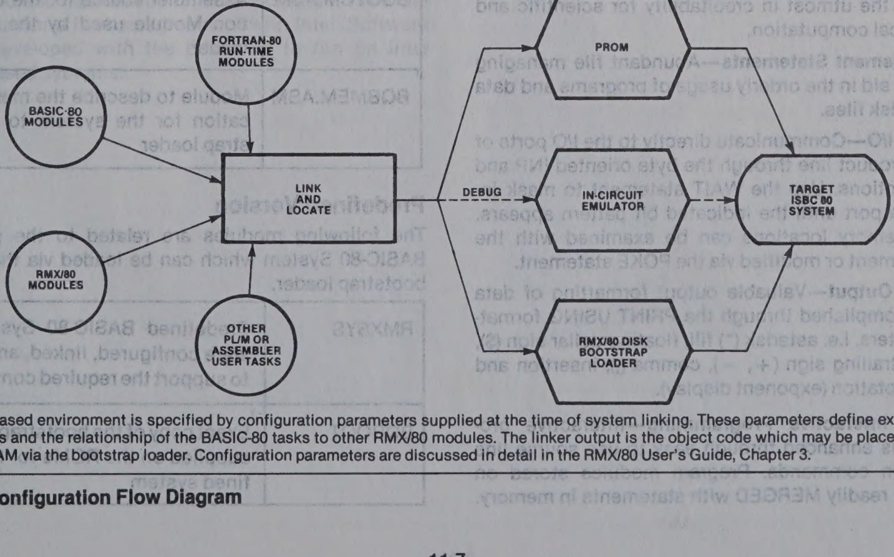
Meets New Industry Standard

BASIC-80 provides the OEM and end-user with a resident programming language for the iSBC 80/10A, iSBC 80/20, iSBC 80/20-4, or iSBC 80/30 based systems. A desirable and cost effective language feature is its PROM or disk resident capability. BASIC-80 also complies with an industry standard that defines the Minimal BASIC language specification and provides a level of confidence and structure not previously available to the OEM with BASIC interpreters. Since Intel's BASIC-80 meets this standard, the user can be assured of a maximum amount of compatibility with other BASIC interpreters.

Major Features of ANS X3.60-1978 Include:

Constants and Variables—The user can describe and manipulate constants and variables in a form most suited to the application. The numeric expression can be constructed from variables, numeric constants, and function references. The string expression is composed of a string variable or a string constant.

Numeric Functions—Commonly used single precision scientific numeric functions are provided for cosine, sine,



The RMX/80 based environment is specified by configuration parameters supplied at the time of system linking. These parameters define expected system characteristics and the relationship of the BASIC-80 tasks to other RMX/80 modules. The linker output is the object code which may be placed in EPROM or loaded into RAM via the bootstrap loader. Configuration parameters are discussed in detail in the RMX/80 User's Guide, Chapter 3.

Figure 1. Configuration Flow Diagram

tangent, arctangent, square root, exponentiation, absolute value, integer, sign of a number, log, and random number generation. In addition, RANDOMIZE can be used to override the predefined pseudo-random number values. All underflow and overflow conditions are recognized and reported in a consistent and defined manner.

Program Control and Sequencing—Specific program control and the sequencing of statement execution is provided.

Assigned Variable Values—Variables can be assigned values by the use of DATA statements which can be READ and manipulated through the RESTORE statement.

Custom Functions—The user can define custom functions for use during program execution.

Indexed Arrays—Arrays can be indexed starting with 0 or 1 and the array's size is established through a dimension (DIM) statement.

Interactive I/O—Program directed prompts can be sent to the terminal through the INPUT statement in addition to accepting input data values. Effective tabular output is accomplished through the PRINT statement which will cause the transmission of a character string to an external device.

EXTENSION BEYOND INDUSTRY STANDARD

Intel's BASIC-80 has enhancements and extensions beyond the standard. These include the following:

PROM Storage—BASIC-80 interpreter and program source can be stored in PROM and then executed at system startup. This allows users to take advantage of special routines they have written in other languages, PL/M-80, FORTRAN-80, or 8080/8085 Assembler.

Floating Point Standardization—The OEM can code floating point algorithms in BASIC-80 because the accuracy is insured by the BASIC-80 interpreter's adherence to the Intel Floating Point Standard. Single precision is accurate to a maximum value 3.40282E + 38 and double precision is accurate to a maximum value of 1.79769313486231 D + 308 for the utmost in creditability for scientific and mathematical computation.

File Management Statements—Abundant file managing statements aid in the orderly usage of programs and data stored on disk files.

Direct Port I/O—Communicate directly to the I/O ports of the iSBC product line through the byte oriented INP and OUT instructions. Use the WAIT statement to mask inputs from a port until the indicated bit pattern appears. Specific memory locations can be examined with the PEEK statement or modified via the POKE statement.

Formatted Output—Valuable output formatting of data can be accomplished through the PRINT USING formatting characters, i.e. asterisk (*) fill, floating dollar sign ($), leading or trailing sign (+, −), comma (,), insertion and scientific notation (exponent display).

Enhanced Interactive Programming—Interactive programming is enhanced through easy to use source line modification commands. Program modules stored on disk can be readily MERGED with statements in memory.

GENERATION CONSIDERATIONS

Generation of Configurable Version

The configurable portion of the iSBC 802 BASIC-80 package consists of several relocatable library modules. These modules are configurable with the appropriate RMX/80 library routines (Minimal Terminal Handler, Nucleus, Disk File System and Loader) and the other application tasks to form a full system. Through the proper linkage and location of the appropriate modules, a complete software solution for the iSBC 80 system can be generated. This software then can be quickly loaded into the iSBC 80 system through ICE 80 or 85 during debug. The final application code is placed in EPROM or loaded directly from disk via the RMX/80 bootstrap loader.

DESCRIPTION AND CAPABILITIES SUMMARY

Configurable Version

To create a tailored BASIC-80 System for an iSBC 80 based product, libraries are selected from two packages: the RMX/80 Real-Time Multitasking Executive and the BASIC-80 Configurable RMX/80 Disk Based Interpreter package. The BASIC-80 Configurable RMX/80 Disk Based Interpreter package provides the following files for use with RMX/80 (Version 1.3 and above).

BASIC.LIB	Necessary modules for linkage with RMX/80
BQOPS.ASM	"Include" source file for BASIC-80 options related to the creation of a tailored system
BASCM.ASM	The macro assembler source for the Configuration Module used for RMX/80
BQMEM.ASM	Module to describe the memory allocation for the BASIC-80 task
BOOTCM.ASM	Assembler source for the Configuration Module used by the bootstrap loader
BQBMEM.ASM	Module to describe the memory allocation for the system to the bootstrap loader

Predefined Version

The following modules are related to the predefined BASIC-80 System which can be loaded via the supplied bootstrap loader.

RMXSYS	Predefined BASIC-80 System software configured, linked, and located to support the required configuration
BQBOOT	Exact copy of the bootstrap loader as supplied on the ROMs for the predefined system

SPECIFICATIONS

Configurable Version Generation Requirements

Intellec® Microcomputer Development System with ISIS-II Diskette Operating System

Minimum of 48K bytes RAM memory

Dual Floppy Diskettes

RMX/80 Real-Time Multitasking Executive library diskettes (Version 1.3 and above)

Compatible Run-Time Hardware

Single Board Computers
- iSBC 80/10A
- iSBC 80/20-4
- iSBC 80/30

Disk Controllers
- iSBC 202
- iSBC 204
- iSBC 206

Predefined Version Generation Requirements

No system generation is required as the software system has been predefined to execute in the run-time environment specified below:

- iSBC 80/30
- iSBC 204 disk controller
- Additional 32K bytes memory (either iSBC 032 or two iSBC 016 memory boards)
- Compatible Intellec diskette drives and cable (cable supplied with iSBC 802)
- RS232C compatible terminal

Physical Characteristics

Product distributed on both a single and double density diskette. Each diskette contains both the modules for configuring a tailored system and the predefined software system.

Two ROMs which contain the bootstrap loader.

One cable for the predefined system which provides a connection from the iSBC 204 to the user's Intellec Diskette Drive Chassis (MDS DDS, MDS DDR, and MDS 2DS, MDS 710, MDS 720, MDS 730).

Reference Manuals

The following material is shipped with the product:

9800758	BASIC-80 Reference Manual (SUPPLIED)
9800774	BASIC-80 Pocket Reference (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 802	BASIC-80 Configurable RMX/80 Disk Based Interpreter

BASIC-80 Configurable RMX/80 Disk Based Interpreter is copyrighted and licensed by Intel Corporation. It is available only under a license agreement with Intel. Software may be developed with the BASIC-80 to run on Intel RMX/80 based systems.

RMX/80
REAL-TIME MULTI-TASKING EXECUTIVE

Designed for Intel iSBC 80/10A, iSBC 80/20, and iSBC 80/30 based applications

Completely user configurable

Priority oriented scheduling

Small, efficient nucleus

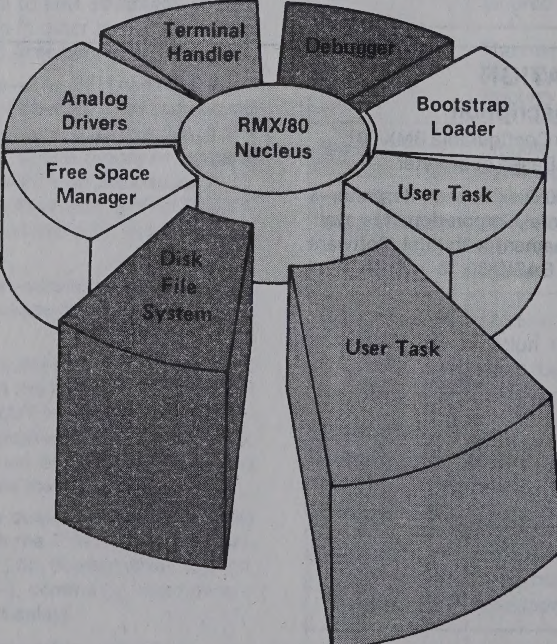
Simple user task interface

Comprehensive I/O support

Library of flexible modules

Structured application environment

The RMX/80 Real-Time Multi-Tasking Executive is an easy-to-use, sophisticated, software system which operates on Intel Single Board Computers. It provides the means to concurrently monitor and control mutiple external events occurring asynchronously in real-time. The RMX/80 executive provides a framework which allows system developers to begin implementing their software immediately and later select the specific Intel Single Board Computer upon which the application will be based. The RMX/80 executive contains all major real-time facilities including priority based system resource allocation, intertask communication and control, interrupt driver control for standard I/O devices, real-time clock control, interrupt handling, as well as many optional features. These facilities eliminate the need for users to design and implement application specific executives, greatly simplifying application design and reducing development time and risk.



FEATURES

The RMX/80 executive provides users of Intel Single Board Computers simple, easy-to-use tools for creating a wide range of application systems. The most popular features of the RMX/80 executive are:

Structured Environment—The RMX/80 executive provides a consistent structure from application to application thus allowing experience gained on one system to be easily transferred to others. Often entire programs may be used in multiple applications.

Simple Interface—The RMX/80 executive provides a simple straightforward program interface for user programs. This interface is consistent throughout the range of facilities offered, reducing the number of concepts which must be learned.

Library Modules—The RMX/80 executive is constructed in a thoroughly modular manner with the full range of facilities being offered in multiple library modules, allowing easy selection of the exact facilities required.

Small Nucleus—The RMX/80 Nucleus provides a small, efficient foundation upon which application systems may be easily built. A wide range of multi-tasking, real-time facilities such as intertask communication and control are included.

Priority Oriented Scheduler—The RMX/80 scheduler insures that the highest priority task which is ready to execute is given system control allowing the application system to be responsive to its external world.

Comprehensive I/O Support—The RMX/80 libraries contain support for a wide range of I/O boards supplied by Intel, simplifying the addition of peripherals to an application system. For applications which require custom boards the RMX/80 device handler philosophy allows easy addition of user written handlers.

User Configurable—RMX/80 executive based applications may be configured from a wide range of facilities, selecting only those which meet the specific requirements of the application system. The resultant system contains only the modules necessary for its use, allowing the RMX/80 executive to fit a wide range of applications from small special purpose dedicated applications to large general purpose systems.

Broad Technological Support—The RMX/80 executive provides support for a range of processor technologies from the 8080 based iSBC 80/10 single board computer to the 8085 based iSBC 80/30 single board computer. Applications are offered an easy upgrade path with the RMX/80 executive which allows greater price/performance to be achieved without expensive software modification.

Extensive Debugging Aids—The RMX/80 executive provides two user oriented, interactive software debugging aids. The debuggers allow memory examination and modification, execution breakpoints, and automatic stack overflow monitoring. These powerful aids allow simplified task debugging and faster application system development.

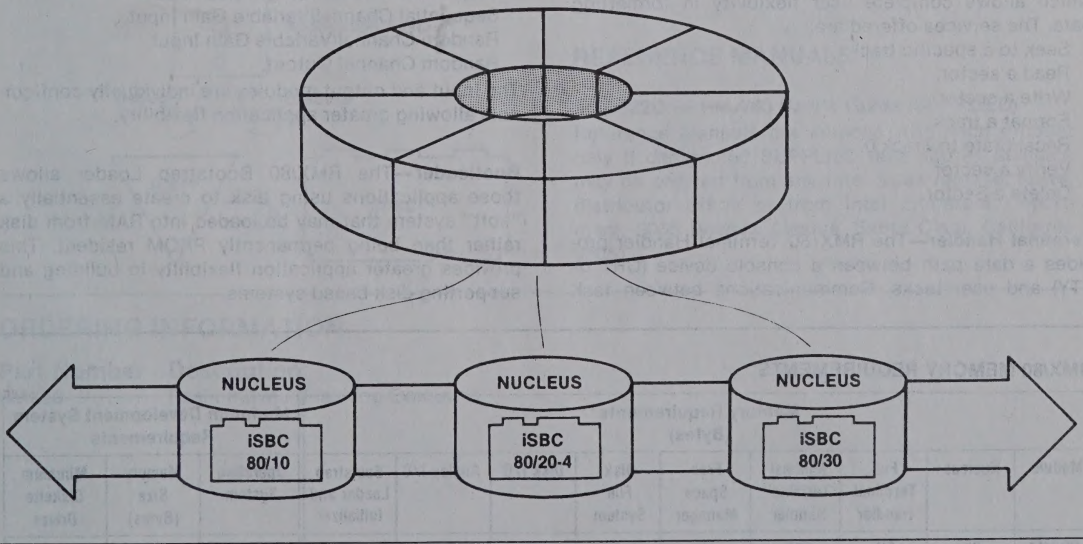


Figure 1. Configuration Flexibility Provides Application Freedom. The RMX/80 executive allows you the freedom to choose from a wide range of iSBC™ family processors and peripherals upon which your application may be built. It allows you to break the software "chain" which ties your application to a single processor type and thereby gain application freedom.

FACILITIES

The various facilities offered by the RMX/80 executive are provided as independent library modules, thus allowing simple inclusion or exclusion depending on the user's specific requirements. These facilities are described below.

Nucleus—The RMX/80 executive provides nuclei for operation on various iSBC single board computers. The nuclei provide real-time scheduling, interrupt handling, intertask communications, and task control. The services offered are:

Send a message from one task to another.
Accept a message from another task.
Wait for a message to be transmitted from another task.
Transmit a special interrupt message to a task.
Suspend execution of a task temporarily.
Continue execution of a previously suspended task.

Disk File System—The RMX/80 Disk File System provides for the filing and retrieving of data using disks. The RMX/80 DFS allows for either Intellec® Development Systems, ISIS-II compatible media format or a user specified format. RMX/80 DFS offers the following services in an ISIS-II compatible media format:

Open a file for processing.
Read data from a file.
Write data to a file.
Position to a specific location within a file.
Close a file to further processing.
Rename a file.
Delete a file.

For those applications which require unique media formats, the RMX/80 executive offers a level of processing which allows complete user flexibility in formatting data. The services offered are:

Seek to a specific track.
Read a sector.
Write a sector.
Format a track.
Recalibrate to Track 0.
Verify a sector.
Delete a Sector.

Terminal Handler—The RMX/80 Terminal Handler provides a data path between a console device (CRT or TTY) and user tasks. Communications between task and device are effected by using the nucleus services SEND and WAIT. Two versions of the Terminal Handler are offered:

Full Terminal Handler—The Full Terminal Handler has a built-in interface to the debugger. It also provides for:

Correction of data previously input.
Automatic buffering of data input prior to a read request.
Priority output path which allows "emergency" messages to bypass any other messages which may be queued for output.
Automatic baud rate search to determine communications terminal speed.

Minimal Terminal Handler—The Minimal Terminal Handler provides a limited feature version of the full Terminal Handler for memory space critical applications. The Minimal Terminal Handler provides for correction of data previously input.

Free Space Manager—The RMX/80 Free Space Manager provides the capability of dynamically allocating RAM memory based upon user requests. Requests may be made for any size memory blocks and will be accommodated based on memory availability. The Free Space Manager services are:

Request Memory
Release Memory.

Analog Handlers—The RMX/80 Analog Handlers provide a convenient mechanism for obtaining and transmitting analog values between user tasks and Intel's iSBC 711, 724 and 732 Analog boards. The Analog Handlers offer a full range of services including:

Repetitive Channel Input.
Sequential Channel/Single Gain Input.
Sequential Channel/Variable Gain Input.
Random Channel/Variable Gain Input.
Random Channel Output.

The input and output modules are individually configurable allowing greater application flexibility.

Bootloader—The RMX/80 Bootstrap Loader allows those applications using disk to create essentially a "soft" system that may be loaded into RAM from disk rather than being permanently PROM resident. This provides greater application flexibility in building and supporting disk based systems.

RMX/80 MEMORY REQUIREMENTS

			Memory Requirements** (Bytes)					
Module	**Nucleus**	**Full Terminal Handler**	**Minimal Terminal Handler**	**Free Space Manager**	**Disk File System**	**Disk I/O**	**Analog I/O**	**Bootstrap Loader and Initializer**
PROM*	2K	3K	600	1K	5.5K	700	800	600
RAM	250	950	120	250	1.6K	100	50	900

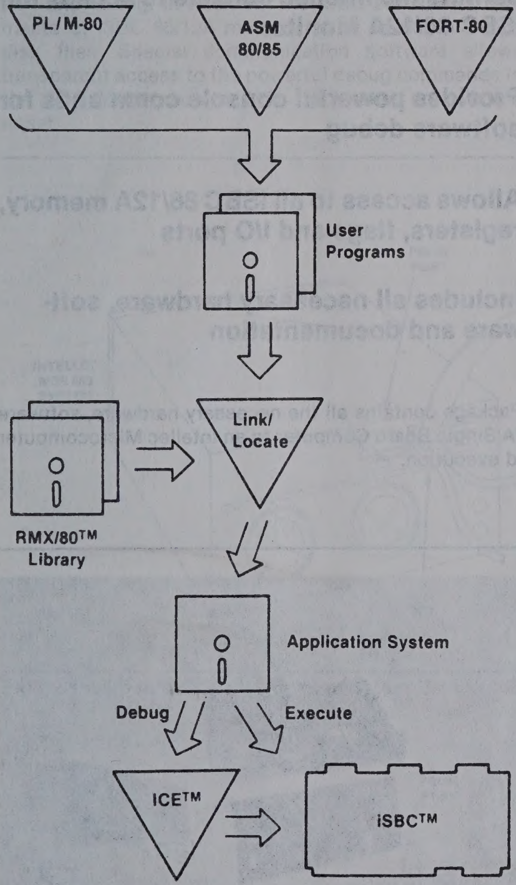
Minimum Development System Requirements		
Operating System	**Memory Size (Bytes)**	**Minimum Diskette Drives**
ISIS-II	48K RAM	2

**All figures are Approximate

*Indicates amount of code which can be configured in PROM.

THE SYSTEMS GENERATION PROCESS

The RMX/80 generation process allows application programs written in PL/M-80, FORTRAN-80, or 8080/8085 Assembly Language to be merged with the specific RMX/80 modules desired. The system may then be debugged using Intel's sophisticated In-Circuit Emulation (ICE™) products or RMX/80 debugger. The final application system is then available for either PROM or Disk Based Systems.



SUPPORTED HARDWARE

Single Board Computers
- iSBC 80/10A Single Board Computer
- iSBC 80/20-4 Single Board Computer
- iSBC 80/30 Single Board Computer

Mass Storage Controllers
- iSBC 201
- iSBC 202
- iSBC 204
- iSBC 206

Analog Boards
- iSBC 711
- iSBC 724
- iSBC 732

RMX/80 EXECUTIVE SHIPPING PACKAGE

- Single and double density diskettes containing:
  - a. iSBC 80/10, 80/20, and 80/30 Nuclei
  - b. Terminal Handler
  - c. Minimal Terminal Handler
  - d. Free Space Manager
  - e. Disk File System
  - f. Analog Handlers
  - g. Debuggers
  - h. Bootstrap Loader
  - i. Configuration Macros
- Software Problem Reports
- Registration Card
- Reference Manual

REFERENCE MANUALS

9800522C — RMX/80 User's Guide (SUPPLIED)

Reference Manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
RMX80	Real-time Multi-tasking Executive

iSBC 957
INTELLEC – iSBC 86/12A INTERFACE AND EXECUTION PACKAGE

Establishes communication between the iSBC 86/12A and the Intellec Development Systems to aid in MCS-86™ software development

Allows full speed execution of MCS-86™ programs

Includes EPROM resident system monitor for iSBC 86/12A

Allows Intellec ISIS-II files to be transferred between iSBC 86/12A and Intellec Microcomputer Development System

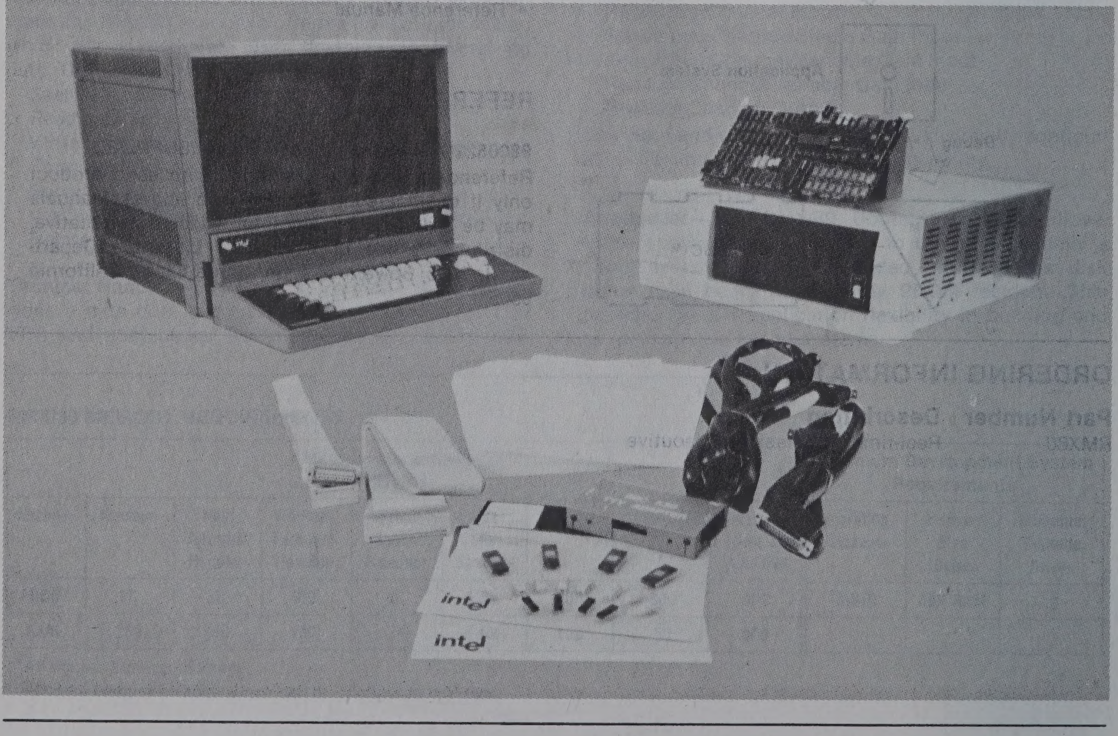
Offers "Virtual Terminal" capability which permits the Intellec console to access the iSBC 86/12A Monitor

Provides powerful console commands for software debug

Allows access to all iSBC 86/12A memory, registers, flags and I/O ports

Includes all necessary hardware, software and documentation

The iSBC 957 Intellec–iSBC 86/12A Interface and Execution Package contains all the necessary hardware, software cables and documentation required to interface an iSBC 86/12A Single Board Computer to an Intellec Microcomputer Development System for software development and full speed execution.



FUNCTIONAL DESCRIPTION

Overview

The iSBC 957 Intellec–iSBC 86/12A Interface and Execution Package extends the software development capabilities of the Intellec Microcomputer Development Systems to the iSBC 86/12 and iSBC 86/12A Single Board Computers. It allows software modules developed under the Intellec resident ISIS-II Operating Systems to be down loaded to the iSBC 86/12A for full-speed execution and debug. In addition, the iSBC 957 allows segments of iSBC 86/12A memory to be saved on floppy disk files. Special communication software allows transparent access to the powerful debug commands in the iSBC 86/12A monitor from the Intellec console terminal.

Software Capabilities

The software included in the iSBC 957 package consists of the iSBC 86/12A monitor residing on four Intel EPROMs which are inserted into sockets on the iSBC 86/12A board. A diskette is also included which contains the Intellec resident communications software that links the iSBC 86/12A with the Intellec Microcomputer Development System. The EPROM resident software creates an execution environment in which object modules may be loaded into the iSBC 86/12A memory, executed at full speed, modified if necessary and saved on the Intellec system floppy disk. The monitor provides the ability to execute selected program segments with breakpoints or by single stepping, examine and modify registers and memory, perform port I/O, move a block of memory, compare blocks of memory, search for a word/

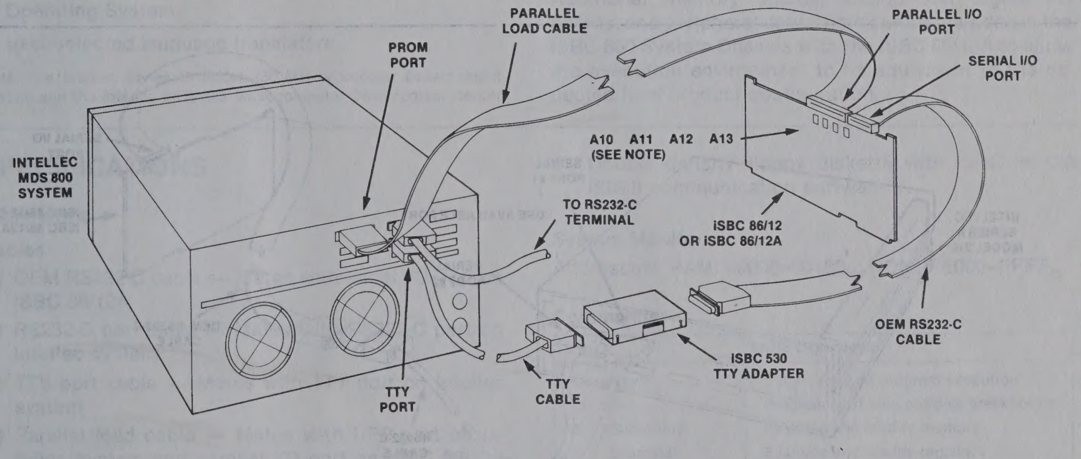
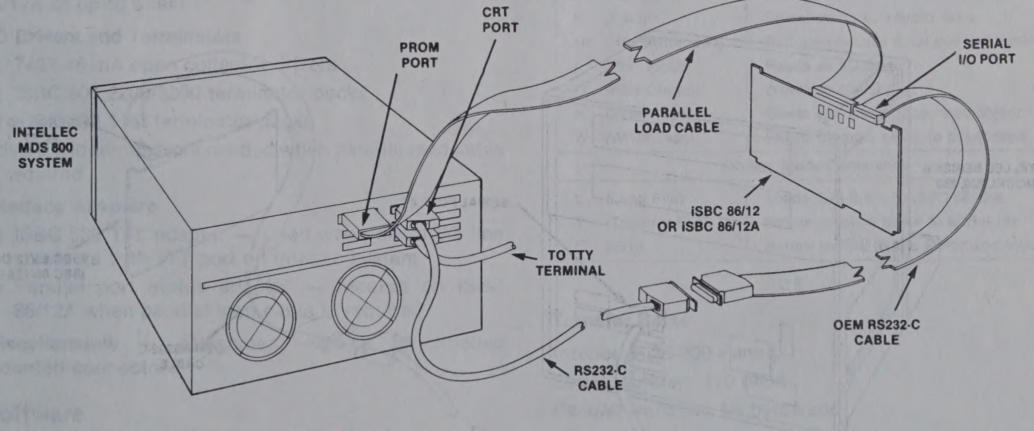

PARALLEL LOAD CABLE
PROM PORT
PARALLEL I/O PORT
SERIAL I/O PORT
INTELLEC MDS 800 SYSTEM
A10 A11 A12 A13 (SEE NOTE)
TO RS232-C TERMINAL
iSBC 86/12 OR iSBC 86/12A
OEM RS232-C CABLE
iSBC 530 TTY ADAPTER
TTY CABLE
TTY PORT

Figure 1a. Intellec MDS-800 Series System Using RS232-C Compatible Terminal


CRT PORT
PROM PORT
SERIAL I/O PORT
INTELLEC MDS 800 SYSTEM
PARALLEL LOAD CABLE
iSBC 86/12 OR iSBC 86/12A
TO TTY TERMINAL
OEM RS232-C CABLE
RS232-C CABLE

Note: A10, A12, A13 — Insert Terminator Pack (supplied)
A11 — Insert Status Adapter Ass'y (supplied)

Figure 1b. Intellec MDS-800 Series System with TTY Terminal

byte value, and perform hex arithmetic. In addition, the monitor provides for the recognition of interrupts via a user-defined table. The program on the diskette contains communication software which passes appropriate console commands to the iSBC 86/12A resident monitor and also interfaces with the ISIS-II operating system to transfer files between the development system diskettes and the iSBC 86/12A.

System Interfacing

The physical interface between the Intellec Microcomputer Development System and the iSBC 86/12A is accomplished with cables supplied with the iSBC 957 package. The cabling arrangement varies depending on whether the system is a member of the Intellec MDS-800 family or one of the Intellec Series II family.

Intellec MDS-800 Interface — In the case of the Intellec MDS-800 family, cables connect the serial I/O port of the iSBC 86/12A to the available serial port on the Intellec system (if the TTY port is used for the iSBC 86/12A interface, the iSBC 530 TTY adapter is inserted into the line). (See Figure 1.) This serial port implements the communication link from the Intellec console terminal to the iSBC 86/12A resident monitor via the Intellec based communication software and is used to pass commands to the iSBC 86/12A. Additionally, a cable is run from the Universal PROM Programmer (UPP) port on the Intellec system to the parallel I/O port on the iSBC 86/12A. The necessary terminators/line drivers and a status adapter assembly are also included to complete this parallel interface on the iSBC 86/12A. This interconnection is used for transferring the ISIS-II disk files between the development system and the iSBC 86/12A.

Intellec Series II Interface — For Intellec Series II Development Systems the connection between it and the iSBC 86/12A is accomplished with a single serial line in-

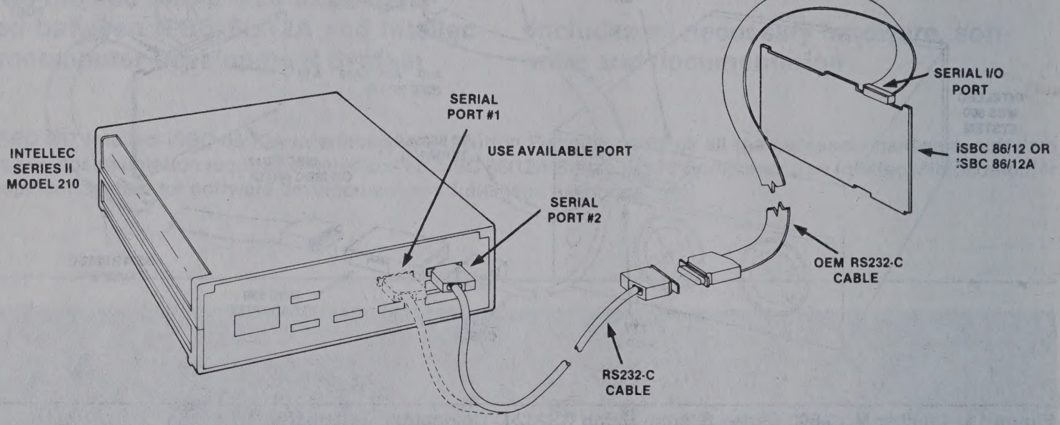

INTELLEC
SERIES II
MODEL 210
SERIAL
PORT #1
USE AVAILABLE PORT
SERIAL
PORT #2
SERIAL I/O
PORT
iSBC 86/12 OR
iSBC 86/12A
OEM RS232-C
CABLE
RS232-C
CABLE

Figure 2a. Intellec Series II Model 210

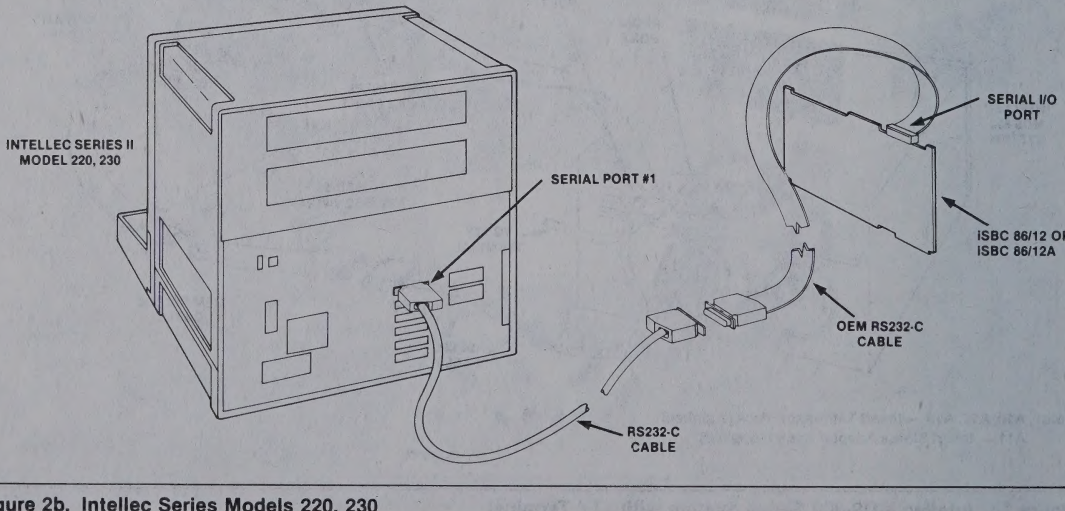

INTELLEC SERIES II
MODEL 220, 230
SERIAL PORT #1
SERIAL I/O
PORT
iSBC 86/12 OR
iSBC 86/12A
OEM RS232-C
CABLE
RS232-C
CABLE

Figure 2b. Intellec Series Models 220, 230

terconnecting the iSBC 86/12A serial port with an available serial port on the Intellec system. All communication including command and data transfer occurs over this serial line. Development systems based on the Intellec Model 210 can use either one of the two available serial ports. (See Figure 2a.) On Models 220 and 230, Serial Port 1 is specified. (See Figure 2b.)

Intellec Environment

An Intellec Microcomputer Development System to be used in conjunction with the iSBC 957 package and an iSBC 86/12A must have the following necessary functionality to support program development and storage:

1. Intellec Development System with 64K bytes of RAM.
2. Console CRT or TTY terminal.
3. Intellec MDS-DDS Dual Double Density Diskette Drive and ISIS-II Operating System or Intellec MDS-2DS Dual Single Density Diskette Drive and ISIS-II Operating System.
4. User-selected language translators.

Note: The Intellec Series II Model 230 Microcomputer Development System and the Intellec MDS-888 Microcomputer Development Center contain all necessary hardware and operating system software to be used with the iSBC 957 package and the iSBC 86/12A.

Execution Environment

A full capability iSBC 86/12A execution environment should include the following components for effective utilization:

1. An iSBC 86/12A Single Board Computer.
2. An iSBC 957 Intellec–iSBC 86/12A Interface and Execution Package.
3. An iSBC 655 or iSBC 660 System Chassis for power and MULTIBUS expansion.
4. One or more iSBC 032, 048, or 064 RAM boards for programs requiring more than 32K bytes of RAM.

Note: The iSBC 86/12A cannot be mounted in the Intellec system and requires a separate operating environment.

Additional memory boards, analog and digital I/O boards, and peripheral controllers can be included in the iSBC 660 System Chassis with the iSBC 86/12A to allow the execution environment to be equivalent to the expected final product configuration.

SPECIFICATIONS

Hardware

Cables

(1) OEM RS232-C cable — Mates with serial I/O port on iSBC 86/12A

(1) RS232-C port cable — Mates with RS232-C port on Intellec system

(1) TTY port cable — Mates with TTY port on Intellec system

(1) Parallel load cable — Mates with UPP port on Intellec system and parallel I/O port on iSBC 86/12A (only used on Intellec MDS-800 series systems)

All cables allow separation of Intellec system and iSBC 86/12A of up to 6 feet.

I/O Drivers and Terminators

(1) 7437 48 mA open collector drivers

(4) iSBC 901 220Ω/330Ω terminator packs

(4) iSBC 902 1 kΩ terminator packs

Drivers and terminators needed when parallel load cable is required

Interface Adapters

(1) iSBC 530 TTY adapter — Used when serial I/O line connects with TTY port on Intellec system

(1) Parallel port status adapter — Mounts on iSBC 86/12A when parallel load cable is required

Miscellaneous — Attachment screws for Intellec mounted connectors

Software

(4) EPROMs with iSBC 86/12A system monitor

(1) Single density floppy diskette with iSBC 86/12A ISIS-II communication software

(1) Double density floppy diskette with iSBC 86/12A ISIS-II communication software

System Monitor

Addresses: RAM: $00000–00180_H$; ROM: $FE000–FFFF_H$

Commands

Basic Commands	
N (Next)	Single stepped program execution
G (Go)	Program start with optional breakpoints
S (Substitute)	Examine and modify memory
X (Examine)	Examine and modify registers
D (Display)	Display blocks of memory
M (Move)	Moves (duplicates) blocks of memory
C (Compare)	Compare two blocks of memory
F (Find)	Searches for byte/word value
H (Hex Arithmetic)	Performs hexadecimal add and subtract
I (Port Input)	Reads an I/O port
O (Port Output)	Writes to an I/O port
R (Read Tape)	Reads and loads paper tape object file
W (Write Tape)	Writes memory block to paper tape
Intellec Mode Commands	
L (Load File)	Loads ISIS-II file to iSBC 86/12A
T (Transfer File)	Writes memory block to ISIS-II file
E (Exit)	Return to ISIS (Basic Command Mode)

Transfer Rates

Intellec MDS-800 Family

Serial transfer: 110 baud

Parallel transfer: 1K bytes/sec

Intellec Series II Family

Serial transfer: Determined by system console (up to 9600 baud)

Reference Manuals

9800645 — iSBC 86/12 Hardware Reference Manual

9803074-01 — iSBC 86/12A Hardware Reference Manual

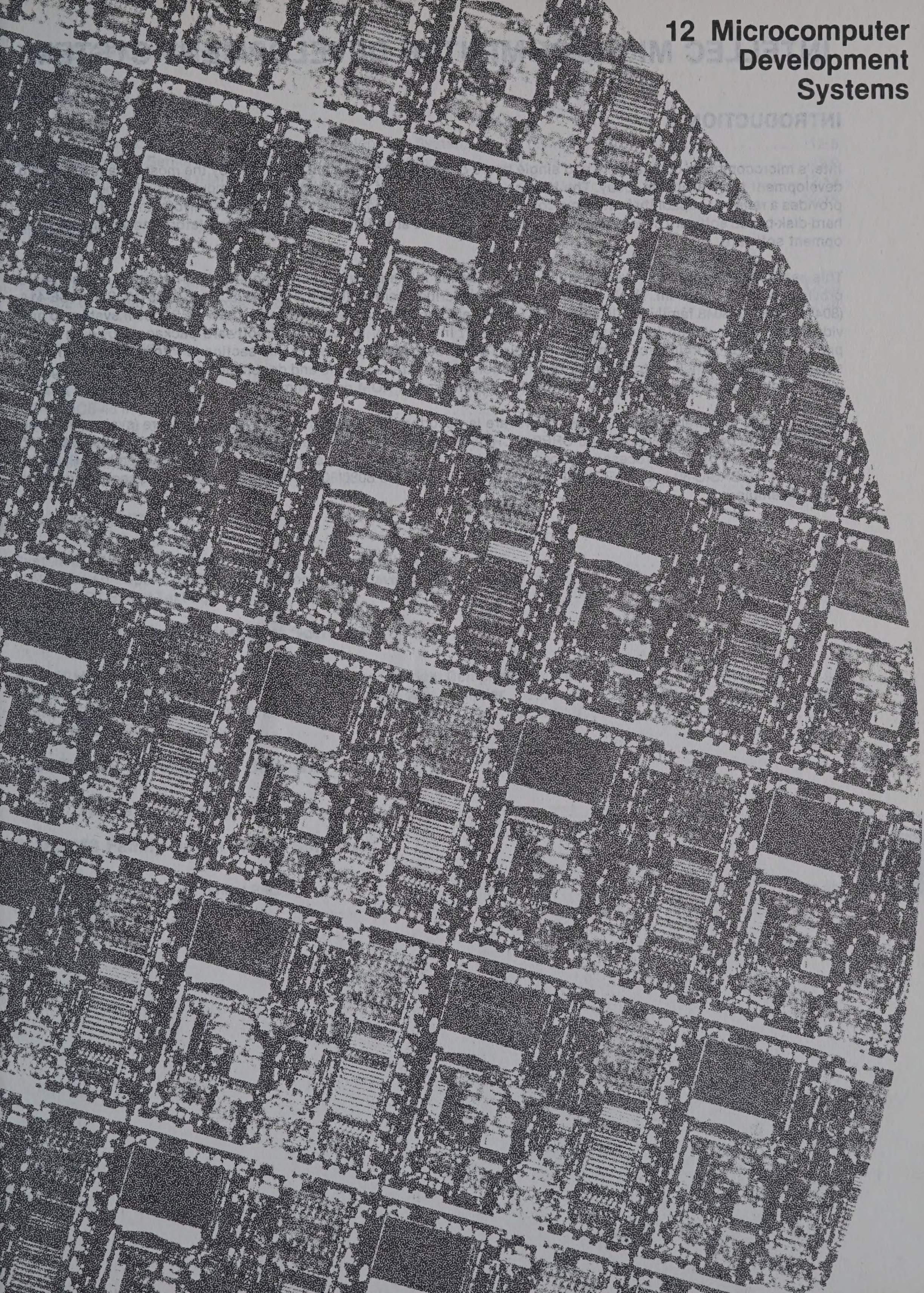
9800743 — iSBC 957 Intellec-iSBC 86/12 Interface and Execution Package User's Guide

9800640 — 8086 Assembly Language Manual

ORDERING INFORMATION

Part Number	Description
SBC 957	Intellec-iSBC 86/12A Interfacing and Execution Package

12 Microcomputer Development Systems



INTELLEC MICROCOMPUTER DEVELOPMENT SYSTEM

INTRODUCTION

Intel's microcomputer components and single board computer products are supported by the most advanced system development tools available today. The Intellec Series II family of compatible microcomputer development systems provides a range of capability from a low cost disk-based edit debug workstation to a high performance, full capability hard-disk-based software development system. Also included are a full line of in-circuit emulators and advanced development software.

This section describes each system in the Intellec Series II line in detail, including standard hardware and software provided with each system. The in-circuit emulators described here include the ICE-80 (8080), ICE-85 (MCS-85), ICE-41A (8041A), ICE-49 (8048 family and ICE-86 (8086 family), all of which may be added to any Intellec Series II system to provide in-circuit emulation for the specified processor. In addition, the multi-ICE software package providing multiprocessor debug with in-circuit emulation is also described. Also included in this section is information on Intellec system peripherals including technical specification for the Intellec single and double density diskette operating systems. Additional peripheral equipment includes the universal PROM programmer.

Finally, Intel's comprehensive full line of software is described including Intellec system software (system monitor, ISIS-II diskette operating system, and CREDIT CRT-based text editor) and development software for 8048, 8080, 8085 and 8086 families of microprocessors. Specifically technical information is provided on the 8048 Assembler, PL/M-80, FORTRAN-80, BASIC-80 and COBOL-80 high level languages, the 8086/8088 software development package and the 8089 Assembler.

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MCS-48 Diskette Based Software Support Package 12-78

8086/8088 Family Development Software

8086/8088 Software Development Package 12-80
8089 Assembler Support Package 12-89

MODEL 220
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development system in one package for MCS-86, MCS-85, MCS-80, and MCS-48 microprocessor families

Single LSI electronics board with CPU, 32K bytes RAM memory, and 4K bytes ROM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Integral 250K-byte floppy disk with total storage capacity expandable to over 2M bytes

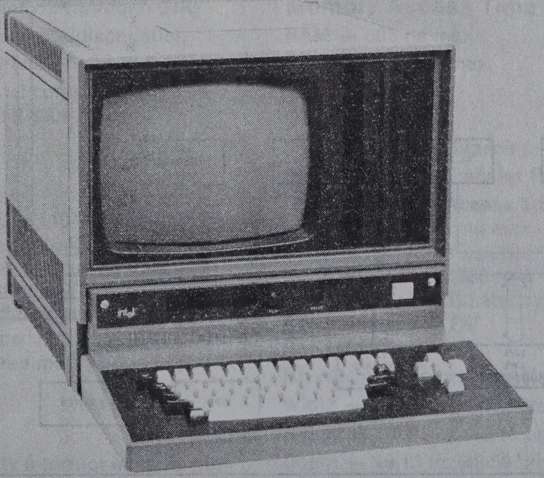
Powerful ISIS-II Diskette Operating System with relocating macroassembler, linker, and locater

Standard MULTIBUS with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 220 Intellec Series II Microcomputer Development System is a complete microcomputer development system integrated into one compact package. It includes a CPU with 32K bytes of RAM memory, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard with cursor controls and upper/lower case capability, and a 250K-byte floppy diskette drive. Powerful ISIS-II Diskette Operating System software allows the Model 220 to be used quickly and efficiently for assembling and debugging programs for Intel's MCS-86, MCS-85, MCS-80, or MCS-48 microprocessor families without the need for paper tape handling. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 220 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 220 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, single floppy diskette drive, and two printed circuit cards. A separate, full ASCII keyboard is connected with a cable.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt, and bus interface circuitry, fashioned from Intel's high-technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second, slave CPU card, is responsible for all remaining I/O control, including the CRT and keyboard interface and floppy disk control. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface, thus in effect creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus, thus leaving the remaining 5 slots in the cardcage available for system expansion. A block diagram of the IOC is shown in Figure 1.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259A interrupt controller, the interrupt system may be user programmed to respond to individual needs.

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 220 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or data terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interfaces for the CRT, keyboard, integral floppy disk and standard Intellec peripherals, including a printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. This CPU controls all I/O operations, as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of ROM are used for CRT screen refresh storage and the floppy disk buffer. These do not occupy any space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT Display — The CRT is a 12-inch raster scan-type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip, programmable CRT controller. The master processor on

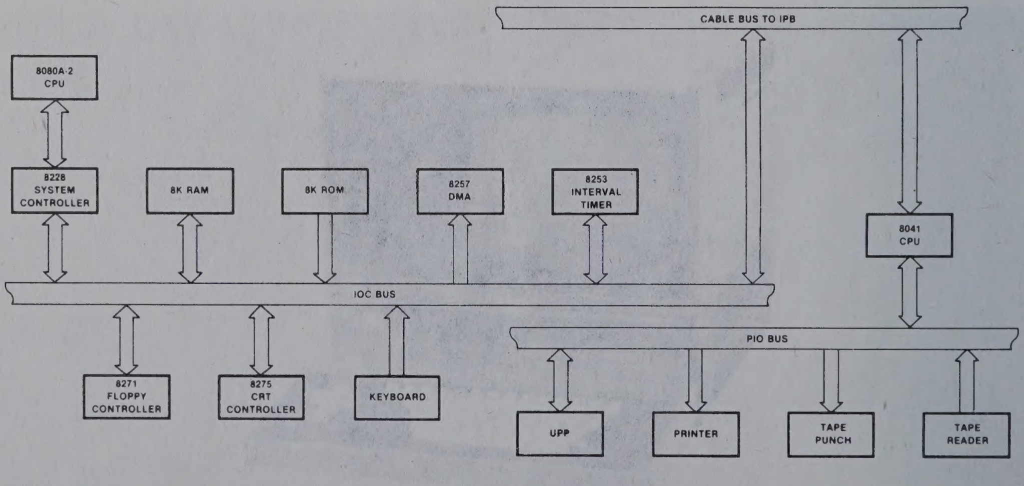


Figure 1. I/O Controller (IOC) Block Diagram for the Model 220 Intellec Series II Microcomputer Development System

the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower-case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter-style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Floppy Disk Drive

The floppy disk drive is controlled by an Intel 8271 single chip, programmable floppy disk controller. It transfers data via an Intel 8257 DMA controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes, and reading status, all upon appropriate commands from the IOC microprocessor.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals, including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate, 8-bit bidirectional data bus. Connectors for the devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259A, as well as to the Intellec Series II bus.

MULTIBUS Capability

All Intellec Series II models implement the industry-standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

Expansion

The Model 220 may be expanded to 64K of RAM and up to 2.25M bytes of on-line diskette storage.

SPECIFICATIONS

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 32K, expandable to 64K with iSBC 032 RAM boards (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

I/O Interfaces

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251A USARTs. Serial Channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

Diskette

Diskette System Capacity — 250K bytes (formatted)

Diskette System Transfer Rate — 160K bits/sec

Diskette System Access Time

Track-to-Track: 10 ms max

Average Random Positioning: 260 ms max

Rotational Speed: 360 rpm

Average Rotational Latency: 83 ms max

Recording Mode: FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 15.81 in. (40.16 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 86 lb (39 kg)

Keyboard

Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.0 cm)
Weight — 6 lb (3 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30.0	7.5
+ 12 ± 5%	2.5	0.2
− 12 ± 5%	0.3	0.05
− 10 ± 5%	1.5	0.15
+ 15 ± 5%	1.5	1.3*
+ 24 ± 5%	1.7	1.2*

*Not available on bus.

AC Requirements

50–60 Hz. 115/230V AC

Equipment Supplied

Model 220 chassis
Integrated processor board (IPB)
I/O controller board (IOC)
CRT and keyboard
250K-byte floppy disk drive
ROM resident system monitor
ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800559 — Intellec Series II Installation and Service Manual (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)

9800555 — Intellec Series II Hardware Interface Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800605 — Intellec Series II System Monitor Source Listing (SUPPLIED)

9800554 — Intellec Series II Schematic Drawing (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-220	Intellec Series II Model 220 microcomputer development system (110V/60 Hz)
MDS-221	Intellec Series II Model 220 microcomputer development system (220V/50 Hz)

MODEL 230 INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development center for Intel MCS-86, MCS-80, MCS-85 and MCS-48 microprocessor families

LSI electronics board with CPU, RAM, ROM, I/O, and interrupt circuitry

64K bytes RAM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Powerful ISIS-II Diskette Operating System software with relocating macroassembler, linker, and locater

1 million bytes (expandable to 2.5M bytes) of diskette storage

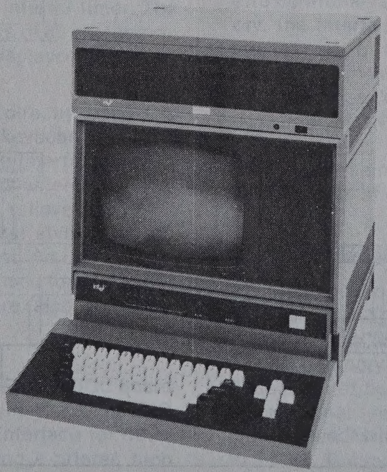
Supports PL/M and FORTRAN high level languages

Standard MULTIBUS with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 230 Intellec Series II Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, a detachable full ASCII keyboard, and dual double density diskette drives providing over 1 million bytes of on-line data storage. Powerful ISIS-II Diskette Operating System software allows the Model 230 to be used quickly and efficiently for assembling and/or compiling and debugging programs for Intel's MCS-86, MCS-80, MCS-85, or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations, leaving the user free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 230 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 230 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, and five printed circuit cards. A separate, full ASCII keyboard is connected with a cable. A second chassis contains two floppy disk drives capable of double-density operation along with a separate power supply, fans, and cables for connection to the main chassis. A block diagram of the Model 230 is shown in Figure 1.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry fashioned from Intel's high technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second slave CPU card is responsible for all remaining I/O control including the CRT and keyboard interface. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface logic, thus, in effect, creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus.

Memory and Control Cards — In addition, 32K bytes of RAM (bringing the total to 64K bytes) is located on a separate card in the main cardcage. Fabricated from Intel's 16K RAMs, the board also contains all necessary address decoding and refresh logic. Two additional boards in the cardcage are used to control the two double-density floppy disk drives.

Expansion — Two remaining slots in the cardcage are available for system expansion. Additional expansion of 4 slots can be achieved through the addition of an Intellec Series II expansion chassis.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259A interrupt controller, the interrupt system may be user programmed to respond to individual needs.

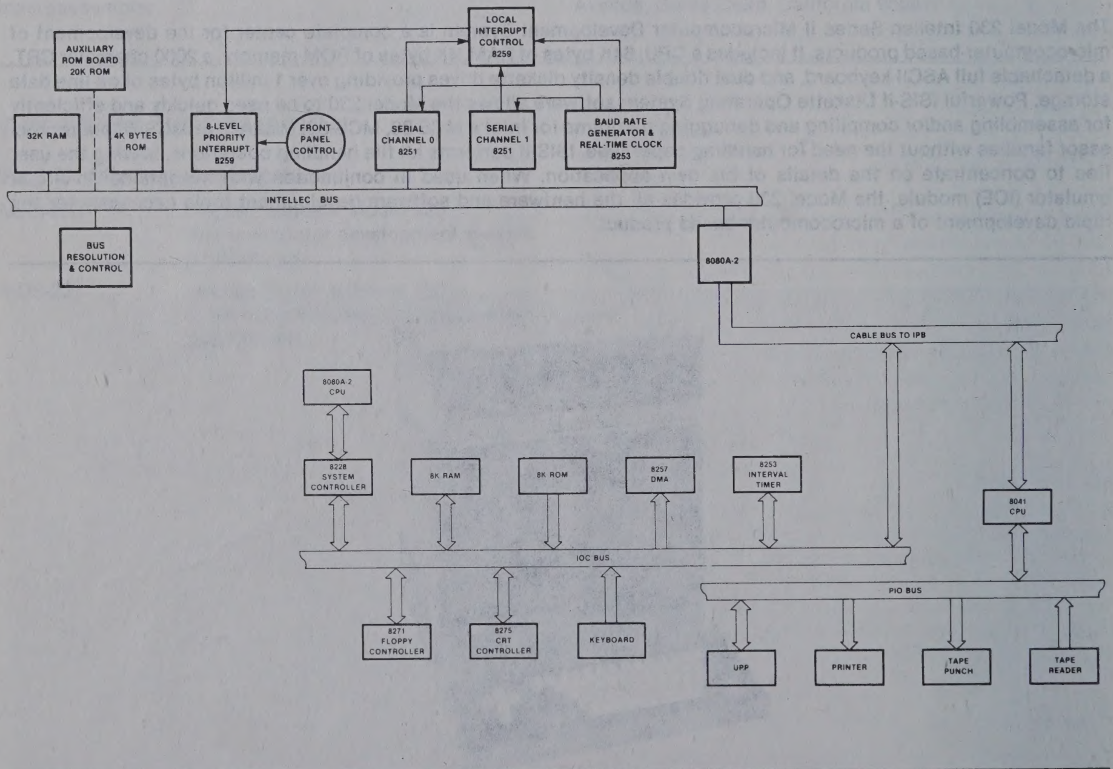

LOCAL INTERRUPT CONTROL 8259
AUXILIARY ROM BOARD 20K ROM
32K RAM
4K BYTES ROM
8-LEVEL PRIORITY INTERRUPT 8259
FRONT PANEL CONTROL
SERIAL CHANNEL 0 8251
SERIAL CHANNEL 1 8251
BAUD RATE GENERATOR & REAL-TIME CLOCK 8253
INTELLEC BUS
BUS RESOLUTION & CONTROL
8080A-2
CABLE BUS TO IPB
8080A-2 CPU
8228 SYSTEM CONTROLLER
8K RAM
8K ROM
8257 DMA
8253 INTERVAL TIMER
8041 CPU
IOC BUS
PIO BUS
8271 FLOPPY CONTROLLER
8275 CRT CONTROLLER
KEYBOARD
UPP
PRINTER
TAPE PUNCH
TAPE READER

Figure 1. Intellec Series II Model 230 Microcomputer Development System Block Diagram

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 230 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251A USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interface for the CRT, keyboard, and standard Intellec peripherals including printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. The CPU controls all I/O operations as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage. These do not occupy space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT

Display — The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip programmable CRT controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel, consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259A, as well as to the Intellec Series II bus.

Diskette System

The Intellec Series II double density diskette system provides direct access bulk storage, intelligent controller, and two diskette drives. Each drive provides ½ million bytes of storage with a data transfer rate of 500,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec Series II system bus, as well as supporting up to four diskette drives. The diskette system records all data in soft sector format. The diskette system is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Diskette Controller Boards — The diskette controller consists of two boards, the channel board and the interface board. These two PC boards reside in the Intellec Series II system chassis and constitute the diskette controller. The channel board receives, decodes and responds to channel commands from the 8080A-2 CPU in the Model 230. The interface board provides the diskette controller with a means of communication with the diskette drives and with the Intellec system bus. The interface board validates data during reads using a cyclic redundancy check (CRC) polynomial and generates CRC data during write operations. When the diskette controller requires access to Intellec system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intellec bus. In addition to supporting a second set of double density drives, the diskette controller may co-reside with the Intel single density controller to allow up to 2.5 million bytes of on-line storage.

MULTIBUS Capability

All Intellec Series II models implement the industry standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

SPECIFICATIONS

Host Processor (IPB)

RAM — 64K (system monitor occupies 62K through 64K)
ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Diskette System Capacity (Basic Two Drives)

Unformatted
Per Disk: 6.2 megabits
Per Track: 82.0 kilobits
Formatted
Per Disk: 4.1 megabits
Per Track: 53.2 kilobits

Diskette Performance

Diskette System Transfer Rate — 500 kilobits/sec
Diskette System Access Time
Track-to-Track: 10 ms
Head Settling Time: 10 ms
Average Random Positioning Time — 260 ms
Rotational Speed — 360 rpm
Average Rotational Latency — 83 ms
Recording Mode — M^2FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)
Height — 15.81 in. (40.16 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 73 lb (33 kg)

Keyboard
Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.86 cm)
Weight — 6 lb (3 kg)

Dual Drive Chassis
Width — 16.88 in. (42.88 cm)
Height — 12.08 in. (30.68 cm)
Depth — 19.0 in. (48.26 cm)
Weight — 64 lb (29 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30	14.25
+ 12 ± 5%	2.5	0.2
− 12 ± 5%	0.3	0.05
− 10 ± 5%	1.5	15
* + 15 ± 5%	1.5	1.3
* + 24 ± 5%	1.7	

*Not available on bus.

AC Requirements — 50/60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Model 230 chassis
Integrated processor board (IPB)
I/O controller board (IOC)
32K RAM board
CRT and keyboard
Double density floppy disk controller (2 boards)
Dual drive floppy disk chassis and cables
2 floppy disk drives (512K byte capacity each)
ROM-resident system monitor
ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800550 — Intellec Series II Installation and Service Guide (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800292 — ISIS-II 8080/8085 Assembler Operator's Manual (SUPPLIED)

9800605 — Intellec Series II Systems Monitor Source Listing (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-230	Intellec Series II Model 230 microcomputer development system (110V/60 Hz)
MDS-231	Intellec Series II Model 230 microcomputer development system (220V/50 Hz)

MODEL 240
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development center for Intel MCS-80™, MCS-85™, MCS-86™, and MCS-48™ microprocessor families

64K bytes RAM memory

Self-test diagnostic capability

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

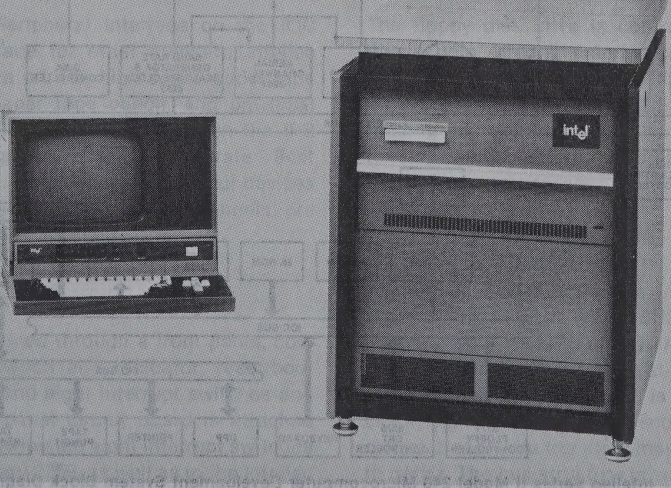
Integral 250K-byte floppy disk plus 7.3 million bytes (expandable to 15.6M bytes) of hard disk storage

Powerful ISIS-II Diskette Operating System software with relocating macroassembler, linker, and locater

Supports PL/M, FORTRAN, BASIC and COBOL high level languages

Software compatible with previous Intellec systems

The Model 240 Intellec Series II Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, a detachable full ASCII keyboard, and 250K-byte floppy diskette drive. A hard disk subsystem provides over 7 million bytes of on-line data storage. Powerful ISIS-II Diskette Operating System software allows the Model 240 to be used quickly and efficiently for assembling and/or compiling and debugging programs for Intel's MCS-80, MCS-85, MCS-86, or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations, leaving the user free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE™) module, the Model 240 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 240 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, single floppy diskette drive, and five printed circuit cards. A separate, full ASCII keyboard is connected with a cable. A free-standing pedestal houses the hard disk drive along with a separate power supply, fans, and cables for connection to the main chassis. A block diagram of the Model 240 is shown in Figure 1.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry fashioned from Intel's high technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second slave CPU card is responsible for all remaining I/O control including the CRT and keyboard interface. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface logic, thus, in effect, creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus.

Memory and Control Cards — In addition, 32K bytes of RAM (bringing the total to 64K bytes) is located on a separate card in the main cardcage. Fabricated from Intel's 16K RAMs, the board also contains all necessary address decoding and refresh logic. Two additional boards in the cardcage are used to control the hard disk drives.

Expansion — Two remaining slots in the cardcage are available for system expansion. Additional expansion of 4 slots can be achieved through the addition of an Intellec Series II expansion chassis.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs. A separate board provides an additional 32K bytes of RAM.

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 240 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interface for

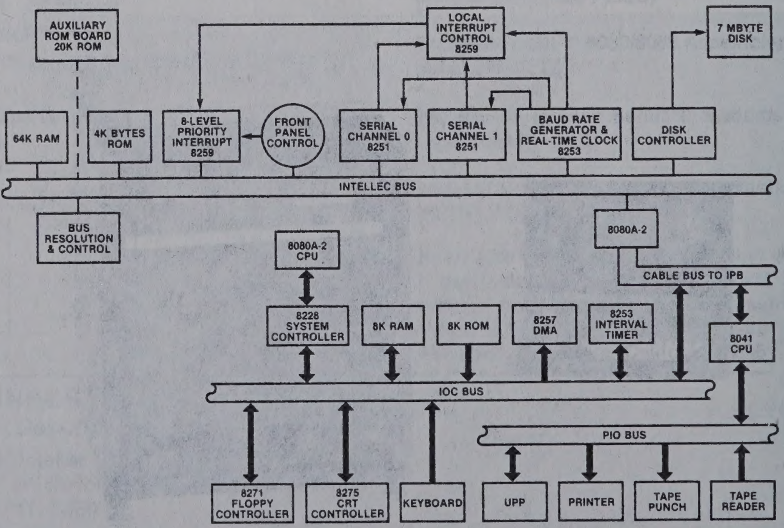

AUXILIARY ROM BOARD 20K ROM
LOCAL INTERRUPT CONTROL 8259
7 MBYTE DISK
64K RAM
4K BYTES ROM
8-LEVEL PRIORITY INTERRUPT 8259
FRONT PANEL CONTROL
SERIAL CHANNEL 0 8251
SERIAL CHANNEL 1 8251
BAUD RATE GENERATOR & REAL-TIME CLOCK 8253
DISK CONTROLLER
INTELLEC BUS
BUS RESOLUTION & CONTROL
8080A-2 CPU
8080A-2
CABLE BUS TO IPB
8228 SYSTEM CONTROLLER
8K RAM
8K ROM
8257 DMA
8253 INTERVAL TIMER
8041 CPU
IOC BUS
PIO BUS
8271 FLOPPY CONTROLLER
8275 CRT CONTROLLER
KEYBOARD
UPP
PRINTER
TAPE PUNCH
TAPE READER

Figure 1. Intellec Series II Model 240 Microcomputer Development System Block Diagram

the CRT, keyboard, and standard Intellec peripherals including printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. The CPU controls all I/O operations as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage. These do not occupy space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT

Display — The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single-chip programmable CRT controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters is displayed, including lower case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board provides interface for other standard Intellec peripherals including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel, consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

Disk System

The Intellec Series II Hard Disk System provides direct access bulk storage, intelligent controller, and a disk drive containing one fixed platter and one removable cartridge. Each provides 3.5 million bytes of storage with a data transfer rate of 2.5 Mbits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec Series II system bus, as well as supporting up to 2 disk drives. The disk system records all data in Double Frequency (FM) on 2 surfaces per platter. Each platter can be write protected by a front panel switch. The disk system is capable of performing six different operations: recalibrate, seek, format track, write data, read data, and verify CRC.

Disk Controller Boards — The disk controller consists of two boards, the channel board and the interface board. These two PC boards reside in the Intellec Series II system chassis and constitute the disk controller. The channel board receives, decodes and responds to channel commands from the 8080A-2 CPU in the Model 240. The interface board provides the disk controller with a means of communication with the disk drives and with the Intellec system bus. The interface board validates data during reads using a cyclic redundancy check (CRC) polynomial and generates CRC data during write operations. When the disk controller requires access to Intellec system memory, the channel board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The channel board also acknowledges I/O commands as required by the Intellec bus. In addition to supporting a second drive, the disk controller may co-reside with the Intel double-density controller to allow up to 17 million bytes of on-line storage.

Floppy Disk Drive

The floppy disk drive is controlled by an Intel 8271 single chip, programmable floppy disk controller. It transfers data via an Intel 8257 DMA controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes, and reading status, all upon appropriate commands from the IOC microprocessor.

MULTIBUS™ Capability

All Intellec Series II models implement the industry standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

SPECIFICATIONS

Host Processor (IPB)

RAM — 64K (system monitor occupies 62K through 64K)
ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Disk Drive

Type — 5440 top loading cartridge and one fixed platter
Tracks per Inch — 200
Mechanical Sectors per Track — 12
Recording Technique — double frequency (FM)
Tracks per Surface — 400
Density — 2,200 bits/inch
Bits per Track — 62,500
Recording Surfaces per Platter — 2

Disk System Capacity

Per Surface — 15M bits
Per Platter — 29M bits
Per Drive — 59M bits
Per Drive — 7.3M bytes (formatted)

Disk Performance

Disk Transfer Rate — 2.5M bits/sec
Disk System Access Time —
Track to Track: 13 ms max
Full Stroke: 100 ms
Rotational Speed: 2,400 rpm

Diskette

Diskette System Capacity — 250K bytes (formatted)
Diskette System Transfer Rate — 160K bits/sec
Diskette System Access Time —
Track to Track: 10 ms max
Average Random Positioning: 260 ms
Rotational Speed: 360 rpm
Average Rotational Latency: 83 ms
Recording Mode: FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)
Height — 15.81 in. (40.16 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 73 lb. (33 kg)

Keyboard

Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.86 cm)
Weight — 6 lb. (3 kg)

Disk Drive on Pedestal

Width — 18.5 in. (47.0 cm)
Height — 34.0 in. (86.4 cm)
Depth — 29.75 in. (75.6 cm)
Weight — 202 lb. (92 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30	17.0
+12 ± 5%	2.5	1.1
−12 ± 5%	0.3	0.1
−10 ± 5%	1.0	0.08
+15 ± 5%*	1.5	1.5
+24 ± 5%*	1.7	1.7

*Not available on bus.

AC Requirements for Mainframe and 2 Drives —
110V, 60Hz — 16A (Mainframe — 5.9, 5.0 each drive)
220V, 50Hz — 8.6A (Mainframe — 3.1, 3.0 each drive)

Environmental Characteristics

Operating Temperature — 16°C to 32°C (90°F)
Humidity — 20% to 80%

Equipment Supplied

Model 240 Chassis
Integrated Processor Board (IPB)
I/O Controller Board (IOC)
32K RAM Board
CRT and Keyboard
One Hard Disk Drive, Pedestal Mounted
Hard Disk Controller (two boards) with Cables
ROM-Resident System Monitor
ISIS-II System Diskette with MCS-80/MCS-85 Macroassembler
Disk Cartridge (blank 5440 type)

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800559 — Intellec Series II Installation and Service Guide (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800292 — ISIS-II 8080/8085 Assembler Operator's Manual (SUPPLIED)

9800605 — Intellec Series II Systems Monitor Source Listing (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

9800943 — Hard Disk Subsystem Operation and Checkout (SUPPLIED)

Additional manuals may be ordered from any Intel sales representative or distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-240	Intellec Series II Model 240 Microcomputer Development System (110 V/60 Hz)
MDS-241	Intellec Series II Model 240 Microcomputer Development System (220 V/50 Hz)

EXPANSION CHASSIS
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Four expansion slots for Intellec Series II systems

Internal power supply

Snug fit beneath all Intellec Series II units

Cable connectable to main Intellec bus

Standard Intellec MULTIBUS with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

The Intellec Series II Expansion Chassis provides four expansion slots for use with Intellec Series II microcomputer development systems. With its own separate power supply, the expansion chassis may be fully loaded with any boards needed to expand a user's Intellec Series II system. With the addition of the expansion chassis, Intellec Series II Models 220 and 230 contain a total of ten slots, sufficient for any configuration Intellec Series II system. The Intellec Series II Expansion Chassis is a compact chassis with a four slot cardcage, power supply, fans, and cable assemblies. It is designed to fit under any Intellec Series II system, connect directly to the system bus through an opening in the top of the chassis, and provide additional slots for the system users. The power supply is linked directly to the main chassis power supply, allowing power to flow to both chassis when the main power is turned on.

SPECIFICATIONS

Physical Characteristics

Width — 17.37 in. (44.12 cm)
Height — 4.81 in. (17.22 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 42 lb. (19 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	System Requirements
+ 5 ± 5%	24	None
+ 12 ± 5%	2.0	None
− 12 ± 5%	0.3	None
− 10 ± 5%	1.0	None

AC Requirements — 50-60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Expansion chassis
Cables

Reference Manuals

9800550 — Intellec Series II Installation and Service Guide (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-201	Intellec Series II expansion chassis

INTELLEC® SINGLE/DOUBLE DENSITY FLEXIBLE DISK SYSTEM

Flexible Disk system providing high speed Input/Output and data storage for Intellec Microcomputer Development Systems

Available in both single density and double density systems

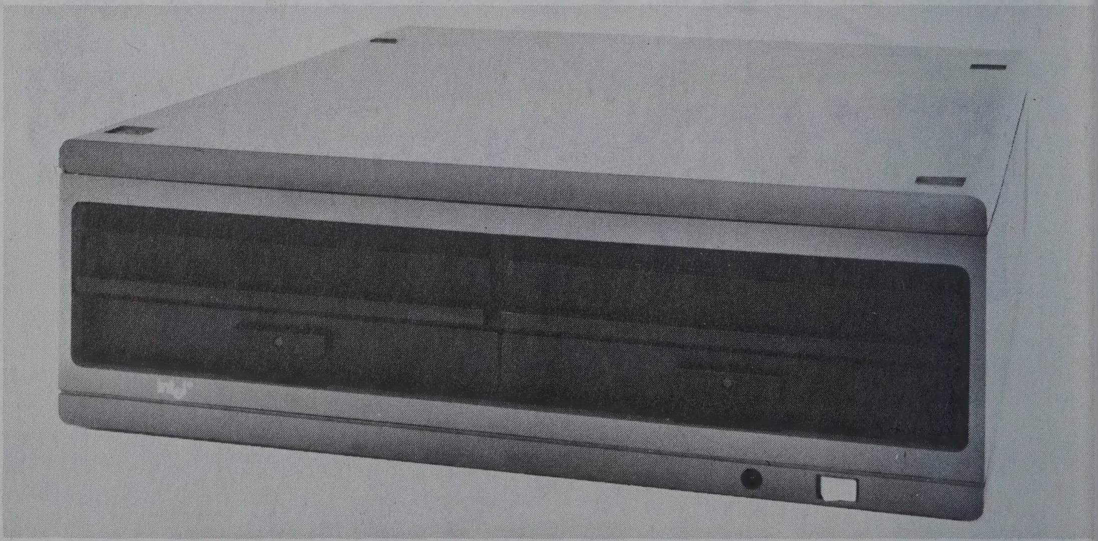
Data recorded on single density flexible disk is in IBM soft-sectored format which allows ¼ million byte data capacity with up to 200 files per flexible disk

Data recorded on double density flexible disk is in soft-sectored format which allows ½ million byte data capacity with up to 200 files per flexible disk

Associated software supports up to four double density drives and two single density drives, providing up to 2.5 Megabytes of storage in one system

Dynamic allocation and deallocation of flexible disk sectors for variable length files

The Intellec® Flexible Disk System is a sophisticated, general purpose, bulk storage peripheral for use with the Intellec Microcomputer Development System. The use of a flexible disk operating system significantly reduces program development time. The software system known as ISIS-II (Intel System Implementation Supervisor), provides the ability to edit, assemble, compile, link, relocate, execute and debug programs, and performs all file management tasks for the user.

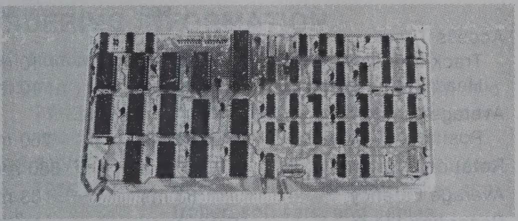


FLEXIBLE DISK SYSTEM

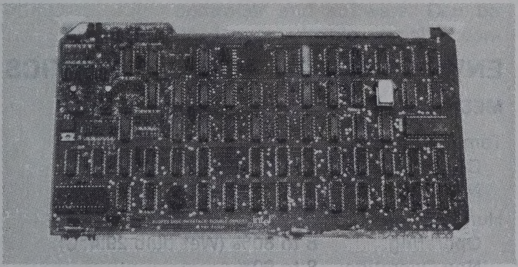
HARDWARE

The Intellec® flexible disk system provides direct access bulk storage, intelligent controller, and two flexible disk drives. Each single density drive provides ¼ million bytes of storage with a data transfer rate of 250,000 bits/second. The double density drive provides ½ million bytes of storage with a data transfer rate of 500,000 bits/second. The controllers are implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controllers provide interface to the Intellec System bus. Each single density controller will support two drives. Each double density controller will support up to four drives. The flexible disk system records all data in soft sector format.

The single/double density flexible disk controllers each consists of two boards, the Channel Board and the Interface Board. These two printed circuit boards reside in the Intellec System chassis. The boards are shown in the photograph, and are described in more detail in the following paragraphs.



SINGLE/DOUBLE DENSITY CHANNEL BOARD



DOUBLE DENSITY INTERFACE BOARD
(SINGLE DENSITY INTERFACE BOARD
IS SIMILAR TO THE ONE SHOWN ABOVE)

CHANNEL BOARD

The *Channel Board* is the primary control module within the flexible disk system. The Channel Board receives, decodes, and responds to channel commands from the Central Processor Unit (CPU) in the Intellec system. The Channel Board can access a block of Intellec system memory to determine the particular flexible disk operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 × 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

This board is the same for either single or double density drives, except that the Series 3000 microcode is different.

INTERFACE BOARD

The *Interface Board* provides the flexible disk controller with a means of communication with the flexible disk drives, as well as with the Intellec system bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the flexible disk platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the flexible disk, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

When the flexible disk controller requires access to Intellec system memory, the Interface Board requests the DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intellec bus.

The Flexible Disk System is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

The channel board is different for single and double density drives, due to the different recording techniques used. The single density controller boards support one set of dual single density drives. The double density controller boards support up to two sets of dual double density drives (four drives total).

The double density controller may co-reside with the Intel single density controller to allow conversion of single density flexible disk to double density format, and provide up to 2.5M bytes of storage.

FLEXIBLE DISK DRIVE MODULES

Each flexible disk drive consists of read/write and control electronics, drive mechanisms, read/write head, track positioning mechanism, and the removable flexible disk platter. These components interact to perform the following functions:

- Interpret and generate control signals
- Move read/write head to selected track
- Read and write data

ASSOCIATED SOFTWARE — INTEL SYSTEMS IMPLEMENTATION SUPERVISOR (ISIS-II)

The Flexible Disk Drive System is to be used in conjunction with the ISIS-II Operating System. ISIS-II provides total file management capabilities, file editing, library management, run-time supports, and utility management.

ISIS-II provides automatic implementation of random access disk files. Up to 200 files may be stored on each ¼ million byte flexible disk for single density system or on each ½ million byte flexible disk for double density system. For more information, see the ISIS-II data specification sheet.

ISIS-II OPERATIONAL ENVIRONMENTAL

ISIS-II

32K bytes RAM memory
48K bytes when using Assembler Macro feature
64K bytes when using PL/M or Fortran
System Console
Single or Double density Flexible Disk Drive

HARDWARE SPECIFICATIONS

MEDIA

Single Density	Double Density
Flexible Disk	Double Density Specified Flexible Disk
One Recording Surface	One Recording Surface
IBM Soft Sector Format	Soft Sector Format
77 Tracks/Diskette	77 Tracks/Diskette
26 Sectors/Track	52 Sectors/Track
128 Bytes/Sector	128 Bytes/Sector

PHYSICAL CHARACTERISTICS

CHASSIS AND DRIVES

Mounting: Table-Top
Height: 5.7 in. (14.5 cm)
Width: 17.6 in. (44.7 cm)
Depth: 19.4 in. (49.3 cm)
Weight: 43.0 lb. (19.5 kg)

ELECTRICAL CHARACTERISTICS

CHASSIS

DC Power Supplies
Supplied Internal to the Cabinet
AC Power Requirements
3-wire input with center conductor (earth ground) tied to chassis
Single-phase, 115 VAC; 60 Hz; 1.2 Amp Maximum (For a Typical Unit)
230 VAC; 50 Hz; 0.7 Amp Maximum (For a Typical Unit)

FLEXIBLE DISK OPERATING SYSTEM CONTROLLER

DC Power Requirements (All power supplied by Intellec Development System)

CHANNEL BOARD

Single Density	Double Density
5V @ 3.75A (typ), 5A (max)	5V @ 3.75A (typ), 5A (max)

INTERFACE BOARD

Single Density	Double Density
5V @ 1.5A (typ), 2.5A (max)	5V @ 1.5A (typ), 2.5A (max) −10V @ 0.1A (typ), 0.2A (max)

FLEXIBLE DISK DRIVE PERFORMANCE SPECIFICATION

	Single Density	Double Density
Capacity (Unformatted):		
Per Disk	3.1 megabits	6.2 megabits
Per Track	41 kilobits	82 kilobits
Capacity (Formatted):		
Per Disk	2.05M bits	4.10 megabits
Per Track	26.6K bits	53.2 kilobits
Data Transfer Rate	250 kilobits/sec	500 kilobits/sec
Access Time:		
Track-to-Track	10 ms	10 ms
Head Settling Time	10 ms	10 ms
Average Random Positioning Time	260 ms	260 ms
Rotational Speed	360 rpm	360 rpm
Average Latency	83 ms	83 ms
Recording Mode	Frequency Modulation	M^2FM

ENVIRONMENTAL CHARACTERISTICS

MEDIA

Temperature:
Operating: 15.6°C to 51.7°C
Non-Operating: 5°C to 55°C
Humidity:
Operating: 8 to 80% (Wet bulb 29.4°C)
Non-Operating: 8 to 90%

DRIVES AND CHASSIS

Temperature:
Operating: 10°C to 38°C
Non-Operating: −35°C to 65°C
Humidity:
Operating: 20% to 80% (Wet bulb 26.7°C)
Non-Operating: 5% to 95%

CONTROLLER BOARDS

Temperature:
Operating: 0 to 55°C
Non-Operating: −55°C to 85°C
Humidity:
Operating: Up to 95% relative humidity without condensation
Non-Operating: All conditions without condensation of water or frost

EQUIPMENT SUPPLIED

SINGLE DENSITY	DOUBLE DENSITY
Cabinet, Power Supplies, Line Cord, Two Drives	Cabinet, Power Supplies, Line Cord, Two Drives
Single Density FDC Channel Board	Double Density FDC Channel Board
Single Density FDC Interface Board	Double Density FDC Interface Board
Dual Auxiliary Board Connector	Dual Auxiliary Board Connector
Flexible Disk Controller Cable	Flexible Disk Controller Cable
Flexible Disk Peripheral Cable	Flexible Disk Peripheral Cable
Hardware Reference Manual	Hardware Reference Manual
Reference Schematics	Reference Schematics
ISIS-II Single Density System Disk	ISIS-II Double Density System Disk
ISIS-II System User's Guide	ISIS-II System User's Guide

OPTIONAL EQUIPMENT

MDS-BLD	10 Blank Flexible Disks
MDS-730/731	Second Drive Cabinet with two additional drives

ORDERING INFORMATION

Part Number	Description
MDS-710/110V 711/220V	Flexible Disk drive unit with two drives, single density drive controller, software, and cables.
MDS-720/110V 721/220V	Flexible Disk drive unit with two drives, double density drive controller, software, and cables.
MDS-730/110V 731/220V	Add-on drive unit with two drives and double density cable, without controller and software. Can be used with double density controller.

UPP-103*
UNIVERSAL PROM PROGRAMMER

Replaces UPP-101, UPP-102 Universal PROM Programmers

Intellec development system peripheral for PROM programming and verification

Provides personality cards for programming all Intel PROM families

Provides zero insertion force sockets for both 16-pin and 24-pin PROMs

Universal PROM mapper software provides powerful data manipulation and programming commands

Provides flexible power source for system logic and programming pulse generation

Holds two personality cards to facilitate programming operations using several PROM types

The UPP-103 Universal PROM Programmer is an Intellec system peripheral capable of programming and verifying all of the Intel programmable ROMs (PROMs). In addition, the UPP-103 programs the PROM memory portions of the 8748 microcomputer, 8741 UPI, the 8755 PROM and I/O chip and the 2920 signal processor. Programming and verification operations are initiated from the Intellec development system console and are controlled by the universal PROM mapper (UPM) program.

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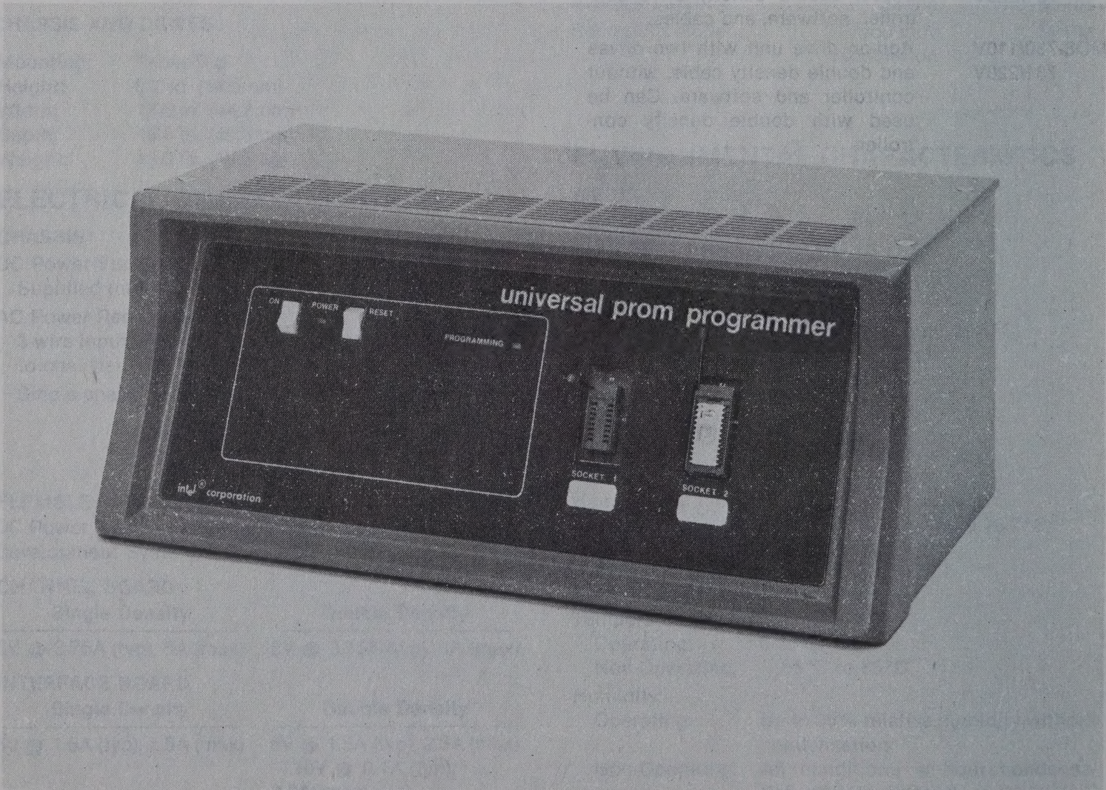


FUNCTIONAL DESCRIPTION

Universal PROM Programmer

The basic Universal PROM Programmer (UPP) consists of a controller module, two personality card sockets, a front panel, power supplies, a chassis, and an Intellec development system interconnection cable. An Intel 4040-based intelligent controller monitors the commands from the Intellec System and controls the data transfer interface between the selected PROM personality card and the Intellec memory. A unique personality card contains the appropriate pulse generation functions for each Intel PROM family. Programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card. The front panel contains a power-on switch and indicator, a reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides power for system logic and for PROM programming pulse generation. The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19-inch RETMA cabinet.

Universal PROM Mapper

The Universal PROM Mapper (UPM) is the software program used to control data transfer between paper tape or diskette files and a PROM plugged into the Universal PROM Programmer. It uses Intellec system memory for intermediate storage. The UPM transfers data in 8-bit HEX, BNPF, or binary object format between paper tape or diskette files and the Intellec system memory. While the data is in Intellec system memory, it can be displayed and changed. In addition, word length, bit position, and data sense can be adjusted as required for the PROM to be programmed. PROMs may also be duplicated or altered by copying the PROM contents into the Intellec system memory. Easy to use program and compare commands give the user complete control over programming and verification operations. The UPM eliminates the need for a variety of personalized PROM programming routines because it contains the programming algorithms for all Intel PROM families. The UPM (diskette based version) is included with the Universal PROM Programmer.

SPECIFICATIONS

Hardware Interface

Data — Two 8-bit unidirectional buses

Commands — 3 write commands, 2 read commands, one initiate command

Physical Characteristics

Width — 6 in. (14.7 cm)

Height — 7 in. (17.2 cm)

Depth — 17 in. (41.7 cm)

Weight — 18 lb (8.2 kg)

Electrical Characteristics

AC Power Requirements — 50–60 Hz; 115/230V AC: 80W

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Optional Equipment

Personality Cards

UPP-816: 2716 personality card

UPP-832: 2732 personality card

UPP-848: 8748, 8741 personality card with 40-pin adaptor socket

UPP-865: 3602, 3622, 3602A, 3622A, 3621, 3604, 3624, 3604A, 3624A, 3604AL, 36046-6, 3605, 3605A, 3625, 3625A, 3608, 3628, 3636

UPP-872: 8702A/1702A personality card

UPP-878: 8708/8704/2708/2704 personality card

UPP-955: 8755A personality card with 40-pin adaptor socket

PROM Programming Sockets

UPP-501: 16-pin/24-pin socket pair

UPP-502: 24-pin/24-pin socket pair

UPP-562: Socket adaptor for 3621, 3602, 3622, 3602A, 3622A

UPP-555: Socket adaptor for 3604AL, 36046-6, 3608, 3628, 3636

UPP-566: Socket adaptor for 3605, 3625, 3605A, 3625A

Equipment Supplied

Cabinet

Power supplies

4040 intelligent controller module

Specified zero insertion force socket pair

Intellec development system interface cable

Universal PROM Mapper program (diskette-based version)

Reference Manuals

9800819 — Universal PROM Programmer User's Manual (SUPPLIED)

ORDERING INFORMATION

Part Number	Description
UPP-103	Universal PROM programmer with 16-pin/24-pin socket pair and 24-pin/24-pin socket pair.

ICE-41A
UPI-41A IN-CIRCUIT EMULATOR

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing user UPI-41A devices

Emulates user system UPI-41A devices in real time

Allows user configured system to use static RAM memory for program debug

Provides hardware comparators for user designated break conditions

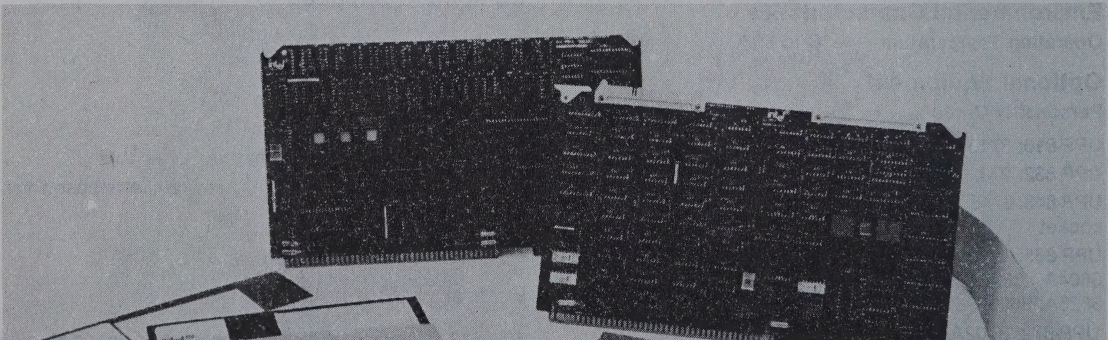
Eliminates need for extraneous debugging tools residing in user system

Collects address, data, and UPI-41A status information on machine cycles emulated

Provides capability to examine and alter UPI-41A registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early in engineering cycle to save development time

The ICE-41A UPI-41A In-Circuit Emulator module is an Intellec system resident module that interfaces to any user configured UPI-41A system. The ICE-41A module interfaces with a UPI-41A pin-compatible plug which replaces the UPI-41A device in the system. With the ICE-41A plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real time trace data. In addition, he can single step the system program during execution. Static RAM memory is available through the ICE-41A module to store UPI-41A programs. The designer may display and alter the contents of program memory, internal UPI-41A registers and flags, and I/O ports. Powerful debug capability is extended into the UPI-41A system while ICE-41A debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in the system.



FUNCTIONAL DESCRIPTION

Debug Capability Inside User System

Intellec memory is used for the execution of the ICE-41A software. The Intellec CRT console and the file handling capabilities provide the designer with the ability to communicate with the ICE-41A module and display information on the operation of the prototype system. The ICE-41A module block diagram is shown in Figure 1.

Symbolic Debugging

Symbol Table — ICE-41A software allows the user to make symbolic references to I/O ports, memory addresses, and data in his program. The user symbol table which is generated along with the object file during a program assembly can be loaded to Intellec memory for access during emulation. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that he may find useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location. In addition, ICE-41A provides symbolic definition of all UPI-41A registers and flags.

Symbolic Reference — Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up addresses of key locations in his program which can change with each assembly. Meaningful symbols from his source program can be used instead. For example, the command:

```
GO FROM .START TILL CODE. RSLT
```

begins execution of the program at the address referenced by the label START in the designer's assembly program. A breakpoint is set to occur the first time the microprocessor executes the program memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-41A software driver supplies them automatically from information stored in the symbol table.

Memory Replacement

The 8741/8741A and 8041/8041A contain internal program and data memory. When the UPI-41A microcomputer is replaced by the ICE-41A socket in a system, the ICE-41A module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-41A module has enough RAM memory available to emulate up to the total 1K control memory capability of the system.

Real-Time Trace

The ICE-41A module captures trace information while the designer is executing programs in real time. The instructions executed, program counter, port values for port 1 and port 2, and the values of selected UPI-41A status lines are stored for the last 255 instruction cycles executed. When retrieved for display, code is disassembled for user convenience. This provides data for determining how the user system was reacting prior to emulating break.

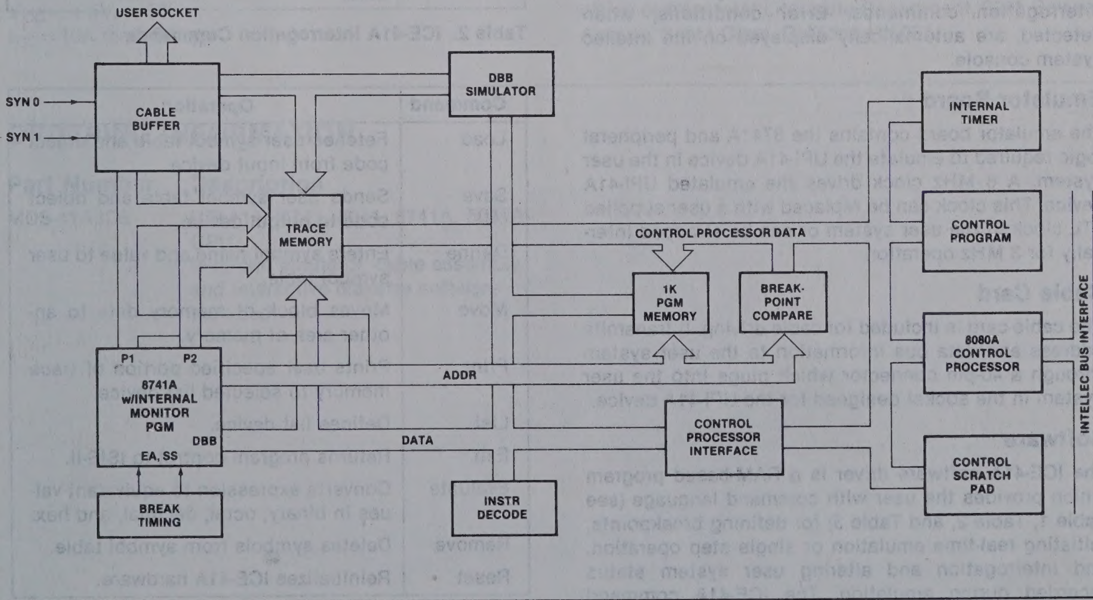

USER SOCKET
SYN 0
SYN 1
CABLE BUFFER
DBB SIMULATOR
TRACE MEMORY
P1
P2
8741A W/INTERNAL MONITOR PGM
DBB
EA, SS
BREAK TIMING
ADDR
DATA
INSTR DECODE
CONTROL PROCESSOR DATA
1K PGM MEMORY
BREAK-POINT COMPARE
CONTROL PROCESSOR INTERFACE
INTERNAL TIMER
CONTROL PROGRAM
8080A CONTROL PROCESSOR
CONTROL SCRATCH PAD
INTELLEC BUS INTERFACE

Figure 1. ICE-41A Module Block Diagram

Integrated Hardware/Software Development

The user prototype systems need no more than a UPI-41A socket and timing logic to begin integration of software and hardware development efforts. Through the ICE-41A module, Intellec system resources can be accessed to replace the prototype system. UPI-41A software development can proceed without the prototype hardware. Hardware designs can be tested using previously tested system software.

Hardware

The ICE-41A module is a microcomputer system utilizing Intel's UPI-41A microprocessor as its nucleus. This system communicates with the Intellec system 8080A processor via direct memory access. Host processor commands and ICE-41A status are interchanged through a DMA channel. ICE-41A hardware consists of two printed circuit boards, the controller board and the emulator board, which reside in the Intellec system chassis. A cable assembly interfaces the ICE-41A module to the user's UPI-41A system. The cable terminates in a UPI-41A pin-compatible plug which replaces any UPI-41A device in the user system.

Controller Board

The ICE-41A module interfaces to the Intellec systems as a peripheral device. The controller board receives commands from the Intellec system and responds through a DMA port. Three 10-bit hardware breakpoint registers are available which can be loaded by the user. While in emulation mode, a hardware comparator is constantly monitoring address lines for a match which will terminate an emulation. The controller board returns real-time trace data, UPI-41A registers, flag and port values, and status information to a control block in the Intellec system when emulation is terminated. This information is available to the user through the ICE-41A interrogation commands. Error conditions, when detected, are automatically displayed on the Intellec system console.

Emulator Board

The emulator board contains the 8741A and peripheral logic required to emulate the UPI-41A device in the user system. A 6 MHz clock drives the emulated UPI-41A device. This clock can be replaced with a user supplied TTL clock in the user system or can be strapped internally for 3 MHz operation.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the UPI-41A device.

Software

The ICE-41A software driver is a RAM-based program which provides the user with command language (see Table 1, Table 2, and Table 3) for defining breakpoints, initiating real-time emulation or single step operation, and interrogation and altering user system status recorded during emulation. The ICE-41A command language contains a broad range of modifiers which provide the user with maximum flexibility in defining the operation to be performed. The ICE-41A software driver is available on diskette and operates in 32K of Intellec RAM memory.

Command	Operation
Enable	Activates breakpoint and display registers for use with go and step commands.
Go	Initiates real-time emulation and allows user to specify breakpoints and data retrieval.
Step	Initiates emulation in single instruction increments. Each step is followed by register dump. User may optionally tailor other diagnostic activity to his needs.
Interrupt	Emulates user system interrupt

Table 1. ICE-41A Emulation Commands

Command	Operation
Display	Prints contents of memory, UPI-41A device registers, I/O ports, flags, pins, real-time trace data, symbol table, or other diagnostic data on list device.
Change	Alters contents of memory, register, output port, or flag. Sets or alters breakpoints and display registers.
Base	Establishes mode of display for output data.
Suffix	Establishes mode of display for input data.

Table 2. ICE-41A Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Move	Moves block of memory data to another area of memory.
Print	Prints user specified portion of trace memory to selected list device.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, octal, decimal, and hex.
Remove	Deletes symbols from symbol table.
Reset	Reinitializes ICE-41A hardware.

Table 3. ICE-41A Utility Commands

SPECIFICATIONS

ICE-41A Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-41A module

Required Software

System monitor
ISIS-II
ICE-41A diskette-based software

System Clock

Crystal controlled 6.0 MHz or 3.0 MHz internal or user supplied TTL external

Physical Characteristics

Printed Circuit Boards

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 8.00 lb (3.64 kg)

Cable Buffer Box

Width: 8.00 in. (20.32 cm)
Height: 4.00 in. (10.16 cm)
Depth: 1.25 in. (3.17 cm)
Flat Cable: 4.00 ft (121.92 cm)
User Cable: 15.00 in. (38.10 cm)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V, \pm 5\%$
$I_{CC} = 10A$ max; 8A typ
$V_{DD} = +12V, \pm 5\%$
$I_{DD} = 100$ mA max; 60 mA typ
$V_{BB} = -10V$
$I_{BB} = 30$ mA

Input Impedance

@ ICE-41A user socket pins:
$V_{IL} = 0.8V$ max; $I_{IL} = 1.6$ mA
$V_{IH} = 2.0V$ min; $I_{IH} = 40\ \mu A$
@ Bus:
$V_{IL} = 0.8V$ max; $I_{IL} = 250\ \mu A$
$V_{IH} = 2.0V$ min; $V_{IH} = 20\ \mu A$

Output Impedance

@ P1, P2:
$V_{OL} = 0.5V$ max; $I_{OL} = 16$ mA
$V_{OH} = V_{CC}$ (10K pullup)
@ Bus:
$V_{OL} = 0.5V$ max; $I_{OL} = 25$ mA
$V_{OH} = 3.65V$ min; $I_{OH} = 1$ mA

Others

$V_{OL} = 0.5V$ max; $I_{OL} = 16$ mA
$V_{OH} = 2.4V$ max; $I_{OH} = 400\ \mu A$

Equipment Supplied

Controller board
Emulator board
Interface cables and buffer module
Operator's manual
ICE-41A diskette based software

Reference Manuals

9800465 — ICE-41A Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-41A-ICE	UPI-41A (8741, 8041, 8741A, 8041A) CPU In-circuit emulator, cable assembly and interactive diskette software included

ICE-49
MCS-48 IN-CIRCUIT EMULATOR

Emulates 8049, 8048, 8748, 8039, 8035, and 8021 Microcomputers*

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing system MCS-48 device

Emulates user system MCS-48 device in real time

Shares static RAM memory with user system for program debug

Provides hardware comparators for user designated break conditions

Eliminates need for extraneous debugging tools residing in user system

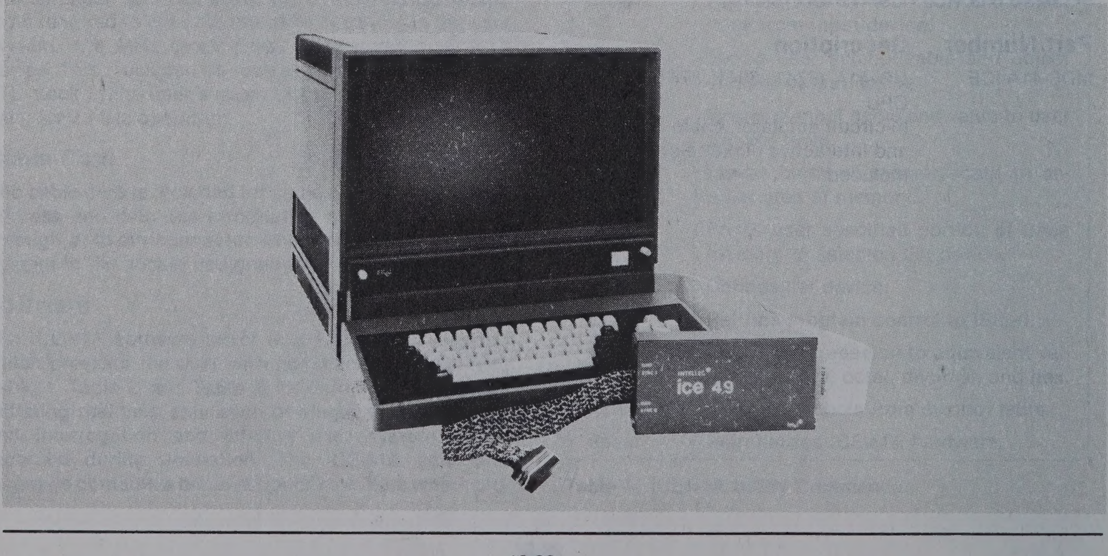
Collects bus, register, and MCS-48 status information on instructions emulated

Provides capability to examine and alter MCS-48 registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-49 MCS-48 In-Circuit Emulator module is an Intellec-resident module that interfaces with any MCS-48 system. The MCS-48 family consists of the 8049, 8048, 8748, 8039, 8035, and 8021 microcomputers. The ICE-49 module interfaces with an MCS-48 system through a cable terminating in an MCS-48 pin-compatible plug which replaces the MCS-48 device in the sytem. With the ICE-49 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real-time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available through the ICE-49 module to emulate MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags and I/O ports. Powerful debug capability is extended into the MCS-48 system while ICE-49 debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in this system.

*EM1 emulator board is also required.



Memory Mapping

The 8049, 8748 and 8048 contain internal program and data memory. Both program and data memory can be expanded using external memory devices.

Internal Memory — When the MCS-48 microcomputer is replaced by the ICE-49 socket in a system, the ICE-49 module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-49 module has enough RAM memory available to emulate up to the total 4K control memory capability of the system. The ICE-49 module also provides for up to 384 bytes of data memory.

External Memory — The ICE-49 module separates replacement control memory into sixteen 256-byte blocks. Replacement external data memory consists of one 256-byte block. Each block of memory can be defined separately as supplied by the user system or supplied by the ICE-49 module. The user may assign ICE-49 equivalent memory to take the place of external memory not yet supplied in his system.

Symbolic Debugging

ICE-49 software provides symbolic definition of all MCS-48 registers, flags, and selected MCS-48 pins. Symbolically defined pseudo registers provide access to the sense of MCS-48 flip flops which enable time, counter, interrupt, and flag-0/flag-1 options. In addition, the user may reference locations in program and data memory, or their contents, symbolically. The user symbol table generated along with the object file during a program assembly may be loaded to Intellec memory for access during emulation. The user is encouraged to add to this symbol table any additional symbolic values for memory addresses, constants, or variables he may find useful during system debugging. Symbols may be substituted for numeric values in any of the ICE-49 commands. Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up those addresses of key locations in his program that can change with each assembly. Meaningful symbols from his source program may be used instead. For example, the command:

```
GO FROM .START TILL XDATA. RSLT WRITTEN
```

begins execution of the program at the address referenced by the label START in the designers assembly program. A breakpoint is set to occur the first time the microprocessor writes to the external data memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-49 software driver supplies them automatically from information stored in the symbol table.

Hardware

The ICE-49 module is a microcomputer system utilizing Intel's 8049 or 8048/8748 microcomputer as its nucleus. The 8049 provides the 8049, 8039 emulation characteristics. The 8048/8748 provides the 8748/8048/8035/8021 emulation characteristics. The ICE-49 module uses an Intel 8080 to communicate with the Intellec host processor via a common memory space. The 8080 also controls an internal ICE-49 bus for intramodule communication. ICE-49 hardware consists of two PC boards, the controller board, and the emulator board, all of which reside in the Intellec chassis. A cable interfaces the ICE-49 boards to the MCS-48 system. The cable terminates in a MCS-48 pin compatible plug which replaces any MCS-48 device in the user system. The ICE-49 module block diagram is shown in Figure 1.

Real-Time Trace

Trace Buffer — While the ICE-49 module is executing the user program, it is monitoring port, program counter, data, and status lines. Values for each instruction cycle executed are stored in a 255 x 44 real-time RAM trace buffer. A resetable timer resident on the controller board counts instruction cycles.

Controller Board

The ICE-49 module talks to the Intellec system as a peripheral device. The controller board receives commands from the Intellec system and responds through the parameter block. Three 15-bit hardware breakpoint registers are available for loading by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match to terminate an emulation. The breakpoint registers provide a signal when a match is detected. The user may disable the emulation break capability and use the signal to synchronize other debug tools. The controller board returns real-time trace data, MCS-48 register, flag, and pin values, and ICE-49 status information, to a control block in the Intellec system when emulation is terminated. This information is available to the user through the ICE-49 interrogation commands. Error conditions, when present, are automatically displayed on the Intellec system console. The controller board also contains static RAM memory, which can be used to emulate MCS-48 program and data memory in real time. 4K of memory is available in sixteen 256-byte pages to emulate MCS-48 PROM or PROM program memory. A 256-byte page of data memory is available to access in place of MCS-48 external data memory. The controller board address map directs the ICE-49 module to access either replacement ICE-49 memory or actual user system external memory in 256-byte segments based on information provided by the user.

Emulator Board

The emulator board contains the 8049* and peripheral logic required to emulate the MCS-48 device in the user system. A software selectable 6 MHz or 3 MHz clock drives the emulated MCS-48 device. This clock can be disabled and replaced with a user supplied TTL clock in the user system.

---

*Use 8048 with internal monitor program when emulating 8748/8048/8035/8021.

FUNCTIONAL DESCRIPTION

Debug Capability Inside User System

The ICE-49 module provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools. The module connects to the user system through the socket provided for the MCS-48 device in the user system. Intellec memory is used for the execution of the ICE-49 software. The Intellec console and file handling capabilities provide the designer with the ability to communicate with the ICE-49 module and display information on the operation of the prototype system. The ICE-49 module block diagram is shown in Figure 1.

Batch Testing

In conjunction with the ISIS-II diskette operating system, the ICE-49 module can run extensive system diagnostics without operator intervention. The designer or test engineer can define a complete diagnostic exercise, which is stored in a file on the diskette. When activated with an ISIS-II submit command, this file can instruct the ICE-49 module to execute the diagnostic routine and store the results in another file on the diskette. Results are available to the designer at his convenience. In this way, routine diagnostics and long term testing may be done without tying up valuable manpower.

Integrated Hardware/Software Development

The user prototype need consist of no more than an MCS-48 socket and timing logic to begin integration of software and hardware development efforts. Through the ICE-49 module mapping capabilities, Intellec system resources can be accessed to replace prototype memory. Hardware designs can be tested using the system software to drive the final product. Thus, the system integration phase, which can be costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

Real-Time Trace

The ICE-49 module captures trace information while the designer is executing programs in real time. The instructions executed, program counter, port values for bus 0, port 1 and port 2, and the values of selected MCS-48 status lines are stored for the last 255 instruction cycles executed. When retrieved for display, code is disassembled for user convenience. This provides data for determining how the user system was reacting prior to emulation break, and is available whether the break was user initiated or the result of an error condition. For more detailed information on the actions of internal registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

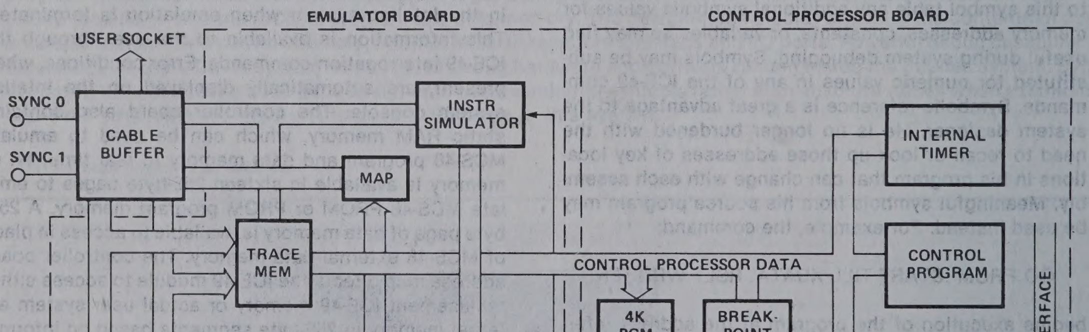

EMULATOR BOARD
CONTROL PROCESSOR BOARD
USER SOCKET
SYNC 0
SYNC 1
CABLE BUFFER
INSTR SIMULATOR
MAP
TRACE MEM
LATCH ADDR
P1
P2A
8049 OR 8048 W/INTERNAL MONITOR PGM
P0
EA,SS
BREAK TIMING
INSTR DECODE
ADDR
DATA
CONTROL PROCESSOR DATA
4K PGM MEM
BREAK-POINT COMPARE
CONTROL PROCESSOR INTERFACE
256-BYTE DATA MEMORY
INTERNAL TIMER
CONTROL PROGRAM
8080 CONTROL PROCESSOR
CONTROL SCRATCH PAD
INTELLEC BUS INTERFACE

Figure 1. ICE-49 Module Block Diagram

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the MCS-48 device.

Software

The ICE-49 software driver is a RAM-based program which provides the user with an easy to use command language (see Table 1, Table 2, and Table 3) for defining breakpoints, initiating real-time emulation or single step operation, and interrogating and altering user system status recorded during emulation. The ICE-49 command language contains a broad range of modifiers to provide the user with maximum flexibility in defining the operation to be performed. The ICE-49 software driver is available on diskette and operates in 32K of Intellec RAM memory.

Command	Operation
Enable	Activates breakpoint and display registers for use with go and step commands.
Go	Initiates real-time emulation and allows user to specify breakpoints and data retrieval.
Step	Initiates emulation in single instruction increments. Each step is followed by register dump. User may optionally tailor other diagnostic activity to his needs.
Interrupt	Emulates user system interrupt.

Table 1. ICE-49 Emulation Commands

Command	Operation
Display	Prints contents of memory, MCS-48 device registers, I/O ports, flags, pins, real-time trace data, symbol table, or other diagnostic data on list device.
Change	Alters contents of memory, register, output port, or flag. Sets or alters breakpoints and display registers.
Map	Defines memory status.
Base	Establishes mode of display for output data.
Suffix	Establishes mode of display input data.

Table 2. ICE-49 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Move	Moves block of memory data to another area of memory.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, octal, decimal, and hex.
Remove	Deletes symbols from symbol table.
Reset	Reinitializes ICE-49 hardware.

Table 3. ICE-49 Utility Commands

SPECIFICATIONS

ICE-49 Operating Environment

Required Hardware

Intellec microcomputer development system

System console

Intellec diskette operating system

ICE-49 Module

Required Software

System monitor

ISIS-II

Equipment Supplied

Printed circuit boards (control board, emulator board)

Interface cables and buffer module

ICE-49 software, diskette-based version (single density or double density)

8048 with internal monitor program

System Clock

Crystal controlled 6.0 MHz internal, 3.0 MHz internal or user supplied TTL external: software selectable.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 8.00 lb. (3.64 kg)

Electrical Characteristics

DC Power Requirements

V_{CC} = +5V ±5%
I_{CC} = 10A max; 7.0A typ
V_{DD} = +12V ±5%
I_{DD} = 79 mA max; 45 mA typ
V_{BB} = −10V ±5%
I_{BB} = 20 mA max

Input Impedance — @ICE-49 user socket pins:

V_{IL} = 0.8V (max), I_{IL} = −1.6 mA,
V_{IH} = 2.0V (min), I_{IH} = 40 μA

For Bus:
V_{IL} = 0.8V (max), I_{IL} = −250 μA
V_{IH} = 2.0V (min), I_{IH} = 20 μA

Output Impedance — @ICE-49 user socket pins:

P1, P2:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = V_{CC} (10K pullup)

For Bus:
V_{OL} = 0.5V (max), I_{OL} = 25 mA
V_{OH} = 3.65V (min), I_{OH} = −1 mA

Others:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = 2.4V (max), I_{OH} = −400 μA

Environmental Characteristics

Operating Temperature — 0°C to 40°C (Room Temperature)

Operating Humidity — Up to 95% relative humidity without condensation

Reference Manuals

9800632 — ICE-49 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-49-ICE	8049, 8048, 8039, 8748, 8035, 8021 CPU in-circuit emulator. Cable assembly and interactive diskette software included

ICE-80™
8080 IN-CIRCUIT EMULATOR

Connects Intellec system to user configured system via an external cable and 40-pin plug, replacing the user system 8080

Allows real-time (2 MHz) emulation of user system 8080

Shares Intellec RAM, ROM, and PROM memory and Intellec I/O facilities with user system

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates need for extraneous debugging tools residing in user system

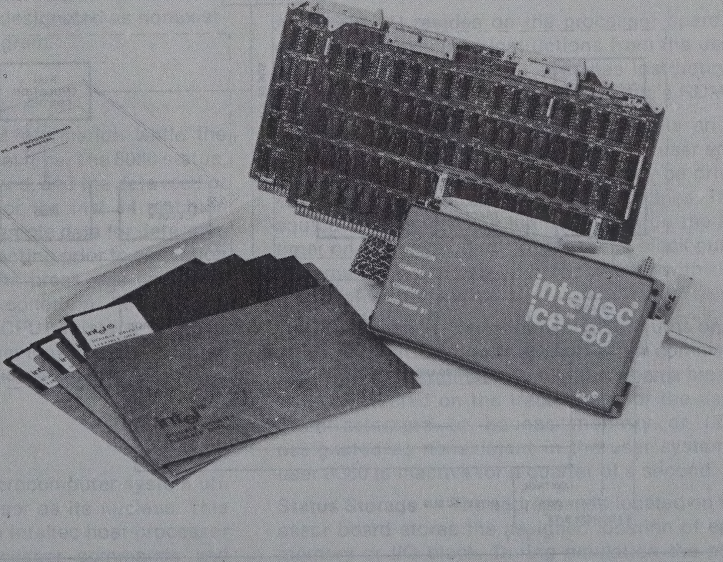
Provides address, data, and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin, and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec ICE-80 8080 In-Circuit Emulator is an Intellec resident module designed to interface with any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer may emulate the system's 8080 in real time, single step the system's program, and substitute Intellec memory and I/O for user system equivalents. Powerful Intellec debug functions are extended into the user system. For the first time the designer may examine and modify his system with symbolic references instead of absolute values.



FUNCTIONAL DESCRIPTION

Integrated Hardware/Software Development

Use of the ICE-80 module enables the system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, to become a convenient two-way debug tool when begun early in the design cycle. The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. With the ICE-80 mapping capabilities, system resources may be accessed for missing prototype hardware. Hardware designs may be tested using system software to drive the final product. A functional block diagram of the ICE-80 module is shown in Figure 1.

Symbolic Debugging Capability

ICE-80 provides for user-defined symbolic references to program memory addresses and data. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is thus relieved from looking up addresses of variables or program subroutines.

Symbol Table — The user symbol table generated along with the object file during a PL/M-80 compilation or a MAC80 or resident assembly, is loaded to memory along with the user program to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables found useful during system debugging. By referring to symbolic memory addresses, the user may be assured of examining, changing, or breaking at the intended location.

Symbolic Reference — ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: TIMER, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; ADDRESS, the address of the last instruction emulated; INTERRUPTENABLED, the user 8080 interrupt mechanism status; and UPPERLIMIT, the highest RAM address occupied by user memory.

Debug Capability Inside User System

ICE-80 provides for user debugging of full prototype or production systems without introducing extraneous hardware or software test tools. ICE-80 connects to the user system through the socket provided for the user 8080 in the user system (See Figure 2). Intellec memory is used for the execution of the ICE-80 software, while I/O provides the user with the ability to communicate with ICE-80 and receive information on the generation of the user system. A sample ICE-80 debug session is shown in Figure 3.

I/O Mapping and Memory

Memory and I/O for the user system may be resident in the user system or "borrowed" from the Intellec system through ICE-80's mapping capability.

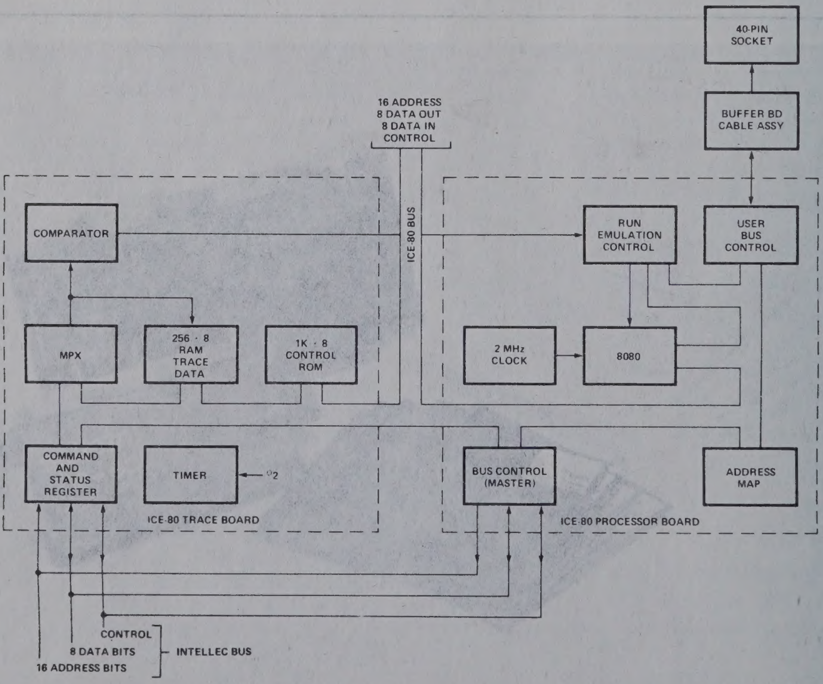

40-PIN SOCKET
BUFFER BD CABLE ASSY
16 ADDRESS
8 DATA OUT
8 DATA IN
CONTROL
ICE-80 BUS
COMPARATOR
RUN EMULATION CONTROL
USER BUS CONTROL
MPX
256 · 8 RAM TRACE DATA
1K · 8 CONTROL ROM
2 MHz CLOCK
8080
COMMAND AND STATUS REGISTER
TIMER
ϕ_2
BUS CONTROL (MASTER)
ADDRESS MAP
ICE-80 TRACE BOARD
ICE-80 PROCESSOR BOARD
CONTROL
8 DATA BITS
16 ADDRESS BITS
INTELLEC BUS

Figure 1. Functional Block Diagram of ICE-80 Module

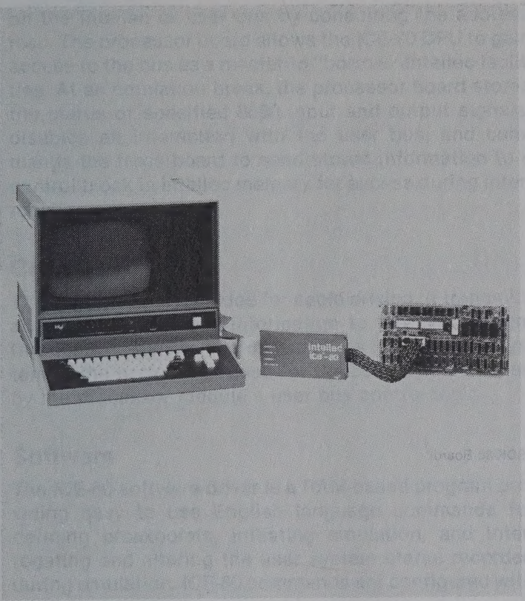


Figure 2. ICE-80 Module Installed in User System

Memory Blocking — ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O may be defined independently. The user may assign system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, memory or I/O may be accessed in place of user system devices during prototype or production checkout.

Error Messages — The user may also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexisting is accessed by the user program.

Real-Time Trace

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition. For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

Hardware

The heart of the ICE-80 is a microcomputer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE-80 trace board. ICE-80 and the system also communicate through a control block resident in the Intellec main memory, which contains detailed configuration and status information transmitted at an emulation break. ICE-80 hardware consists of two PC boards — the processor and trace boards residing in the Intellec chassis — and a 6-foot cable interfacing to the user system. The trace and processor boards communicate with the system on the bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

Trace Board

The trace board talks to the system as a peripheral device. It receives commands to ICE-80 and returns ICE-80 responses. While ICE-80 is executing the user program, the trace board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

Breakpoint — The trace board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparitor is constantly monitoring address and status lines for a match to terminate an emulation. A user probe is also available for attachment to any user signal. When this signal goes true a break condition is recognized.

Interrogation — The trace board signals the processor board when a command to ICE-80 or break condition has been detected. The ICE-80 CPU then sends data stored on the trace board to the control block in memory. Snap data, along with information on 8080 registers and pin status and the reason for the emulation break, are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

Processor Board

An 8080 CPU resides on the processor board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the trace module's ROM.

Timing — The processor board contains an internal clock generator to provide clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the trace board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

On/Off Control — The processor board turns on an emulation when ICE-80 has received a run command from the system. It terminates emulation when a break condition is detected on the trace board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

Status Storage — The address map located on the processor board stores the assigned location of each user memory or I/O block. During emulation the processor board determines whether to send/receive information

```
ISIS 8080 MACROASSEMBLER, V1.0                  PAGE 1

              ;USER PROGRAM TO OUTPUT A SERIES OF
              ;CHARACTERS TO SDK-80 CONSOLE DEVICE
              ;
1320                   ORG    1320H
01E3          C0       EQU    1E3H    ;SDK-80 CONSOLE OUT DRIVER
              ;
1320 0601     START:   MVI    B,1     ;SET UP B VALUE
1322 3A3613            LDA    DAT1    ;LOAD A WITH DAT1 VALUE
135 4F        LOOP:    MDV    C,A
1326 CDE301            CALL   C0      ;SEND C VALUE TO CONSOLE
1329 79                MOV    A,C     ;RESTORE A
132A 93                SBB    B       ;SUBTRACT B FROM A
132B 323713            STA    RSLT    ;STORE RESULT IN RSLT
132E FE40              CPI    40H     ;LAST VALUE TO PRINT
1330 C22513            JNZ    LOOP    ;LOOP AGAIN IF A>40H
1333 C32013            JMP    START   ;ELSE RESTART WHOLE PROCEDURE
              ;
1336 5A       DAT1:    DB     5AH
1337          RSLT:    DS     1
0000                   END

ISIS, V1.0    INITIAL ICE-80 SESSION
-ICE80        (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
ISIS ICE-80, V1.0
①  **XFORM MEMORY 0 TO 1 U
    *XFORM IO 0FH U
②  *LOAD PROG. HEX
    ERR = 067
    STAT = 11H TYPE = 06H CMND = 07H ADDR = 1320H GOOD = 06H BAD = 04H
    *CHANGE MEMORY 1321H = FFH
    ERR = 067
    STAT = 11H TYPE = 06H CMND = 07H ADDR = 1321H GOOD = FFH BAD = FDH
    *LOAD PROG. HEX
③  *GO FROM START UNTIL RSLT WRITTEN
    EMULATION BEGUN
④  ERR = 067
    STAT = 11H TYPE = 07H CMND = 02H
⑤  *DISPLAY CYCLES 5

    STAT = A2H ADDR = 1326H DATA = CDH
    STAT = 82H ADDR = 1327H DATA = E3H
    STAT = 82H ADDR = 1328H DATA = 01H
    STAT = 04H ADDR = FFFFH DATA = 13H
    STAT = 04H ADDR = FFFEH DATA = 29H
⑥  *CHANGE DOUBLE REGISTER SP = 13FFH
    *BASE HEX
    *EQUATE STOP = 1333H
⑦  *GO FROM START UNTIL STOP EXECUTED THEN DUMP
    EMULATION BEGUN
    B = 01H C = 41H D = 00H E = 00H H = 00H L = 00H F = 56H A = 40H P = 1320H * = 1333H S = 13FFH
    EMULATION TERMINATED AT 1333H
⑧  *EXIT
    *FFFF
```

Notes

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H–1FFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).
2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H–13FFH in the prototype system. The problem is fixed and a subsequent load succeeds.
3. A real-time emulation is begun. The program is executed from 'START' (1320H) and continues until 'RSLT' is written [in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT'].
4. An error condition results: TYPE 07, CMND 02 indicate the program accessed is a guarded area.
5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.
6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.
7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a dump of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.
8. Exit returns control to the MDS monitor.

Figure 3. Sample ICE-80 Debug Session

on the Intellec or user bus by consulting the address map. The processor board allows the ICE-80 CPU to gain access to the bus as a master to "borrow" Intellec facilities. At an emulation break, the processor board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the trace board to send stored information to a control block in Intellec memory for access during interrogation mode.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector that plugs into the user system in the socket designed for the 8080 when enabled by the processor module's user bus control logic.

Software

The ICE-80 software driver is a RAM-based program providing easy to use English language commands for defining breakpoints, initiating emulation, and interrogating and altering the user system status recorded during emulation. ICE-80 commands are configured with a broad range of modifiers to provide the user with maximum flexibility in describing the operation to be performed. Listings of emulation commands, interrogation commands, and utility commands are provided in Table 1, Table 2, and Table 3, respectively.

Command	Operation
Go	Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.
Step	Initiates emulation in single or multiple instruction increments. User may specify register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.
Range	Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.
Continue	Resumes real-time emulation.
Call	Emulates user system interrupt.

Table 1. ICE-80 Emulation Commands

Command	Operation
Base	Establishes mode of display for output data.
Display	Prints contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. May also be used for base-to-base conversion, or for addition or subtraction in any base.
Change	Alters contents of memory, register, output port, or 8080 flag.
XFORM	Defines memory and I/O status.
Search	Looks through memory range for specified value.

Table 2. ICE-80 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Equate	Enters symbol name and value to user symbol table.
Fill	Fills memory range with specified value.
Move	Moves block of memory data to another area of memory.
Timeout	Enables/disables user CPU ¼ second wait state timeout.
List	Defines list device (diskette-based version only).
Exit	Returns program control to monitor.

Table 3. ICE-80 Utility Commands

SPECIFICATIONS

Paper Tape-Based Operating Environment

Required Hardware
Intellec system
System console
Reader device
Punch device
ICE-80 module

Required Software
System monitor

Diskette-Based Operating Environment

Required Hardware
Intellec system
32K bytes RAM memory
System console
Intellec diskette operating system
ICE-80 module

Required Software
System monitor
ISIS-II

System Clock

Crystal controlled 2.185 MHz ± 0.01%. May be replaced by user clock through jumper selection.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 8.00 lb (3.64 kg)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V, \pm 5\%$
$I_{CC} = 9.81A$ max; 6.90A typ
$V_{DD} = +12V, \pm 5\%$
$I_{DD} = 79$ mA max; 45 mA typ
$V_{BB} = -9V, \pm 5\%$
$I_{BB} = 1$ mA max; $1\mu A$ typ

Environmental Characteristics

Operating Temperature — 0°C to 40°C

Operating Humidity — Up to 95% relative humidity without condensation

Equipment Supplied

Printed circuit modules (2)
Interface cables and buffer board
ICE-80 software driver, paper tape version
(ICE-80 software driver, diskette-based version is supplied with diskette operating systems)
Operator's Manual

ORDERING INFORMATION

Part Number	Description
MDS-80-ICE	8080 CPU in-circuit emulator, cable assembly and interactive software included

ICE-85™
MCS-85™ IN-CIRCUIT EMULATOR

Connects the Intellec® System Resources to the user-configured system via a 40-pin adaptor plug

Executes user system software in real-time

Allows user-configured system to share Intellec® memory and I/O facilities

Provides 1023 states of 8085 trace data plus 18 additional logic signals via an External Trace Module

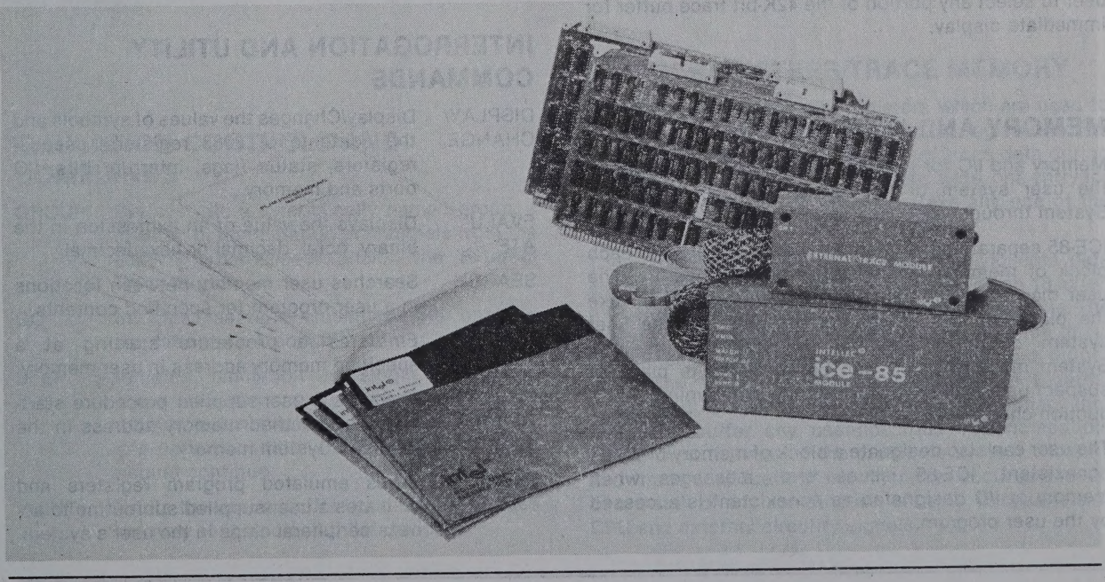
Offers full symbolic debugging capability for both assembly language and Intel's high-level compiler languages PL/M-80 and FORTRAN-80

Displays trace data from the user's 8085 in assembler mnemonics and allows personality groupings of data sampled by the external 18-channel trace module

Extends ICE capabilities to the rest of the prototype system peripheral circuitry by allowing the user to execute his own peripheral chip analysis routines

Provides ability to examine and alter MCS-85™ registers, memory, flag values, interrupt bits and I/O ports

The ICE-85 module resides in the Intellec® Microcomputer Development System and interfaces to the user system's 8085. In addition, an external trace module provides access to user system peripheral circuitry via a user-configured DIP clip for peripheral ICs or may be attached to as many as 18 separate prototype signal nodes via individual probe clips. Using the ICE-85 module, the designer can execute prototype software in real-time or single-step mode and can substitute Intellec® system memory and I/O for user system equivalent. ICE capability can be extended to the rest of the user system peripheral circuitry by allowing the user to create and execute a library of user-defined peripheral chip analyzer routines. All user access to the prototype system software may be done symbolically by assigning names to program locations and data, I/O ports and groups of external trace signals. For the first time, in-circuit emulation extends beyond the user's prototype CPU to the entire user's system, allowing In-System Emulation.



SYMBOLIC DEBUGGING CAPABILITY

ICE-85 allows the user to make symbolic references to I/O ports, memory addresses and data in his program. Symbols and PL/M-80 statement number may be substituted for numeric values in any of the ICE-85 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M-80 or FORTRAN-80 compilation or by the ISIS-II 8080/8085 Macro Assembler is loaded into the Intellec® System memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location.

ICE-85 provides symbolic definition of all 8085 registers, interrupt bits and flags. The following symbolic references are also provided for user convenience: TIMER, the low-order 16 bits of a register containing the number of 2 MHz clock pulses elapsed during emulation; HTIMER, the high-order 16 bits of the timer counter; PPC, the address of the last instruction emulated; BUFFERSIZE, the number of frames of valid trace data (between 0 and 1022).

PERSONALITY GROUPED DISPLAYS

Trace data in the 1023 by 42-channel real-time trace memory buffer is displayed in easy to read format. The user has the option to specify trace data displays in actual 8085 assembler instruction mnemonics. The data collected from the External Trace Module can be grouped and symbolically named according to user specifications and displayed in the appropriate number base designation. Simple ICE-85 commands allow the user to select any portion of the 42K-bit trace buffer for immediate display.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec® System through ICE-85's mapping capability.

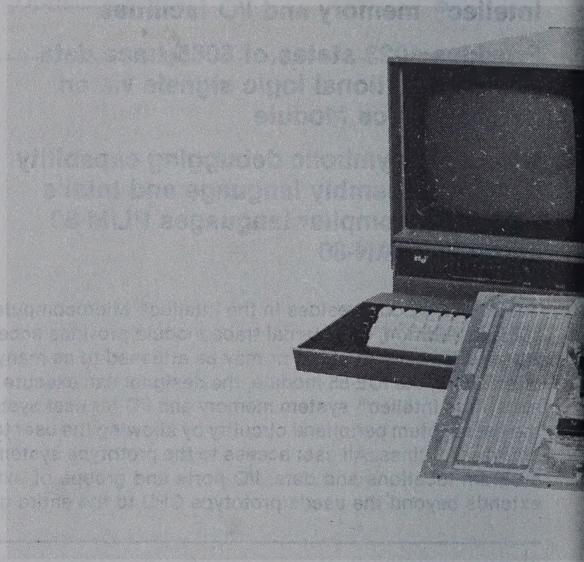
ICE-85 separates user memory into 32 2K blocks. Each block of memory can be defined independently. The user may assign Intellec® System equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, Intellec® System memory or I/O can be accessed in place of suspect user system devices during prototyping or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-85 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8085 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-85 mapping capabilities, Intellec® System equivalents can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.



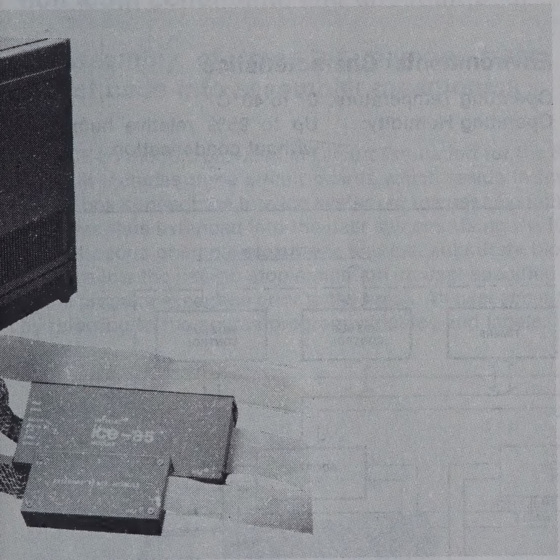
INTERROGATION AND UTILITY COMMANDS

DISPLAY/ CHANGE	Display/Changes the values of symbols and the contents of 8085 registers, pseudo-registers, status flags, interrupt bits, I/O ports and memory.
EVALUATE	Displays the value of an expression in the binary, octal, decimal or hexadecimal.
SEARCH	Searches user memory between locations in a user program for specified contents.
CALL	*Emulates* a procedure starting at a specified memory address in user memory.
ICALL	*Executes* a user-supplied procedure starting at a specified memory address in the Intellec® System memory.
EXECUTE	Saves emulated program registers and emulates a user-supplied subroutine to access peripheral chips in the user's system.

REAL TIME TRACE

ICE-85 captures valuable trace information from the emulating CPU and the External Trace Module while the user is executing programs in real time. The 8085 status, the user memory or port addressed, the data read or written, the serial data lines and data from 18 external signals, is stored for the last 1023 machine states executed (511 machine cycles). This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user-initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multi-step sequences tailored to system debug needs.



EMULATION CONTROLS AND COMMANDS

GROUP	Defines into a symbolically named group, a channel or combination of channels from the 8085 Microprocessor and/or the External Trace Module.
GO	Initiates real-time emulation and controls emulation break conditions.
STEP	Initiates emulation in single instruction steps. User may specify the type and amount of information displayed following each step, and define conditions under which stepping should continue.
PRINT	Prints the user-specified portion of the trace memory to the selected list device.

EXTERNAL TRACE MODULE

TTL level signals from 18 points in the user system may be synchronously sampled by the External Trace Module and collected in ICE-85's trace buffer. The signals can be collected from a single peripheral chip via the supplied 40-pin DIP clip or may be placed by the user on up to 18 separate signal nodes using the supplied 18 individual probe clips. These signals are included in the 42-channel breakpoint comparisons and clock qualifiers. Also, data from these 18 channels may be displayed in each to read, user-defined groupings.

SYNCHRONOUS OPERATION WITH OTHER DESIGN AIDS

ICE-85 can be synchronized with other Intellec® design aids by means of two external synchronization lines. These lines are used to enable and disable ICE-85 trace data collection and to cause break conditions based on an external signal which may not be included in the ICE-85 breakpoint registers. In addition, ICE-85 can generate signals on these lines which may be used to control other design aids.

BREAK REGISTERS/TRACE MEMORY

ICE-85 has two breakpoint registers which are used to break emulation, and two trace qualifier registers which are used to control the collection of trace data during emulation. Each register is 42 entries wide, one entry for each channel and each entry can take any one of the three values 0, 1 or "don't care."

The trace buffer, also 42 entries wide, collects data sampled from 24 8085 processor channels and 18 external channels sampled by the External Trace Module. The signals collected from the 8085 include address lines, data lines, status lines and series input and output lines. The 18 channels extending from the External Trace Module synchronously sample and collect into the trace buffer any user-specified TTL compatible signal from the rest of the prototype system. "Break" and "trace qualification" may therefore occur as a result of a match of any combination of up to 42 channels of CPU and external circuitry signals.

SPECIFICATIONS

ICE-85 Operating Environment

Required Hardware:
  Intellec® Microcomputer Development System
  System Console
  Intellec® Diskette Operating System
  ICE-85 Module
Required Software:
  System Monitor
  ISIS-II
  ICE-85 Software

Equipment Supplied

18-Channel External Trace Module
Printed Circuit Boards (2)
Interface Cable and Emulation Buffer Module
Operator's Manual
ICE-85 Software, Diskette-Based Version

Emulation Clock

User's system clock or ICE-85 adaptor socket (6.144 MHz Crystal)

Physical Characteristics

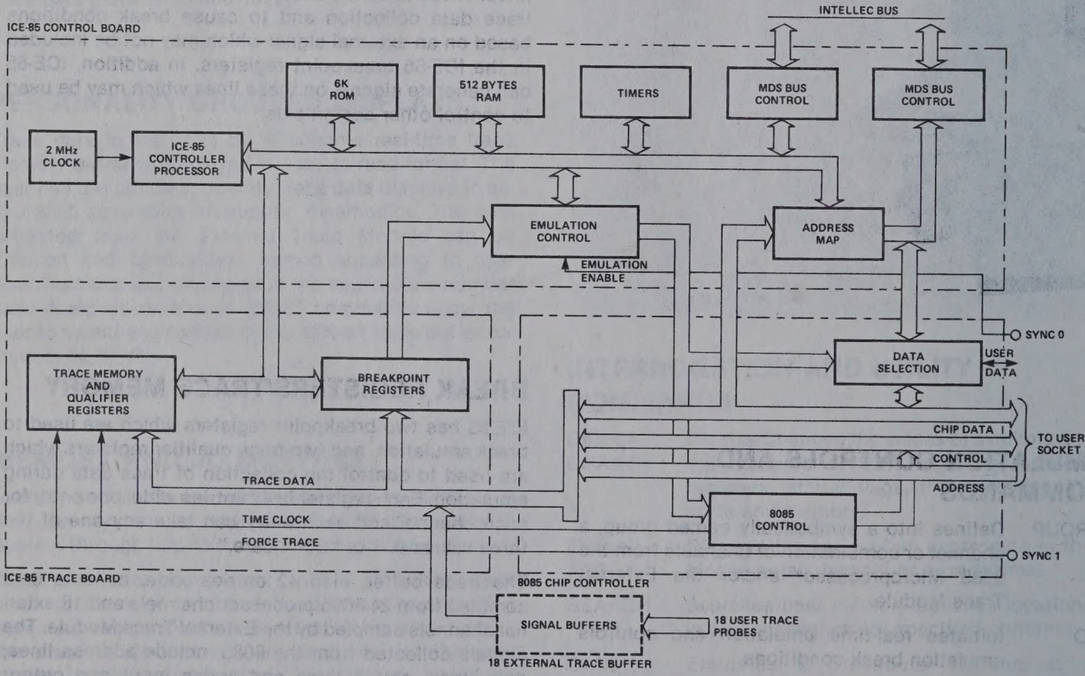
Printed Circuit Boards:
  Width: 12.00 in. (30.48 cm)
  Height: 6.75 in. (17.15 cm)
  Depth: 0.50 in. (1.27 cm)
  Packaged Weight: 6.00 lb (2.73 kg)

Electrical Characteristics

DC Power:
  $V_{CC} = +5V \pm 5\%$
  $I_{CC} = 12A$ maximum; 10A typical
  $V_{DD} = +12V \pm 5\%$
  $I_{DD} = 80$ mA maximum; 60 mA typical
  $V_{BB} = -10V \pm 5\%$
  $I_{BB} = 1$ mA maximum; 10 μA typical

Environmental Characteristics

Operating Temperature: 0° to 40°C
Operating Humidity: Up to 95% relative humidity without condensation.


INTELLEC BUS
ICE-85 CONTROL BOARD
6K ROM
512 BYTES RAM
TIMERS
MDS BUS CONTROL
MDS BUS CONTROL
2 MHz CLOCK
ICE-85 CONTROLLER PROCESSOR
EMULATION CONTROL
ADDRESS MAP
EMULATION ENABLE
SYNC 0
TRACE MEMORY AND QUALIFIER REGISTERS
BREAKPOINT REGISTERS
DATA SELECTION
USER DATA
CHIP DATA
CONTROL
ADDRESS
TO USER'S SOCKET
TRACE DATA
TIME CLOCK
FORCE TRACE
8085 CONTROL
SYNC 1
ICE-85 TRACE BOARD
8085 CHIP CONTROLLER
SIGNAL BUFFERS
18 USER TRACE PROBES
18 EXTERNAL TRACE BUFFER

ICE-85 BLOCK DIAGRAM

Ordering Information

Part Number	Description
MDS-85-ICE	8085 CPU In-Circuit Emulator and 18-Channel External Trace Module

ICE-86™
8086 IN-CIRCUIT EMULATOR

Hardware in-circuit emulation

Full symbolic debugging

Breakpoints to halt emulation on a wide variety of conditions

Comprehensive trace of program execution, both conditional and unconditional

Disassembly of trace or memory from object code into assembler mnemonics

2K bytes of high speed ICE-86 mapped memory

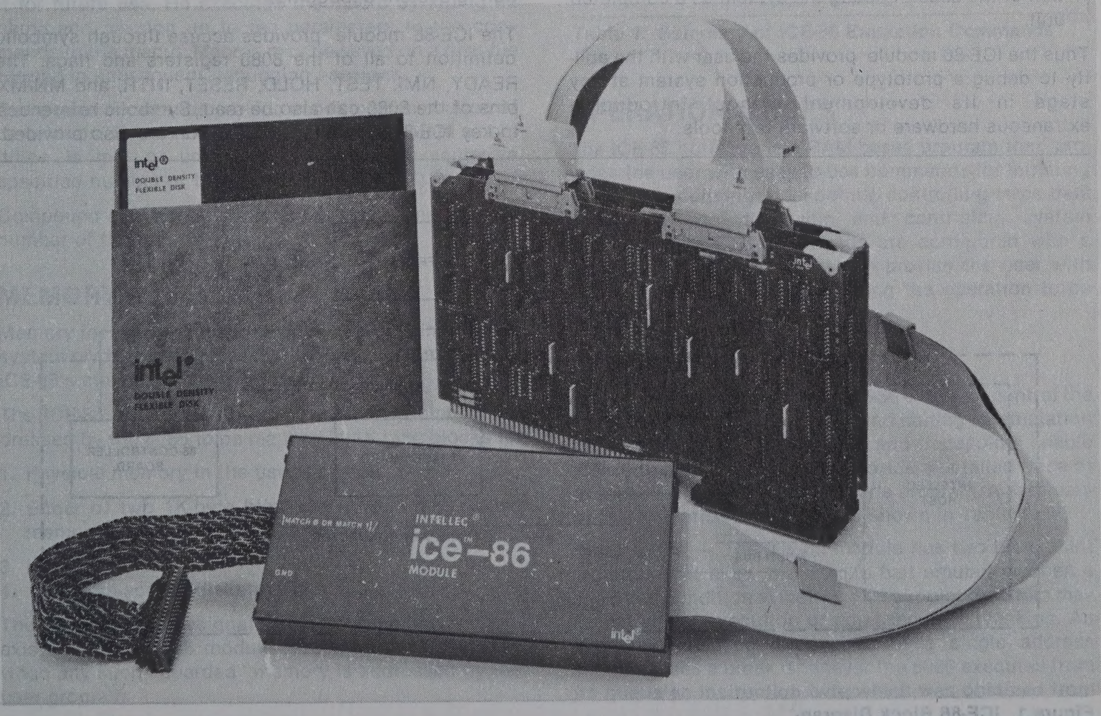
Software debugging with or without user system

Handles full 1 megabyte addressability of 8086

Compound commands

Command macros

The ICE-86 module provides In-Circuit Emulation for the 8086 microprocessor and the iSBC 86/12 Single Board Computer. It includes three circuit boards which reside in Intellec® Microcomputer Development Systems. A cable and buffer box connect the Intellec system to the user system by replacing the user's 8086. Powerful Intellec debug functions are thus extended into the user system. Using the ICE-86 module, the designer can execute prototype software in continuous or single-step mode and can substitute blocks of Intellec system memory for user equivalents. Breakpoints allow the user to stop emulation on user-specified conditions, and the trace capability gives a detailed history of the program execution prior to the break. All user access to the prototype system software may be done symbolically by referring to the source program variables and labels.


intel® DOUBLE DENSITY FLEXIBLE DISK
intel® DOUBLE DENSITY FLEXIBLE DISK
MATCH 0 OR MATCH 1
GND
INTELLEC®
ice™-86
MODULE
intel

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The ICE-86 emulator allows hardware and software development to proceed interactively. This is more effective than the traditional method of independent hardware and software development followed by system integration. With the ICE-86 module, prototype hardware can be added to the system as it is designed. Software and hardware testing occurs while the product is being developed.

Conceptually, the ICE-86 emulator assists three stages of development:

1. It can be operated without being connected to the user's system, so ICE-86 debugging capabilities can be used to facilitate program development before any of the user's hardware is available.
2. Integration of software and hardware can begin when any functional element of the user system hardware is connected to the 8086 socket. Through ICE-86 mapping capabilities, Intellec memory, ICE memory, or diskette memory can be substituted for missing prototype memory. Time-critical program modules are debugged before hardware implementation by using the 2K-bytes of high-speed ICE-resident memory. As each section of the user's hardware is completed, it is added to the prototype. Thus each section of the hardware and software is "system" tested as it becomes available.
3. When the user's prototype is complete, it is tested with the final version of the user system software. The ICE-86 module is then used for real time emulation of the 8086 to debug the system as a completed unit.

Thus the ICE-86 module provides the user with the ability to debug a prototype or production system at any stage in its development without introducing extraneous hardware or software test tools.

SYMBOLIC DEBUGGING

Symbols and PL/M statement numbers may be substituted for numeric values in any of the ICE-86 commands. This allows the user to make symbolic references to I/O ports, memory addresses, and data in the user program. Thus the user need not remember the addresses of variables or program subroutines.

Symbols can be used to reference variables, procedures, program labels, and source statements. A variable can be displayed or changed by referring to it by name rather than by its absolute location in memory. Using symbols for statement labels, program labels, and procedure names simplifies both tracing and breakpoint setting. Disassembly of a section of code from either trace or program memory into its assembly mnemonics is readily accomplished.

Furthermore, each symbol may have associated with it one of the data types BYTE, WORD, INTEGER, SINTEGER (for short, 8-bit integer) or POINTER. Thus the user need not remember the type of a source program variable when examining or modifying it. For example, the command "!VAR" displays the value in memory of variable VAR in a format appropriate to its type, while the command "!VAR = !VAR + 1" increments the value of the variable.

The user symbol table generated along with the object file during a PL/M-86 compilation or an ASM-86 assembly is loaded into memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging.

The ICE-86 module provides access through symbolic definition to all of the 8086 registers and flags. The READY, NMI, $\overline{\text{TEST}}$, HOLD, RESET, INTR, and MN/$\overline{\text{MX}}$ pins of the 8086 can also be read. Symbolic references to key ICE-86 emulation information are also provided.

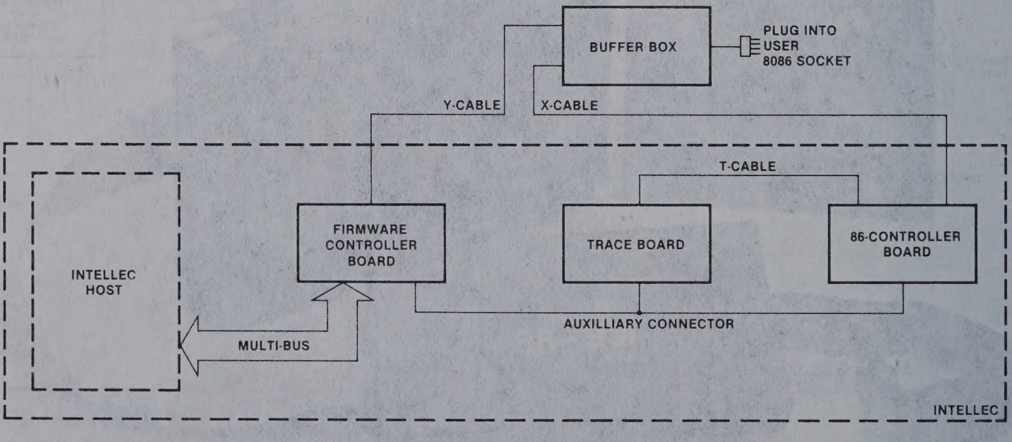
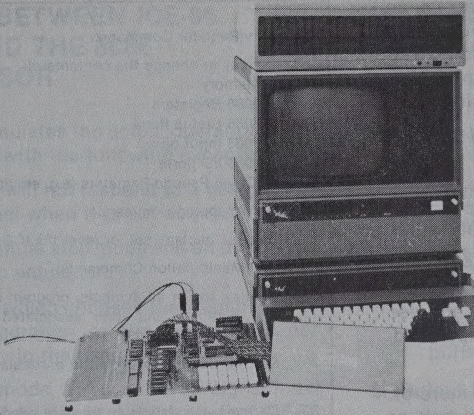


Figure 1. ICE-86 Block Diagran.



A typical ICE-86 development configuration. It is based on a Model 230 Development System, which also includes a Double Density Diskette Operating System and a Model 201 Expansion Chassis (which holds the ICE-86 emulator). The ICE-86 module is shown connected to a user prototype system, in this case an SDK-86.

MACROS AND COMPOUND COMMANDS

The ICE-86 module provides a programmable diagnostic facility which allows the user to tailor its operation using macro commands and compound commands.

A macro is a set of ICE-86 commands which is given a single name. Thus, a sequence of commands which is executed frequently may be invoked simply by typing in a single command. The user first defines the macro by entering the entire sequence of commands which he wants to execute. He then names the macro and stores it for future use. He executes the macro by typing its name and passing up to ten parameters to the commands in the macro. Macros may be saved on a disk file for use in subsequent debugging sessions.

Compound commands provide conditional execution of commands(IF), and execution of commands until a condition is met or until they have been executed a specified number of times (COUNT, REPEAT).

Compound commands and macros may be nested any number of times.

MEMORY MAPPING

Memory for the user system can be resident in the user system or "borrowed" from the Intellec System through ICE-86's mapping capability.

The ICE-86 emulator allows the memory which is addressed by the 8086 to be mapped in 1K-byte blocks to:

1. Physical memory in the user's system,
2. Either of two 1K-byte blocks of ICE-86 high speed memory,
3. Intellec memory,
4. A random-access diskette file.

The user can also designate a block of memory as nonexistent. The ICE-86 module issues an error message when any such "guarded" memory is addressed by the user program.

Command	Description
GO	Initializes emulation and allows the user to specify the starting point and breakpoints. Example: GO FROM .START TILL .DELAY EXECUTED where START and DELAY are statement labels.
STEP	Allows the user to single-step through the program.

Table 1. Summary of ICE-86 Emulation Commands

OPERATION MODES

The ICE-86 software is a RAM-based program that provides the user with easy-to-use commands for initiating emulation, defining breakpoints, controlling trace data collection, and displaying and controlling system parameters. ICE-86 commands are configured with a broad range of modifiers which provide the user with maximum flexibility in describing the operation to be performed.

Emulation

Emulation commands to the ICE-86 emulator control the process of setting up, running and halting an emulation of the user's 8086. Breakpoints and tracepoints enable ICE-86 to halt emulation and provide a detailed trace of execution in any part of the user's program. A summary of the emulation commands is shown in Table 1.

Breakpoints — The ICE-86 module has two breakpoint registers that allow the user to halt emulation when a specified condition is met. The breakpoint registers may be set up for execution or non-execution breaking. An execution breakpoint consists of a single address which causes a break whenever the 8086 executes from its queue an instruction byte which was obtained from the address. A non-execution breakpoint causes an emulation break when a specified condition other than an instruction execution occurs. A non-execution breakpoint condition, using one or both breakpoint registers, may be specified by any one of or a combination of:

1. *A set of address values.* Break on a set of address values has three valuable features:
   a. Break on a single address.
   b. The ability to set any number of breakpoints within a limited range (1024 bytes maximum) of memory.
   c. The ability to break in an unlimited range. Execution is halted on any memory access to an address greater than (or less than) any 20-bit breakpoint address.
2. *A particular status of the 8086 bus* (one or more of: memory or I/O read or write, instruction fetch, halt, or interrupt acknowledge).
3. *A set of data values* (features comparable to break on a set of address values, explained in point one).
4. *A segment register* (break occurs when the register is used in an effective address calculation).

An external breakpoint match output for user access is provided on the buffer box. This allows synchronization of other test equipment when a break occurs.

Tracepoints — The ICE-86 module has two tracepoint registers which establish match conditions to conditionally start and stop trace collection. The trace information is gathered at least twice per bus cycle, first when the address signals are valid and second when the data signals are valid. If the 8086 execution queue is otherwise active, additional frames of trace are collected.

Each trace frame contains the 20 address/data lines and detailed information on the status of the 8086. The trace memory can store 1,023 frames, or an average of about 300 bus cycles, providing ample data for determining how the 8086 was reacting prior to emulation break. The trace memory contains the last 1,023 frames of trace data collected, even if this spans several separate emulations. The user has the option of displaying each frame of the trace data or displaying by instruction in actual ASM-86 Assembler mnemonics. Unless the user chooses to disable trace, the trace information is always available after an emulation.

Interrogation and Utility

Interrogation and utility commands give the user convenient access to detailed information about the user program and the state of the 8086 that is useful in debugging hardware and software. Changes can be made in both memory and the 8086 registers, flags, input pins, and I/O ports. Commands are also provided for various utility operations such as loading and saving program files, defining symbols and macros, displaying trace data, setting up the memory map, and returning control to ISIS-II. A summary of the basic interrogation and utility commands is shown in Table 2.

Memory/Register Commands

Display or change the contents of:
- Memory
- 8086 Registers
- 8086 Status flags
- 8086 Input pins
- 8086 I/O ports
- ICE-86 Pseudo-Registers (e.g. emulation timer)

Memory Mapping Commands

Display, declare, set, or reset the ICE-86 memory mapping.

Symbol Manipulation Commands

Display any or all symbols, program modules, and program line numbers and their associated values (locations in memory).

Set the domain (choose the particular program module) for the line numbers.

Define new symbols as they are needed in debugging.

Remove any or all symbols, modules, and program statements.

Change the value of any symbol.

TYPE

Assign or change the type of any symbol in the symbol table.

ASM

Disassemble user program memory into ASM-86 Assembler mnemonics.

PRINT

Display the specified portion of the trace memory.

LOAD

Fetch user symbol table and object code from the input file.

SAVE

Send user symbol table and object code to the output file.

LIST

Send a copy of all output (including prompts, input line echos, and error messages) to the chosen output device (e.g. disk, printer) as well as the console.

EVALUATE

Display the value of an expression in binary, octal, decimal, hexadecimal, and ASCII.

SUFFIX/BASE

Establish the default base for numeric values in input text/output display (binary, octal, decimal, or hexadecimal).

CLOCK

Select the internal (ICE-86 provided, for stand-alone mode only) or an external (user-provided) system clock.

RWTIMEOUT

Allows the user to time out READ/WRITE command signals based on the time taken by the 8086 to access Intellec memory or diskette memory.

ENABLE/DISABLE RDY

Enable or disable logical AND of ICE-86 Ready with the user Ready signal for accessing Intellec memory, ICE memory, or diskette memory.

Table 2. Summary of Basic ICE-86 Interrogation and Utility Commands

DIFFERENCES BETWEEN ICE-86 EMULATION AND THE 8086 MICROPROCESSOR

The ICE-86 module emulates the actual operation of the 8086 microprocessor with the following exceptions:

- The ICE-86 module will not respond to a user system NMI or RESET signal when it is out of emulation.
- Trap is ignored in single step mode and on the first instruction step of an emulation.
- The MIN/MAX line, which chooses the "minimum" or "maximum" configuration of the 8086, must not change dynamically in the user system.
- In the "minimum" mode, the user HOLD signal must remain active until HLDA is output by the ICE-86 emulator.
- The $\overline{\text{RQ}}/\overline{\text{GT}}$ lines in the "maximum" configuration are not supported.

The speed of run emulation by the ICE-86 module depends on where the user has mapped his memory. As the user prototype progresses to include memory, emulation becomes real time.

Memory Mapped To	Estimated Speed
User System	100% of real time*, up to 4 MHz clock
ICE	2 wait states per 8086-controlled bus cycle
Intellec	Approximately 0.02% of real time at 4 MHz clock
Diskette	**

*100% of real time is emulation at the user system clock rate with no wait states.

**The emulation speed from diskette is comparable to Intellec memory, but emulation must wait when a new page is accessed on the diskette.

DC CHARACTERISTICS OF ICE-86 USER CABLE

1. Output Low Voltages [V_{OL}(Max) = 0.4V]

	I_{OL} (Min)
AD0-AD15	8 mA (24 mA @ 0.5V)
A16/S3-A19/S7, $\overline{\text{BHE}}$/S7, $\overline{\text{RD}}$, $\overline{\text{LOCK}}$, QS0, QS1, $\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{S2}}$, $\overline{\text{WR}}$, M/$\overline{\text{IO}}$, DT/$\overline{\text{R}}$, $\overline{\text{DEN}}$, ALE, $\overline{\text{INTA}}$	8 mA (16 mA @ 0.5V)
HLDA	7 mA
$\overline{\text{MATCH0 OR MATCH1}}$ (on buffer box)	16 mA

2. Output High Voltages [V_{OH} (Min) = 2.4V]

	I_{OH}(Min)
AD0-AD15	−2 mA
A16/S3-A19/S7, $\overline{\text{BHE}}$/S7, $\overline{\text{RD}}$, $\overline{\text{LOCK}}$, QS0, QS1, $\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{S2}}$, $\overline{\text{WR}}$, M/$\overline{\text{IO}}$, DT/$\overline{\text{R}}$, $\overline{\text{DEN}}$, ALE, $\overline{\text{INTA}}$, HLDA	−1 mA
$\overline{\text{MATCH0 OR MATCH1}}$ (on buffer box)	−0.8 mA

3. Input Low Voltages [V_{IL}(Max) = 0.8V]

	I_{IL} (Max)
AD0-AD15	−0.2 mA
NMI, CLK	−0.4 mA
READY	−0.8 mA
INTR, HOLD, $\overline{\text{TEST}}$, RESET	−1.4 mA
MN/$\overline{\text{MX}}$ (0.1 μf to GND)	−3.3 mA

4. Input High Voltages [V_{IH}(Min) = 2.0V]

	I_{IH}(Max)
AD0-AD15	80 μA
NMI, CLK	20 μA
READY	40 μA
INTR, HOLD, $\overline{\text{TEST}}$, RESET	−0.4 mA
MN/$\overline{\text{MX}}$ (0.1 μF to GND)	−1.1 mA

5. $\overline{\text{RQ}}/\overline{\text{GT0}}$, $\overline{\text{RQ}}/\overline{\text{GT1}}$ are pulled up to +5V through a 5.6K ohm resistor. No current is taken from user circuit at V_{CC} pin.

SPECIFICATIONS

ICE-86 Operating Environment

Required Hardware

Intellec microcomputer development system with:

1. Three adjacent slots for the ICE-86 module (Series II requires Model 201 Expansion Chassis.)
2. 64K bytes of Intellec memory. If user prototype program memory is desired, additional memory above the basic 64K is required.

System console
Intellec diskette operating system
ICE-86 module

Required Software

System monitor
ISIS-II, version 3.4 or subsequent
ICE-86 software

Equipment Supplied

Printed circuit boards (3)
Interface cable and emulation buffer module
Operator's manual
ICE-86 software, diskette-based

Emulation Clock

User system clock up to 4 MHz or 2 MHz ICE-86 internal clock in stand-alone mode

Physical Characteristics

Printed Circuit Boards

Width: 12.00 in (30.48 cm)
Height: 6.75 in (17.15 cm)
Depth: 0.50 in (1.27 cm)
Packaged Weight: 9.00 lb (4.10 kg)

Electrical Characteristics

DC Power

$V_{CC} = +5V\ +5\%\ -1\%$
$I_{CC} = 15A$ maximum; 11A typical
$V_{DD} = +12V \pm 5\%$
$I_{DD} = 120$ mA maximum; 80 mA typical
$V_{BB} = -10V \pm 5\%$ or $-12V \pm 5\%$ (optional)
$I_{BB} = 15$ mA maximum; 12 mA typical

Environmental Characteristics

Operating Temperature: 0° to 40°C
Operating Humidity: Up to 95% relative humidity without condensation.

ORDERING INFORMATION

Part Number	Description
MDS-86-ICE	8086 CPU in-circuit emulator, cable assembly and interactive diskette software.

MULTI-ICE™ SOFTWARE MULTIPLE-IN-CIRCUIT-EMULATOR

Facilitates software and hardware debugging of multi-processor systems.

Allows two In-Circuit Emulators to operate simultaneously in a single Intellec Microcomputer Development System.

Provides enhanced software features: Symbolic Display of Addresses, Macro Commands, Compound Commands, Software Synchronization of Processes, and INCLUDE File Capability.

Supports In-Circuit Emulator combinations, 85/85 Emulators, 85/49 Emulators (ICE-49 Emulator supports the design using MCS-48 chip family) and 85/41A Emulators.

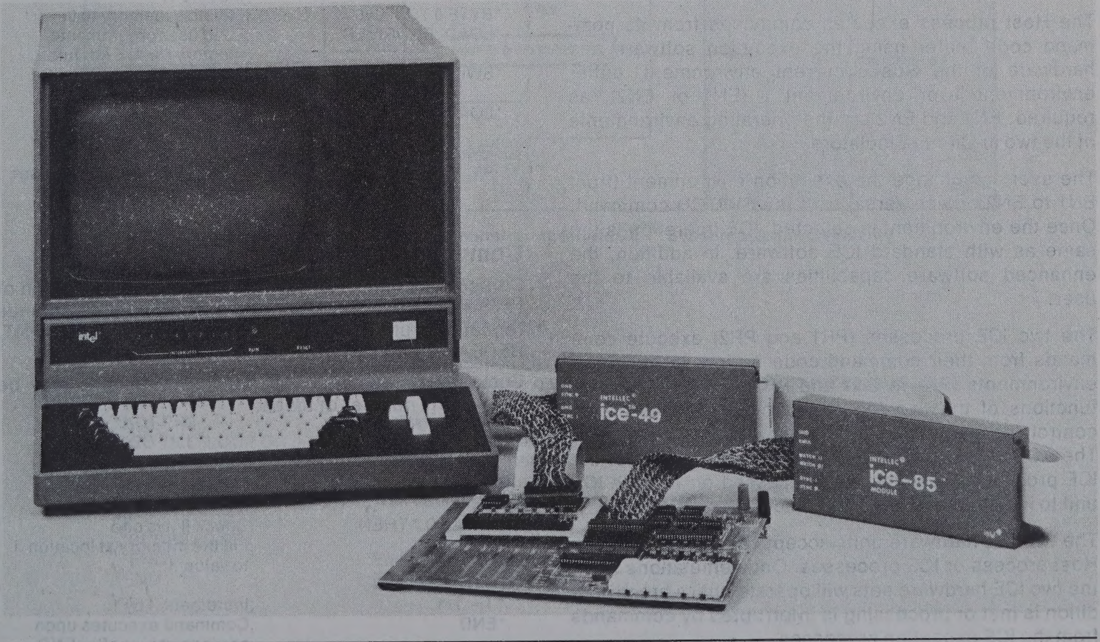
Functions under the supervision of ISIS-II Disk Operating System.

Supports ICE-85 Emulator Hold Request/Hold Acknowledgement handshake while in both emulation and interrogation modes. (Can be used for Dynamic RAM refresh.)

Multi-ICE In-Circuit Emulator is a software product which allows two Intel In-Circuit Emulators to run simultaneously in a single Intellec Microcomputer Development System. Multi-ICE software used in lieu of the standard ICE software gives users full control of the Intellec Microcomputer Development System, and the two ICE modules for hardware and software debugging of multi-processor systems.

Enhancement features available with Multi-ICE software include a compound command capability which enables the user to ''program'' a diagnostic or exercise sequence. Also included are repeat and conditional execution of ICE commands, and the ability to invoke the macro commands by name.

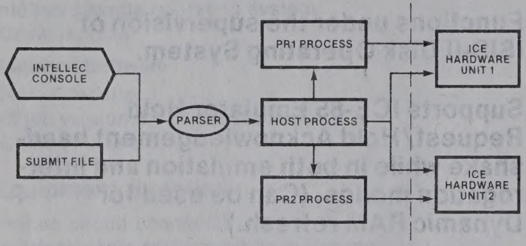
A special EPROM set for the ICE-85 Emulator is included. The new firmware will enable the ICE-85 Emulator to support Hold-Request and Hold-Acknowledgement hand-shake protocol both while in emulation and while in interrogation mode. This allows the ICE-85 Emulator to support typical dynamic RAM and DMA applications.



MULTI-ICE OPERATION

Multi-ICE software is a debug tool which allows two ICE emulators to begin and stop in sequence. Once started, two ICE emulators emulate simultaneously and independently. Thus, Multi-ICE software permits the debugging of asynchronous or synchronous multiprocessor systems.

A conceptual model for the Multi-ICE software can be illustrated with the following block diagram.



Block Diagram of Multi-ICE™ Operation

There are three processes in the Multi-ICE environment: the Host process and the two ICE processes to control the two ICE hardware modules. The processor for these three processes is the microcomputer in the Intellec Microcomputer Development System. Only the Host process is active when Multi-ICE software is invoked. The Parser interfaces with the console, receives commands from the console or from a file, translates them into intermediate code, and loads the code into the Host command code buffer or ICE command code buffers.

The Host process executes commands from its command code buffer using the execution software and hardware of the Host's current environment, either environment 1 or environment 2 (EN1 or EN2), as required. EN1 and EN2 are the operating environments of the two In-Circuit Emulators.

The user can change the execution environment (from EN1 to EN2 or vice versa) with the SWITCH command. Once the environment is selected, ICE operation is the same as with standard ICE software. In addition, the enhanced software capabilities are available to the user.

The two ICE processes (PR1 and PR2) execute commands from their command code buffers in their own environments (PR1 in EN1 and PR2 in EN2). The main functions of the two ICE execution processes are to control the operations of the two ICE hardware sets. The ACTIVATE command controls the execution of the ICE processes. Commands are passed on to each ICE unit to initiate the desired ICE functions.

The two ICE hardware units accept commands from the Host process or ICE processes. Once emulations start, the two ICE hardware sets will operate until a break condition is met or processing is interrupted by commands from the ICE execution processes.

ENHANCED DIAGNOSTIC SOFTWARE FUNCTIONS

Single ICE Operation

Multi-ICE software can be used for single ICE operation. The operating procedures will be identical to the Multi-ICE operation. All the enhanced software functions will be available. The performance will be the same as if the standard ICE software is being used.

Symbolic Display of Addresses

The user has the option of displaying a 16-bit address in the form of a symbol name or line number plus a hex number offset.

Macro Command

A macro is a set of commands which is given a name. Thus, a group of commands which is executed frequently may be defined as a macro. Each time the user wants to execute that group of commands, he may just invoke the macro by typing a colon followed by the macro name. Up to ten parameters may be passed to the macro.

Macro commands may be defined at the beginning of a debug session and then can be used throughout the whole session. If the user wants to save the macros for later use, he may use the PUT command to save the macro on diskette, or the user may edit the macro file off-line using the Intellec text editor. Later, the user may use the INCLUDE command to bring in the macro definition file that he created.

Example:

```
*DEFINE MACRO INITMEM     ;This macro clears the
                           memory and then loads the
                           programs.
.*SWITCH = EN1            ;Select environment 1 (ICE
                           Module 1)
.*BYTE 0 TO 100=0         ;Initialize memory to 0.
.*LOAD :F1:DRIVER         ;Load user program into
                           memory for ICE Module 1.
.*SWITCH = EN2            ;Select environment 2 (ICE
                           Module 2)
.*LOAD :F1:DR2            ;Load user program into
                           memory for ICE Module 2..
.*EM                      ;End of Macro
*                         ;To execute this Macro, user
                           types :INITMEM
```

Compound Command

Compound commands provide conditional execution of commands (IF Command) and execution of commands repeatedly until certain conditions are met (COUNT, REPEAT Commands).

Compound commands and Macro commands may be nested any number of times.

Example:

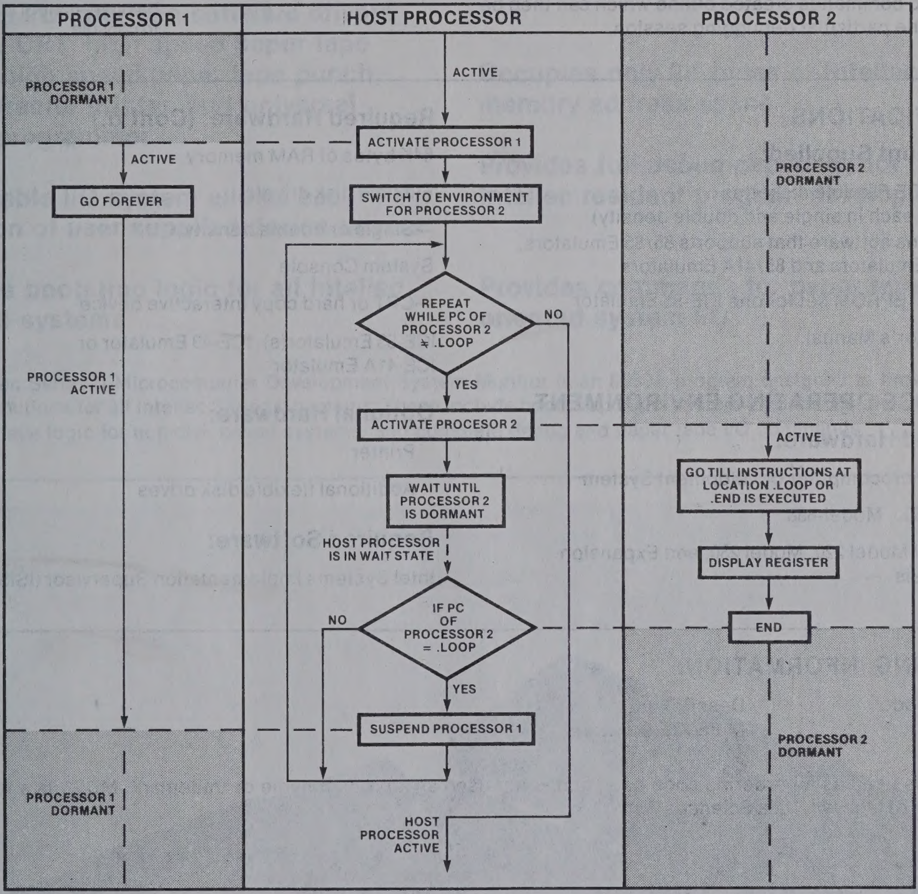
```
*DEFINE .I = 0            ;Define symbol .I to 0
*COUNT 100H               ;Repeat the following
                           commands 100H times.
.*IF .I AND 1 THEN        ;Check if .I is odd
..*BYT .I = .I            ;Fill the memory at location .I
                           to value .I
..*END
.*.I = .I+1               ;Increment .I by 1.
.*END                     ;Command executes upon
                           carriage-return after END
```

Software Synchronization of Processes

Up to three processes (Host, PR1 and PR2) can be active simultaneously in the system. An ICE process can be activated (ACTIVATE), suspended (SUSPEND), killed (KILL), or continued (CONTINUE). The Host process can wait for other processes to become dormant before it becomes active again. Through these synchronization commands, the user can create a system test file off-line yet be able to synchronize the three processes when the actual system test is executed.

Example:

The capability of the software synchronization commands is demonstrated by the following example. The flowchart shows the synchronization requirements. The program steps show the actual implementation.


PROCESSOR 1
HOST PROCESSOR
PROCESSOR 2
PROCESSOR 1 DORMANT
ACTIVE
ACTIVATE PROCESSOR 1
ACTIVE
GO FOREVER
SWITCH TO ENVIRONMENT FOR PROCESSOR 2
PROCESSOR 2 DORMANT
REPEAT WHILE PC OF PROCESSOR 2 ≠ .LOOP
NO
YES
PROCESSOR 1 ACTIVE
ACTIVATE PROCESOR 2
ACTIVE
WAIT UNTIL PROCESSOR 2 IS DORMANT
GO TILL INSTRUCTIONS AT LOCATION .LOOP OR .END IS EXECUTED
HOST PROCESSOR IS IN WAIT STATE
DISPLAY REGISTER
IF PC OF PROCESSOR 2 = .LOOP
NO
END
YES
SUSPEND PROCESSOR 1
PROCESSOR 2 DORMANT
PROCESSOR 1 DORMANT
HOST PROCESSOR ACTIVE

Flowchart of the Example for Demonstrating Multi-ICE™ Synchronization Capability

```
*ACTIVATE PR1               ;Activate PR1
.*GO FROM 800               ;Start ICE Module 1
.*END                       ;End of Activate block
PR1 EMULATION BEGUN
*SWI=EN2                    ;Switch execution Environment to EN2
*REPEAT                     ;Repeat the following block of commands while PC is not equal to .Loop
.*WHILE PC< >.LOOP
.*ACT PR2                   ;Activate PR2
..*GO TILL .LOOP OR .END    ;Go till instruction at location .Loop or at location .END is executed
..*REGISTER                 ;Display the registers
..*END                      ;End of Activate block
.*WAIT PR2                  ;Wait until PR2 is dormant
.*IF PC=.LOOP THEN
..*SUSPEND PR1
..*END                      ;End of IF block
.*END                       ;End of REPEAT block
*
```

MULTI-ICE™ SOFTWARE

INCLUDE File Capability

The INCLUDE command causes input to be taken from the file specified until the end of the file is encountered, at which point, input continues to be taken from the previous source. Nesting of INCLUDES is permitted. Since the command code file can be complex, the ability to edit offline becomes desirable. The INCLUDE command allows the user to pull in command code files and Macro commands created offline which can then be used for the particular debugging session.

Example:

```
*INCLUDE :F1:PROG1          ;Cause input to be taken
                             from file PROG1
*MAP 0 LENGTH 64K=USER      ;Contents of the file PROG1
                             are listed on screen as they
                             are executed.
*MAP IO 0 TO FF = USER
*SWITCH = EN2
*LOAD :F2:LED.HEX
*SWITCH = EN1               ;End of the file PROG1
*                           ;After the end of file is
                             reached, control is returned
                             to console.
```

SPECIFICATIONS

Equipment Supplied:

- Multi-ICE Flexible diskettes
  (one each in single and double density)
  Contains software that supports 85/85 Emulators, 85/49 Emulators and 85/41A Emulators
- Special EPROM set for one ICE-85 Emulator
- Operator's Manual

MULTI-ICE OPERATING ENVIRONMENT

Required Hardware:

Intellec Microcomputer Development System

—Model-800, Model-888

—Series II Model 220, Model 230, and Expansion Chassis

Required Hardware: (Cont'd.)

64K bytes of RAM memory

Flexible disk drive(s)

—Single or double density

System Console

—CRT or hard copy interactive device

ICE-85 Emulator(s), ICE-49 Emulator or ICE-41A Emulator

Optional Hardware:

Printer

Additional flexible disk drives

Required Software:

Intel Systems Implementation Supervisor (ISIS-II)

ORDERING INFORMATION:

Product Code	Description
MDS*-350	Multi-ICE Software

*"MDS" is used as an ordering code only, and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corp.

SYSTEM MONITOR
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

ROM resident

Provides I/O interface software drivers for TTY, CRT, high speed paper tape reader, high speed paper tape punch, line/character printer, and universal PROM programmer

Expandable I/O system allows easy inclusion of user supplied device drivers

Provides bootstrap logic for all Intellec Series II systems

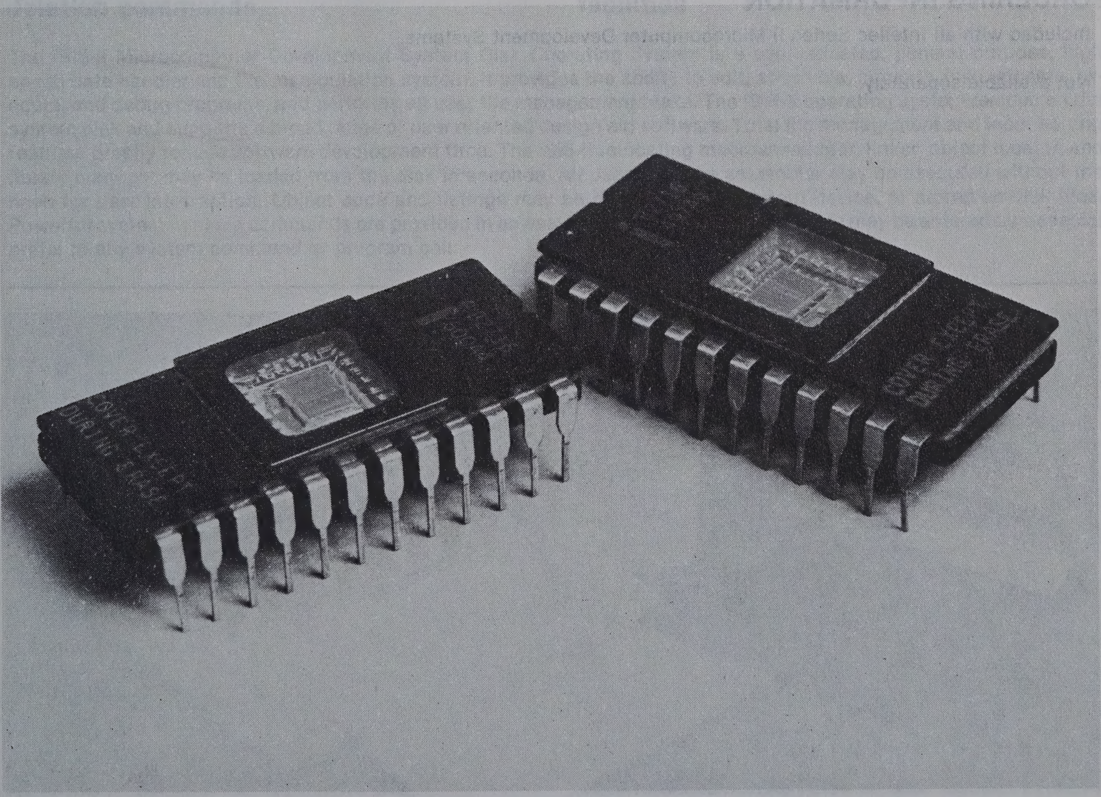
Provides self-test diagnostic capability for Intellec CPU and RAM memory

Occupies only 2K bytes of Intellec memory address space

Provides full debug capability for Intellec resident program development

Provides commands for paper tape oriented system I/O

The Intellec Series II Microcomputer Development System Monitor is an 8080A program designed to provide basic control functions for all Intellec Series II systems. These include bootstrap logic, system diagnostics, the I/O system, user interface logic for non-disk based systems, and complete debug and paper tape I/O commands.



FUNCTIONAL DESCRIPTION

Memory

The system monitor occupies 4K bytes of 8080A memory, although it only uses 2K bytes of Intellec Series II memory space. The remaining 2K bytes of memory contain bootstrap and diagnostic code and are "shadowed" (executed only upon system reset and then disabled in favor of RAM memory present at the same locations.)

Bootstrap Control

Upon system reset, the hardware enables the 2K code segment containing bootstrap and diagnostic logic, and forces a jump to the starting location. The bootstrap then determines if a diskette drive is present and ready, and transfers control either to the system monitor or ISIS-II diskette operating system. The bootstrap and diagnostic code segment is then disabled and removed from 8080A memory space.

User Commands

The monitor accepts and executes user commands. These commands include:

- read paper tape into memory
- punch memory to paper tape
- execute programs in memory with breakpoints
- display/modify memory and CPU registers
- fill memory with a constant
- hexadecimal arithmetic
- execute user diagnostics

Together these commands provide powerful program loading and debug facilities for the non-disk-based user.

Input/Output

The monitor also provides a comprehensive I/O system, including drivers for all standard Intellec Series II devices, as well as linkage mechanism for easy inclusion of non-standard I/O devices. The monitor recognizes four logical I/O devices — a reader device, punch device, console device, and list device. Each logical device may be assigned to any one of four physical I/O devices by means of a monitor command. Device drivers are provided for each standard Intellec peripheral selected by user command. Non-standard devices may be used by "linking" drivers through known absolute memory locations. The system is designed to operate, at a minimum, with a TTY as its sole I/O device.

ORDERING INFORMATION

Included with all Intellec Series II Microcomputer Development Systems.

Not available separately.

intel®

ISIS-II
DISKETTE OPERATING SYSTEM
MICROCOMPUTER DEVELOPMENT SYSTEM

Supports up to two hard disk drives (4 platters), four double density drives and two single density drives, providing up to 17 megabytes of storage in one system with up to 200 files per diskette, and 992 files per disk platter

Relocating MCS-80/MCS-85 macroassembler contains extended macro and conditional assembly capability

Command file facility allows console commands to be submitted from disk file

Disk operating system functions callable from user programs

Disk system text editor provides string search, substitution, insertions, and deletion commands

Supports resident, high level programming languages, PL/M, FORTRAN, BASIC, and COBOL

Provides dynamic allocation and deallocation of disk sectors for variable length files

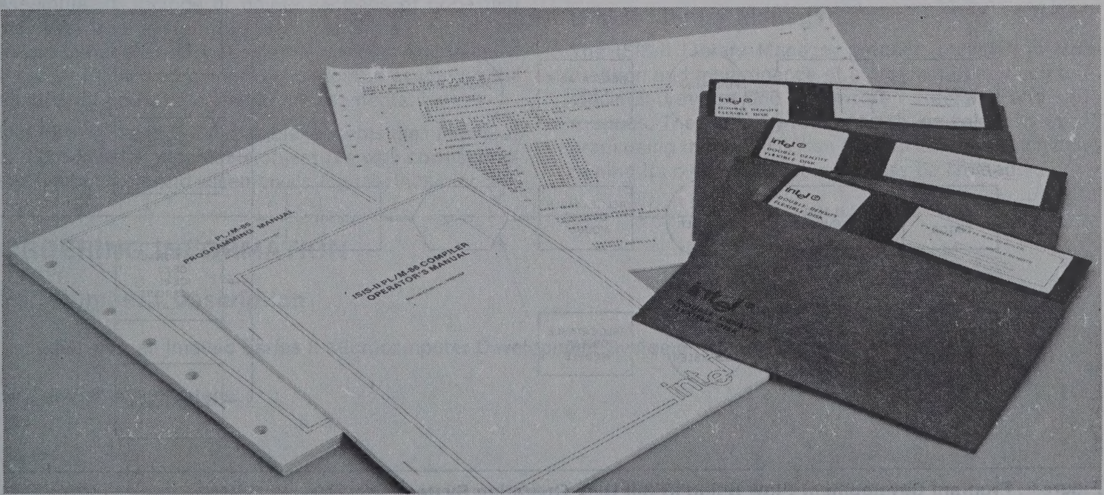
Linker automatically combines separately assembled or compiled programs into single relocatable module

Library manager creates and updates program libraries

Supports all standard Intellec peripherals

Provides access to all Intellec monitor facilities

The ISIS-II Microcomputer Development System Disk Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system. It provides the ability to edit, assemble, compile, link, relocate, execute, and debug programs, and performs all user file management tasks. The ISIS-II operating system resides on the system disk and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the disk in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as disk files. Powerful system console commands are provided in an easy to use context. Monitor mode may be entered by a special prefix to any system command or program call.


PL/M-86 PROGRAMMING MANUAL
ISIS-II PL/M-86 COMPILER OPERATOR'S MANUAL
intel
intel DOUBLE DENSITY FLEXIBLE DISK
intel DOUBLE DENSITY FLEXIBLE DISK
intel DOUBLE DENSITY FLEXIBLE DISK

FUNCTIONAL DESCRIPTION

The ISIS-II operating system resides on the system disk and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the disk in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as disk files. A diagram of the ISIS-II system program development flow is shown in Figure 1.

ISIS-II Files

A file is a user defined collection of information of variable length. ISIS-II also treats each of the standard Intellec system peripherals as files through preassignment of unique file names to each device. In this manner data may be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one disk data file to another. ISIS-II provides automatic implementation of random access disk files. each file is identified by a user chosen name unique on its disk. Up to 200 files may be stored on each disk, 992 on each hard disk platter.

ISIS-II System Commands

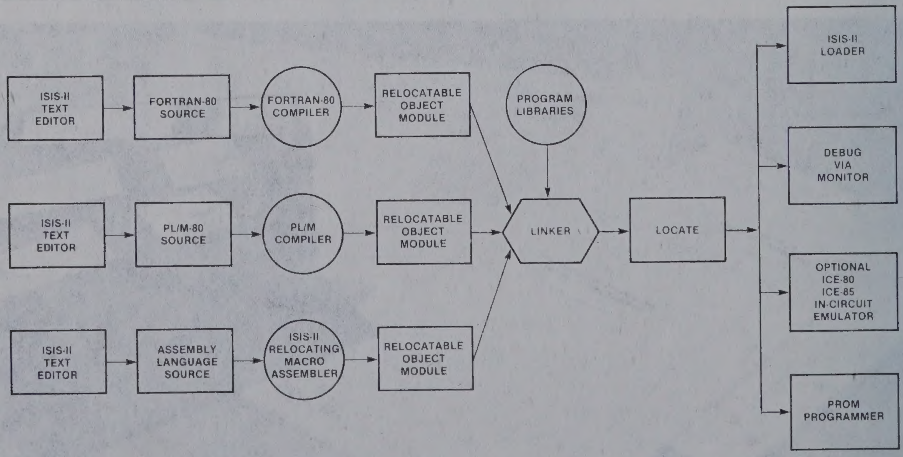
ISIS-II system commands are designed to provide the user with a powerful, easy to use program and file manipulation capability. Several commands have the capability of operating on several files at once via the wildcard file naming convention. As an example, the command DELETE ★ .OBJ deletes all files in the disk directory with the suffix .OBJ. A summary of ISIS-II system commands is presented in Table 1.

Call Capability — The delete, rename, and attribute assignment commands, along with a set of file I/O routines, are callable from user written programs. This allows the user to open, close, read, and write disk files, access standard peripheral devices, write error messages, and load other programs via simple program call statements.

Command	Operation
Initialize disk	Initializes a diskette for use by the system. Requires only one disk drive.
Attribute assignment	Assigns specified attributes to a file, such as write-protect.
Copy	Creates copies of existing diskette files or transfers files from one device to another.
Delete	Removes a file from the diskette, thereby freeing space for allocation of other files.
Directory	Lists name, size, and attributes of files from a specified diskette directory.
Rename	Allows diskette files to be renamed.
Format	Initializes a diskette for use by the system. (Use with two or more drives.)
Debug	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and or debugging.
Submit	Provides capability for executing a series of ISIS-II commands previously written to a diskette file.

Additional commands are provided for support of the hard disk.

Table 1. ISIS-II System Commands



ISIS-II TEXT EDITOR
FORTRAN-80 SOURCE
FORTRAN-80 COMPILER
RELOCATABLE OBJECT MODULE
PROGRAM LIBRARIES
ISIS-II TEXT EDITOR
PL/M-80 SOURCE
PL/M COMPILER
RELOCATABLE OBJECT MODULE
LINKER
LOCATE
ISIS-II TEXT EDITOR
ASSEMBLY LANGUAGE SOURCE
ISIS-II RELOCATING MACRO ASSEMBLER
RELOCATABLE OBJECT MODULE
ISIS-II LOADER
DEBUG VIA MONITOR
OPTIONAL ICE-80 ICE-85 IN-CIRCUIT EMULATOR
PROM PROGRAMMER

Figure 1. Program Development Flow Using ISIS-II Disk Operating System

ISIS-II Text Editor

The ISIS-II text editor is a comprehensive tool for assembly language, PL/M, and FORTRAN program entry and correction for Intel microcomputers. Its command set allows either entire lines of text or individual characters to be manipulated within a line.

Program Entry — Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

Utility Commands — To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

Storage — The contents of the workspace are stored on diskette and can be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II MCS-80/MCS-85 macroassembler.

For users with 64K of RAM memory, the CREDIT Text Editor is available. See CREDIT data sheet for more information.

ISIS-II MCS-80/MCS-85 Relocating Macroassembler

Address Translation — The ISIS-II MCS-80/MCS-85 macroassembler translates assembly language mnemonics into relocatable and/or absolute object code modules. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Extended macro capability eliminates the need to rewrite similar sections of code repeatedly, and thus simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code that may vary from system to system, such as the code required to handle optional external devices. Additionally, the user is allowed complete freedom in assigning the location of code, data, and stack segments.

List File — The ISIS-II Assembler accepts disk file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. A cross reference listing is also option-optionally produced. The list file may then be examined from the system console or copied to a specified list device.

Object File — The relocatable object file generated by the assembler may be combined with other object programs residing on the disk to form a single relocatable object module or it can be converted to an absolute form for subsequent loading and execution.

ISIS-II Linker

The ISIS-II linker provides the capability to combine the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module. The linker automatically resolves all external program and data references during the linking process. Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays. An optional link map showing the contents and lengths of each segment in the output module can be requested. All unsatisfied external references are also listed. If requested by the user, the ISIS-II linker can search a specified set of program libraries for routines to be included in the output module.

ISIS-II Object Locator

The ISIS-II locate program takes output from either the resident FORTRAN or PL/M compilers, the macroassembler, or the linker and transforms that output from relocatable format to an absolute format which may then be loaded via the standard ISIS-II loader, or loaded into an appropriate in-circuit emulator (ICE) module. During the locate process, code, data, and stack segments may be separately relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack are directed to RAM addresses. A locate map showing absolute addresses for each code and data segment and a symbol table dump listing symbols, attributes, and absolute address may also be requested.

ISIS-II Library Manager

The ISIS-II Library Manager program provides for the creation and maintenance of a program library containing Intel-provided and user-written programs and subroutines. These library routines may be linked to a program using the ISIS-II linker. Several libraries, each containing its own set of routines, may be created.

ORDERING INFORMATION

Part Number Description

Included with all Intellec Series II Microcomputer Development Systems.

Not available separately.

CREDIT
CRT-BASED TEXT EDITOR
MICROCOMPUTER DEVELOPMENT SYSTEMS

Provides interactive editing of ASCII Text Files

CRT screen display with cursor-based editing using single character commands for insertion, deletion, page forward and backward

Command line editing with string search, deletion, and insertion

Moves blocks of text within text files

Combines source text from several files

Dynamic macro command definition

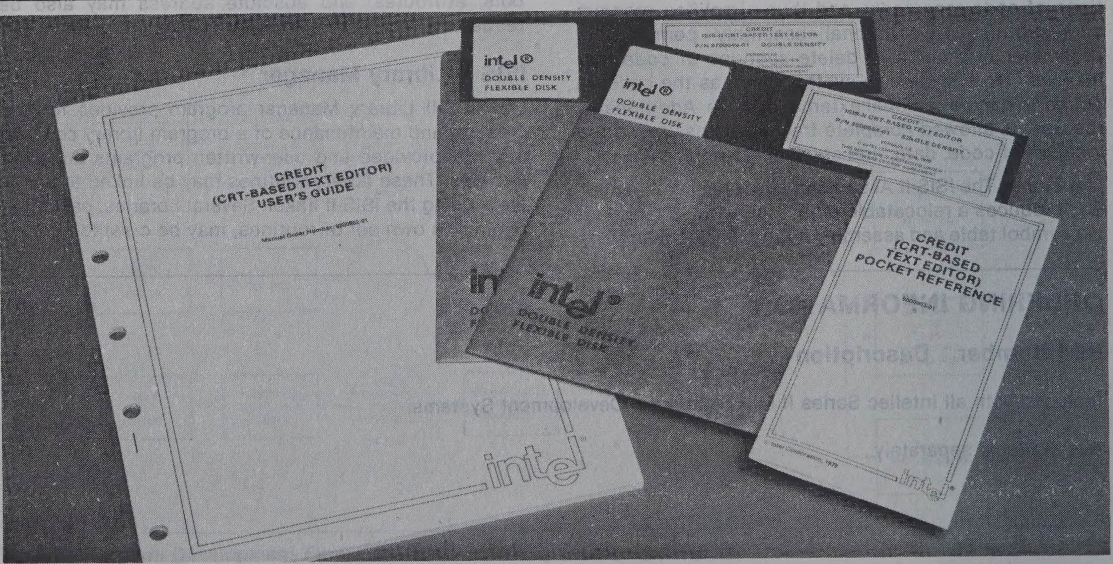
Operates under the ISIS-II operating system on Intellec® and Intellec Series-II Microcomputer Development Systems

HELP command for display of command information

CREDIT is a CRT-based text editor that aids in the creation and editing of ASCII text files on Intellec Microcomputer Development Systems. Once the text has been edited to the programmer's satisfaction, it can be directed to the appropriate language processor for compilation, assembly or interpretation. CREDIT features are easy to use and simplify the change or rearrangement of text files. CREDIT runs under ISIS-II on any Intellec or Intellec Series II Microcomputer Development System with an Intel supplied CRT, disk drive(s) and 64K bytes of memory.

There are two editing modes in CREDIT: a screen mode and a command line mode. The screen mode makes full use of the display characteristics of the CRT. The cursor position is visible on the screen and can be positioned by use of the cursor control keys. Display text can be corrected in two ways—either by simply retyping the text, or by using the single stroke control keys. Specifically, the single character control keys are used for change, deletion, insertion and paging forward and paging backward.

In addition to screen editing, there is command line editing, which includes commands for more powerful and complex editing tasks. Some examples of functions available in the command line mode are search, block move and copy, macro definition and manipulation of external files. These easily used, high level commands facilitate complex editing and speed microcomputer development.



CREDIT FEATURES

- Two editing modes: cursor-driven screen editing and command line context editing

CRT editing includes:

- Single control key commands for insertion, deletion, page forward and backward
- Type-over correction and replacement
- Immediate feedback of the results of each operation
- The current state of the text is always represented on the display

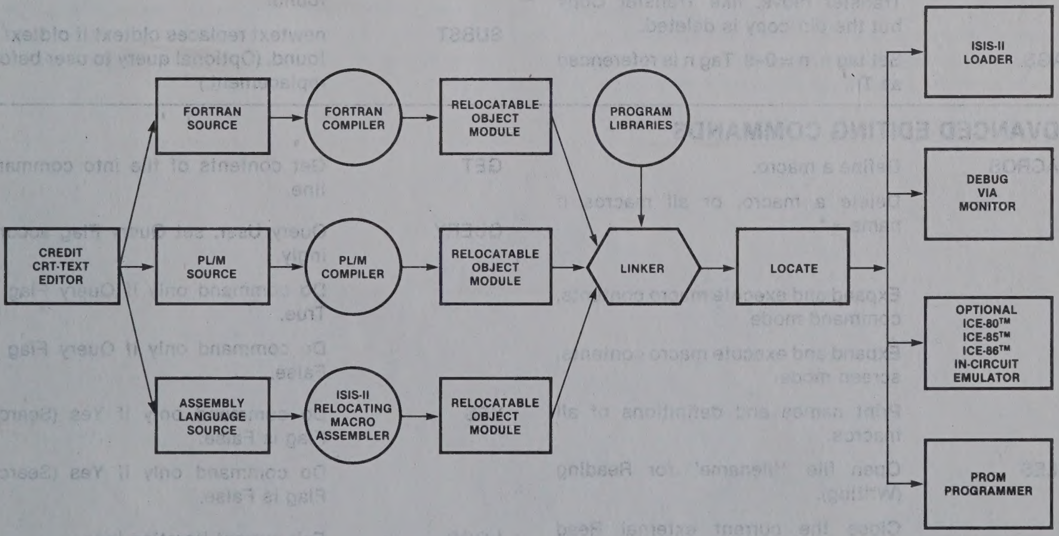
Command line editing includes:

- String search and substitute
- String delete, change or insert
- Block move
- Block copy
- User-defined macros
- External file handling
- Change CREDIT features with ALTER command
- Conditional iteration
- User-defined tab settings
- Symbolic tag positions
- Automatic disk full warning
- Runs under ISIS-II SUBMIT facility
- Option to exit at any time with original file intact
- HELP command

BENEFITS OF CREDIT

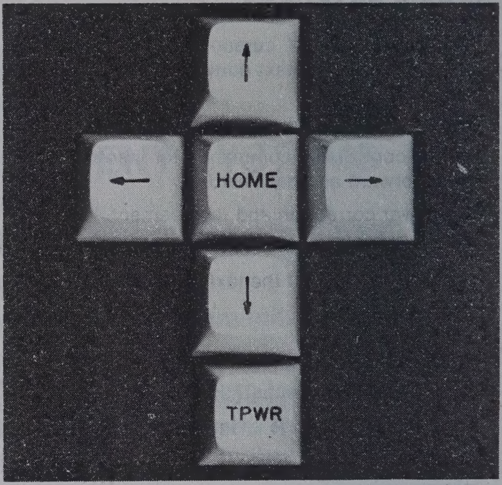
- Speeds source program creation and editing— lowers the costs of these functions
- Easy to learn and use—
  - —source text is clearly displayed
  - —single command keys used for CRT editing
  - —HELP command is available for easy reference when needed
- Complements existing software — source text used for PL/M, FORTRAN, BASIC, and Assemblers and all 8086 Software Products
- Aids in the management of source file libraries
- Offers full use of Intel supplied CRT cursor functions

MICROCOMPUTER PROGRAM DEVELOPMENT


CREDIT CRT-TEXT EDITOR
FORTRAN SOURCE
PL/M SOURCE
ASSEMBLY LANGUAGE SOURCE
FORTRAN COMPILER
PL/M COMPILER
ISIS-II RELOCATING MACRO ASSEMBLER
RELOCATABLE OBJECT MODULE
RELOCATABLE OBJECT MODULE
RELOCATABLE OBJECT MODULE
PROGRAM LIBRARIES
LINKER
LOCATE
ISIS-II LOADER
DEBUG VIA MONITOR
OPTIONAL ICE-80™ ICE-85™ ICE-86™ IN-CIRCUIT EMULATOR
PROM PROGRAMMER

SCREEN MODE COMMANDS

MOVE CURSOR:	Use the directional arrow keys on the keyboard.
REPLACE:	Type over existing text with replacement new text.
INSERT:	Insert one character.
	Insert more than one character.
DELETE:	Delete one character.
	Set boundaries and delete all text between them.
PAGE:	Next Page: Get next screenful of text.
	Previous Page: Get previous screenful.
	View Page: Rewrite current page with possible reframing.



COMMAND MODE COMMANDS

HELP	Display summary of commands.
PRINT	Print n lines or up to tag.
JUMP	Move cursor position n characters or to tag.
	Move cursor position n lines forward or backward.
MOVE	Transfer Copy block of text from tag1, for n lines or through tag2, to cursor position.
	Transfer move: like Transfer Copy but the old copy is deleted.
TAGS	Set tag n, n = 0–9. Tag n is referenced as Tn.

EXIT	Normal exit.
	Exit Quit: Abandon any changes to edit file.
INSERT	Insert before CP all text between delimiters.
DELETE	Delete n characters, or characters up to tag.
	Delete n lines forward or backward.
FIND	Search for text; move pointer if found.
SUBST	newtext replaces oldtext if oldtext is found. (Optional query to user before replacement.)

ADVANCED EDITING COMMANDS

MACROS	Define a macro.
	Delete a macro, or all macros if name = *.
	Expand and execute macro contents, command mode.
	Expand and execute macro contents, screen mode.
	Print names and definitions of all macros.
FILES	Open file "filename" for Reading (Writing).
	Close the current external Read (Write) file.
	Go to beginning of current Read file.
	Read and insert n lines from the Read file.
	Write n lines at CP to the external Write file.

GET	Get contents of file into command line.
QUERY	Query User: set Query Flag accordingly.
	Do command only if Query Flag is True.
	Do command only if Query Flag is False.
YES	Do command only if Yes (Search) Flag is False.
	Do command only if Yes (Search) Flag is False.
LOOP	Exit current iteration loop.
ALTER	Change environmental parameters.
	Change functional parameters.
USER	Copy text to the console.
HELP	Display summary of commands.

SPECIFICATIONS

Required Hardware

Intellec Microcomputer Development System
—MDS-800
—Series-II Model 220, Model 230

64K bytes of RAM memory

Diskette Drive(s)
—Single or double density

System Console
—INTEL supplied CRT

Optional Hardware

Line Printer
Additional diskette drive(s)

Required Software

ISIS-II Diskette Operating System
—Single or double density

Documentation Package

CREDIT (CRT-Based Text Editor) User's Guide (9800902)
CREDIT Pocket Reference (9800903)

Shipping Media

Flexible Diskettes
—Single and double density

ORDERING INFORMATION

Product Code	Description
MDS-360	ISIS-II CREDIT CRT-Based Text Editor

PL/M-80
HIGH LEVEL PROGRAMMING LANGUAGE INTELLEC RESIDENT COMPILER

Provides resident operation on Intellec Microcomputer Development System and Intellec Series II microcomputer development systems

Produces relocatable and linkable object code

Sophisticated code optimization reduces application memory requirements

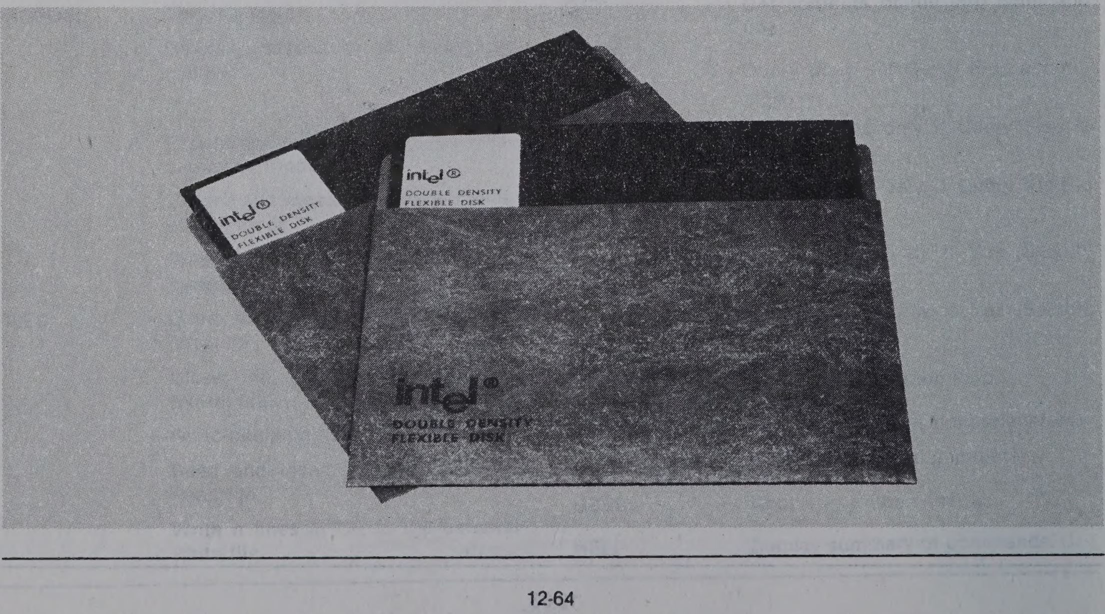
Speeds project completion with increased programmer productivity

Cuts software development and maintenance costs

Improves product reliability with simplified language and consequent error reduction

Eases enhancement as system capabilities expand

The PL/M-80 High Level Programming Language Intellec Resident Compiler is an advanced, high level programming language for Intel 8080 and 8085 microprocessors, iSBC-80 OEM computer systems, and Intellec microcomputer development systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs. PL/M is an algorithmic language in which program statements naturally express the algorithm to be programmed, thus freeing programmers to concentrate on system development rather than assembly language details (such as register allocation, meanings of assembler mnemonics, etc.). The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080/8085 instructions. Substantially fewer PL/M statements are necessary for a given application than would be using assembly language or machine code. Since PL/M programs are problem oriented and thus more compact, programming in PL/M results in a high degree of productivity during development efforts, resulting in significant cost reduction in software development and maintenance for the user.



FUNCTIONAL DESCRIPTION

The PL/M compiler is an efficient multiphase compiler that accepts source programs, translates them into object code, and produces requested listings. After compilation, the object program may be first linked to other modules, then located to a specific area of memory, and finally executed. The diagram shown in Figure 1 illustrates a program development cycle where the program consists of three modules: PL/M, FORTRAN, and assembly language. A typical PL/M compiler procedure is shown in Table 1.

Features

Major features of the Intel PL/M-80 compiler and programming language include:

Resident Operation — on Intellec microcomputer development systems eliminates the need for a large in-house computer or costly timesharing system.

Object Code Generation — of relocatable and linkable object codes permits PL/M program development and debugging in small modules, which may be easily linked with other modules and/or library routines to form a complete application.

Extensive Code Optimization — including compile time arithmetic, constant subscript resolution, and common subexpression elimination, results in generation of short, efficient CPU instruction sequences.

Symbolic Debugging — fully supported in the PL/M compiler and ICE-85 in-circuit emulators.

Compile Time Options — includes general listing format commands, symbol table listing, cross reference listing, and "innerlist" of generated assembly language instructions.

Block Structure — aids in utilization of structured programming techniques.

Access — provided by high level PL/M statements to hardware resources (interrupt systems, absolute addresses, CPU input/output ports).

Data Definition — enables complex data structures to be defined at a high level.

Re-entrant Procedures — may be specified as a user option.

Benefits

PL/M is designed to be an efficient, cost-effective solution to the special requirements of microcomputer software development as illustrated by the following benefits of PL/M use:

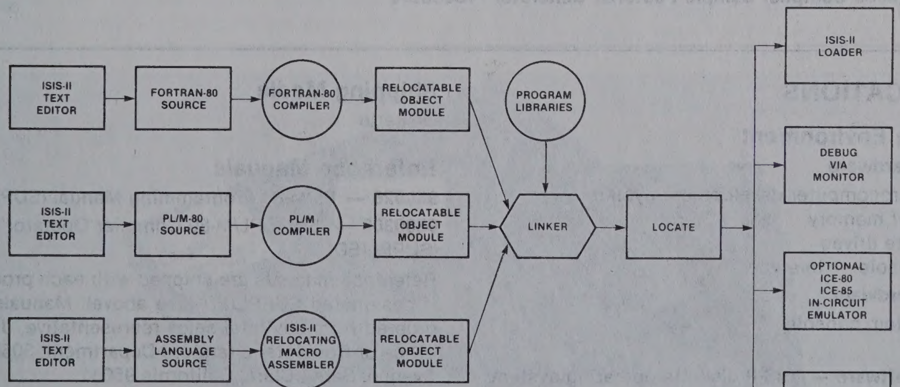
Low Learning Effort — even for the novice programmer, because PL/M is easy to learn.

Earlier Project Completion — on critical projects, because PL/M substantially increases programmmer productivity while reducing program development time.

Lower Development Cost — because increased programmer productivity requiring less programming resources for a given function translates into lower software development costs.

Increased Reliability — because of PL/M's use of simple statements in the program algorithm, which are easier to correct and thus substantially reduce the risk of costly errors in systems that have already reached full production status.

Easier Enhancement and Maintenance — because programs written in PL/M are easier to read and easier to understand than assembly language, and thus are easier to enhance and maintain as system capabilities expand and future products are developed.


ISIS-II TEXT EDITOR
FORTRAN-80 SOURCE
FORTRAN-80 COMPILER
RELOCATABLE OBJECT MODULE
PROGRAM LIBRARIES
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RELOCATABLE OBJECT MODULE
LINKER
LOCATE
ISIS-II TEXT EDITOR
ASSEMBLY LANGUAGE SOURCE
ISIS-II RELOCATING MACRO ASSEMBLER
RELOCATABLE OBJECT MODULE
ISIS-II LOADER
DEBUG VIA MONITOR
OPTIONAL ICE-80 ICE-85 IN-CIRCUIT EMULATOR
PROM PROGRAMMER

Figure 1. Program Development Cycle Block Diagram

Simpler Project Development — because the Intellec microcomputer development system with resident PL/M-80 is all that is needed for developing and debugging software for 8080 and 8085 microcomputers, and the use of expensive (and remote) timesharing or large computers is consequently not required.

```
                    $OBJECT(:F1:FACT.OB2)
                    $DEBUG
                    $XREF
                    $TITLE('FACTORIAL GENERATOR — PROCEDURE')
                    $PAGEWIDTH(80)

 1                  FACT:
                    DO;

 2    1             DECLARE NUMCH BYTE PUBLIC;

 3    1             FACTORIAL: PROCEDURE (NUM,PTR) PUBLIC;
 4    2                DECLARE NUM BYTE, PTR ADDRESS;
 5    2                DECLARE DIGITS BASED PTR (161) BYTE;
 6    2                DECLARE (I,C,M) BYTE;

 7    2                NUMCH = 1; DIGITS(1) = 1;
 9    2                DO M = 1 TO NUM;
10    3                   C = 0;
11    3                   DO I = 1 TO NUMCH;
12    4                      DIGITS(I) = DIGITS(I)*M + C;
13    4                      C = DIGITS(I)/10;
14    4                      DIGITS(I) = DIGITS(I) — 10*C;
15    4                   END;

16    3                   IF C<>0 THEN
17    3                   DO;
18    4                      NUMCH = NUMCH + 1; DIGITS(NUMCH) = C;
20    4                      C = DIGITS(NUMCH)/10;
21    4                      DIGITS(NUMCH) = DIGITS(NUMCH) — 10*C;
22    4                   END
                       END;

24    2             END FACTORIAL;

25    1             END;
```

Table 1. PL/M-80 Compiler Sample Factorial Generator Procedure

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec microcomputer development system
65K bytes of memory
Dual diskette drives
System console — teletype

Optional Hardware

CRT as system console
Line printer

Required Software — ISIS-II diskette operating system

Shipping Media

Diskette

Reference Manuals

980026 — PL/M-80 Programming Manual (SUPPLIED)

9800300 — ISIS-II PL/M-80 Compiler Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code	Description
MDS-PLM	High level language compiler.

intel®

FORTRAN-80
8080/8085 ANS FORTRAN 77
INTELLEC® RESIDENT COMPILER

Meets and exceeds ANS FORTRAN 77 Subset Language Specification

Supports Intel Floating Point Standard with either the floating point support library or the iSBC-310 High Speed Mathematics Board

Resident operation on Intellec® Microcomputer Development System and Intellec® Series II Microcomputer Development System

Supports full symbolic debugging with ICE-80™ and ICE-85™

Produces relocatable and linkable object code compatible with resident PL/M-80 and 8080/8085 Macro Assembler

Full FORTRAN 77 language I/O support or optional RMX-80 run-time library

Well defined I/O interface for configuration with user-supplied drivers

Sophisticated code optimization insures efficient program implementation

FORTRAN-80 is a computer industry-standard, high-level programming language and compiler that translates FORTRAN statements into relocatable object modules. When the object modules are linked together and located into absolute program modules, they are suitable for execution on Intel® 8080/8085 Microprocessors, iSBC-80 OEM Computer Systems, and Intellec® Microcomputer Development Systems. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 Language Subset Specification[1]. The compiler operates on the Intellec Microcomputer Development System under the ISIS-II Disk Operating Systems and produces efficient relocatable object modules that are compatible for linkage with PL/M-80 and 8080/8085 Macro Assembler modules.

The ANS FORTRAN 77 language specification offers many powerful extensions to the FORTRAN language that are especially well suited to Intel® 8080/8085 Microprocessor software development. Because FORTRAN-80 conforms to the ANS FORTRAN 77 standard, the user is assured of compatibility with existing FORTRAN software that meets the standard as well as a guarantee of upward compatibility to other computer systems supporting an ANS FORTRAN 77 Compiler.

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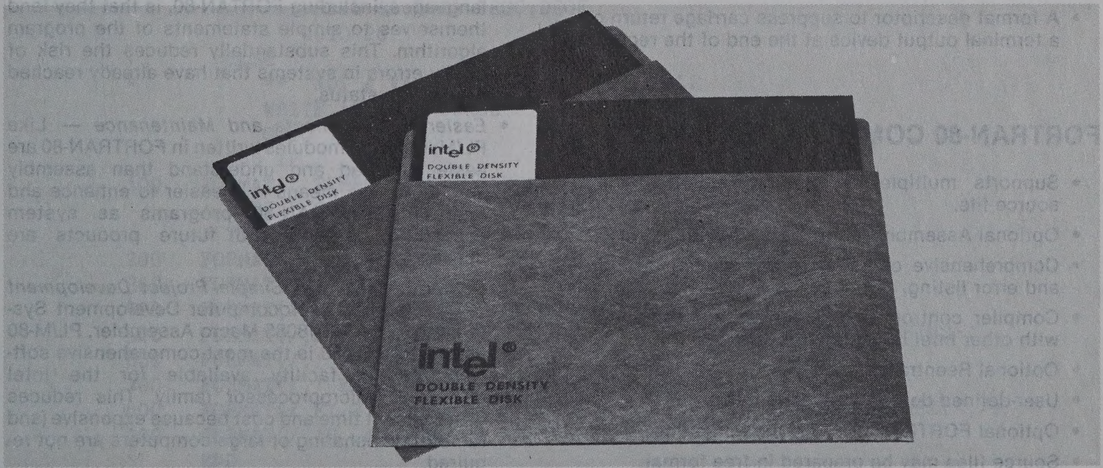
[1] ANSI X3J3/90



FORTRAN-80 LANGUAGE FEATURES

Major ANS FORTRAN 77 features supported by the Intel® FORTRAN-80 Programming Language include:

- Structured Programming is supported with the IF ... THEN ... ELSE IF ... ELSE ... END IF constructs.
- CHARACTER data type permits alphanumeric data to be handled as strings rather than characters stored in array elements.
- Full I/O capabilities include:
  - Sequential and Direct Access files
  - Error handling facilities
  - Formatted, Free-formatted, and Unformatted data representation
  - Internal (in-memory) file units provide capability to format and reformat data in internal memory buffers
  - List Directed Formatting
- Supports arrays of up to seven dimensions.
- Supports logical operators

  .EQV. — Logical equivalence
  .NEQV. — Logical nonequivalence

Major extensions to FORTRAN 77 in Intel FORTRAN-80 include:

- Direct 8080/8085 port I/O supported by intrinsic subroutines.
- Binary and Hexadecimal integer constants.
- Well defined interface to FORTRAN-80 I/O statements (READ, OPEN, etc.), allowing easy use of user-supplied I/O drivers.
- User-defined INTEGER storage lengths of 1, 2 or 4 bytes.
- User-defined LOGICAL storage lengths of 1, 2 or 4 bytes.
- REAL STORAGE lengths of 4 bytes.
- Bitwise Boolean operations using logical operators on integer values.
- Hollerith data constants.
- Implicit extension of the length of an integer or logical expression to the length of the left-hand side in an assignment statement.
- A format descriptor to suppress carriage return on a terminal output device at the end of the record.

FORTRAN-80 COMPILER FEATURES

- Supports multiple compilation units in single source file.
- Optional Assembly Language code listing.
- Comprehensive cross-reference, symbol attribute and error listing.
- Compiler controls and directives are compatible with other Intel language translators.
- Optional Reentrancy.
- User-defined default storage lengths.
- Optional FORTRAN 66 Do Loop semantics.
- Source files may be prepared in free format.
- The INCLUDE control permits specified source files to be combined into a compilation unit at compile time.
- Transparent interface for software and hardware floating point support, allowing either to be chosen at time of linking.

FORTRAN-80 BENEFITS

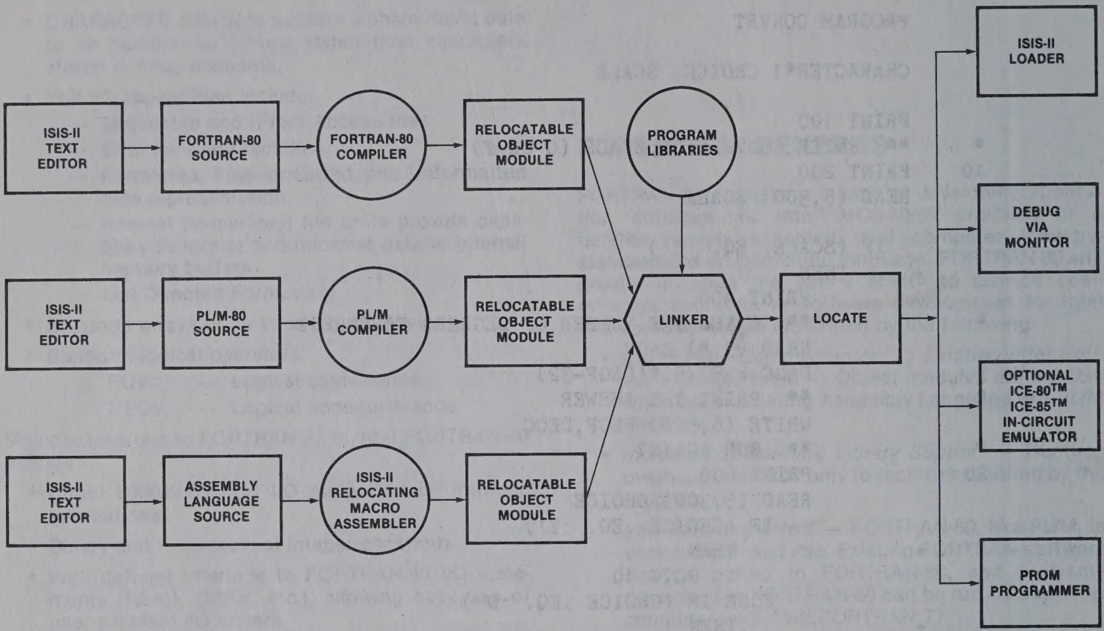
FORTRAN-80 provides a means of developing application software for Intel® MCS-80/85 products in a familiar, widely accepted, and computer industry-standardized programming language. FORTRAN-80 will greatly enhance the user's ability to provide cost-effective solutions to software development for Intel microprocessors as illustrated by the following:

- *Completely Complementary to Existing Intel Software Design Tools* — Object modules are linkable with new or existing Assembly Language and PL/M Modules.
- *Incremental Runtime Library Support* — Runtime overhead is limited only to facilities required by the program.
- *Low Learning Effort* — FORTRAN-80, like PL/M, is easy to learn and use. Existing FORTRAN software can be ported to FORTRAN-80, and programs developed in FORTRAN-80 can be run on any other computer with ANS FORTRAN 77.
- *Earlier Project Completion* — Critical projects are completed earlier than otherwise possible because FORTRAN-80 will substantially increase programmer productivity, and is complementary to PL/M Modules by providing comprehensive arithmetic, I/O formatting, and data management support in the language.
- *Lower Development Cost* — Increases in programmer productivity translates into lower software development costs because less programming resources are required for a given function.
- *Increased Reliability* — The nature of high-level languages, including FORTAN-80, is that they lend themselves to simple statements of the program algorithm. This substantially reduces the risk of costly errors in systems that have already reached production status.
- *Easier Enhancements and Maintenance* — Like PL/M, program modules written in FORTRAN-80 are easier to read and understand than assembly language. This means it is easier to enhance and maintain FORTRAN-80 programs as system capabilities expand and future products are developed.
- *Comprehensive, Yet Simple Project Development* — The Intellec Microcomputer Development System, with the 8080/8085 Macro Assembler, PL/M-80 and FORTRAN-80 is the most comprehensive software design facility available for the Intel MCS-80/85 Microprocessor family. This reduces development time and cost because expensive (and remote) timesharing or large computers are not required.

SAMPLE FORTRAN-80 SOURCE PROGRAM LISTING

```
*   **  THIS PROGRAM IS AN EXAMPLE OF ISIS-II FORTRAN-80 THAT
*   **  CONVERTS TEMPERATURE BETWEEN CELSIUS AND FARENHEIT

      PROGRAM CONVRT

      CHARACTER*1 CHOICE, SCALE

      PRINT 100
*     **  ENTER CONVERSION SCALE (C OR F)
10    PRINT 200
      READ (5,300) SCALE

        IF (SCALE .EQ. 'C')
     +     THEN
              PRINT 400
*             **  ENTER THE NUMBER OF DEGREES FARENHEIT
              READ (5,*) DEGF
              DEGC = 5./9.*(DEGF-32)
*             **  PRINT THE ANSWER
              WRITE (6,500) DEGF,DEGC
*             **  RUN AGAIN?
20            PRINT 600
              READ (5,300) CHOICE
                 IF (CHOICE .EQ. 'Y')
     +              THEN
                       GOTO 10
                 ELSE IF (CHOICE .EQ. 'N')
     +              THEN
                       CALL EXIT
                 ELSE
                    GOTO 20
                 END IF
        ELSE IF (SCALE .EQ. 'F')
     +     THEN
*             **  CONVERT FROM FARENHEIT TO CELSIUS
              PRINT 700
              READ (5,*) DEGC
              DEGF = 9./5.*DEGC+32.
*             **  PRINT THE ANSWER
              WRITE (6,800) DEGC,DEGF
              GOTO 20
        ELSE
*          **  NOT A VALID ENTRY FOR THE SCALE
           WRITE (6,900) SCALE
           GOTO 10
        END IF
100   FORMAT(' TEMPERATURE CONVERSION PROGRAM',//,
     +' TYPE C FOR FARENHEIT TO CELSIUS OR',/,
     +' TYPE F FOR CELSIUS TO FARENHEIT',//)
200   FORMAT(/,' CONVERSION? ',$)
300   FORMAT(A1)
400   FORMAT(/,'ENTER DEGREES FARENHEIT: ',$)
500   FORMAT(/,F7.2,  DEGREES FARENHEIT = ',F7.2,' DEGREES CELSIUS')
600   FORMAT(/,' AGAIN (Y OR N)? ',$)
700   FORMAT(/,' ENTER DEGREES CELSIUS: ',$)
800   FORMAT(/,F7.2,' DEGREES CELSIUS = ',F7.2,' DEGREES FARENHEIT',/)
900   FORMAT(/,1H ,A1,' NOT A VALID CHOICE - TRY AGAIN!',/)
      END
```

The FORTRAN-80 Compiler is an efficient, multiphase compiler that accepts source programs, translates them into relocatable object code, and produces requested listings. After compilation, the object program may be linked to other modules, located to a specific area of memory, then executed. The diagram shown below illustrates a program development cycle where the program consists of modules created by FORTRAN-80, PL/M-80 and the 8080/8085 Macro Assembler.


ISIS-II TEXT EDITOR
FORTRAN-80 SOURCE
FORTRAN-80 COMPILER
RELOCATABLE OBJECT MODULE
ISIS-II TEXT EDITOR
PL/M-80 SOURCE
PL/M COMPILER
RELOCATABLE OBJECT MODULE
ISIS-II TEXT EDITOR
ASSEMBLY LANGUAGE SOURCE
ISIS-II RELOCATING MACRO ASSEMBLER
RELOCATABLE OBJECT MODULE
PROGRAM LIBRARIES
LINKER
LOCATE
ISIS-II LOADER
DEBUG VIA MONITOR
OPTIONAL ICE-80™ ICE-85™ IN-CIRCUIT EMULATOR
PROM PROGRAMMER

SPECIFICATIONS

OPERATING ENVIRONMENT

Required Hardware:

Intellec® Microcomputer Development System
— MDS-800, MDS-888
— Series II Model 220, Model 230

64K bytes of RAM memory

Dual diskette drives
— Single or Double Density

System console
— CRT or hardcopy interactive device

Optional Hardware:
Line Printer
ICE-80™, ICE-85™

Required Software:
ISIS-II Diskette Operating System
— Single or Double Density

Optional Software:
iSBC-801 FORTRAN-80 Run-Time Software Package for RMX-80

DOCUMENTATION PACKAGE

FORTRAN-80 Programming Manual (9800481)

ISIS-II FORTRAN-80 Compiler Operator's Manual (9800480)

FORTRAN-80 Programming Reference Card (9800547)

SHIPPING MEDIA

Flexible Diskettes
— Single and Double Density

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-301	FORTRAN-80 Compiler for Intellec Microcomputer Development Systems

BASIC-80
EXTENDED ANS 1978 BASIC
INTELLEC® RESIDENT INTERPRETER

Meets ANS 1978 standard for minimal BASIC and adds many powerful extensions

Operates under the ISIS-II operating system on Intellec and Intellec Series-II Microcomputer Development Systems

Full sequential and random disk file I/O with ISIS-II

Applications range from prototyping microcomputer software to inexpensive engineering and management problem solving on the Intellec systems

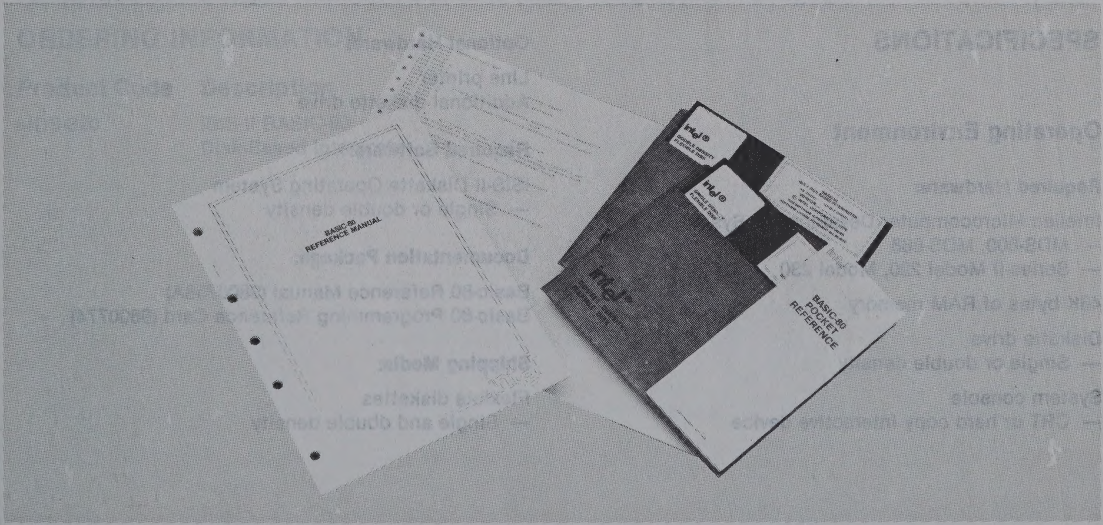
Supports the Intel floating point standard and provides integer and string data types

Can call user subroutines written in FORTRAN-80, PL/M-80, and 8080/85 macro assembler that are resident in the Intellec memory

Easily learned language and interactive environment combine to provide a flexible and powerful facility for developing programs to run on the Intellec Microcomputer Development Systems

BASIC is an industry standard, high-level programming language which is designed to be easily learned and used by novices and experienced programmers alike. The interpreter provides an interactive environment which allows fast and easy program development, testing, and debugging. BASIC is widely used for problem solving in engineering and management; extensive software exists for business applications such as order entry, accounts receivable, accounts payable, and inventory control, and engineering applications such as numeric and statistical analysis.

Intel's BASIC-80 meets the standards of ANS 1978 BASIC and extends them to take advantage of the software development capabilities of the Intellec Microcomputer Development Systems. The matching of these resources with the ease of programming in BASIC-80 provides a very effective tool for both microprocessor systems development and inexpensive applications programming and problem solving on the Intellec systems.



BASIC-80 LANGUAGE FEATURES

Standard ANS 78 BASIC features, all supported by BASIC-80, include:

- String and numeric constants, variables, and arrays.
- FOR . . . TO . . . STEP . . . NEXT statements for loop execution.
- IF . . . THEN statements for conditional execution.
- ON . . . GOTO statements for computed branching.
- GOSUB/RETURN subroutine calls and returns.
- Built in scientific functions:

ABS	RND	TAN
EXP	SGN	COS
INT	SQR	SIN
LOG	ATN	

- User defined single statement functions.

Major extensions to ANS 78 BASIC which BASIC-80 provides include:

- Support for the Intel single and double precision floating point standard.
- Disk file I/O, supporting both random access and sequential access files.
- Direct read and write to CPU I/O ports through the INP and OUT functions.
- Direct memory read and write through the PEEK and POKE functions.
- Calls to user-supplied external subroutines, which may have been written in FORTRAN-80, PL/M-80, or 8080/8085 Assembly Language and have been located at absolute memory locations using the ISIS-II facilities.
- User directed error trapping and handling functions.
- Program execution trace command.
- Formatted print statement with the PRINT USING function.
- ELSE clause for IF . . . THEN statements.
- Matrices with up to 110 dimensions.
- Extensive string manipulation functions.
- Boolean operators.
- Type conversion functions—integer, floating point, and character.

BENEFITS OF BASIC-80

- Added Value to the Intellec Systems—with BASIC-80 the Intellec Microcomputer Development Systems can be effectively used in many engineering and management applications.
- Inexpensive and Accessible Computational Facility—the ease of use and flexibility inherent in BASIC-80 and its interpretive environment fit well with the "at hand" computational resources of the Intellec systems. The combination is a particularly useful tool for obtaining fast and accurate results.
- Easy to Learn—the language is designed to be easily understood and learned. Results are obtained faster and people who may benefit from using the system can do so easily.
- Aid in Microcomputer Software Design—microcomputer software can be prototyped in BASIC-80 to inexpensively develop and test program logic.
- Complemented by Existing Software—subroutines written in PL/M-80, FORTRAN-80, and ASM 8080/85 can be called from BASIC-80 programs.
- Easy to Enhance and Maintain—BASIC-80, being straightforward and easily understood, provides for programs that are easy to maintain and modify in the future.

SPECIFICATIONS

Operating Environment

Required Hardware:

Intellec Microcomputer Development System
— MDS-800, MDS-888
— Series-II Model 220, Model 230

48K bytes of RAM memory

Diskette drive
— Single or double density

System console
— CRT or hard copy interactive device

Optional Hardware:

Line printer
Additional diskette drive

Required Software:

ISIS-II Diskette Operating System
— Single or double density

Documentation Package:

Basic-80 Reference Manual (9800758A)
Basic-80 Programming Reference Card (9800774)

Shipping Media:

Flexible diskettes
— Single and double density

EXAMPLE BASIC-80 PROGRAM

```
list
10 PRINT "THIS PROGRAM CALCULATES THE MEAN AND STANDARD"
20 PRINT " DEVIATION OF INPUT DATA"
30 S=0:V=0
40 INPUT "NUMBER OF VALUES";N
50 FOR I=1 TO N
60 INPUT A(I)
70 S=S+A(I)
80 NEXT
90 S=S/N
100 REM CALCULATION OF VARIANCE
110 FOR I=1 TO N
120 V=V+(A(I)-S)^2/N
130 NEXT
140 SD=SQR(V)
150 PRINT "MEAN=";S
160 PRINT "STANDARD DEVIATION IS=";SD
Ok

run
THIS PROGRAM CALCULATES THE MEAN AND STANDARD
 DEVIATION OF INPUT DATA
NUMBER OF VALUES? 6
? 34.7
? 32.9
? 38.2
? 35
? 37.6
? 40.9
MEAN= 36.55
STANDARD DEVIATION IS= 2.642442
Ok
```

ORDERING INFORMATION

Product Code	**Description**
MDS-320	ISIS-II BASIC-80 Disk-Based Interpreter

iCIS-COBOL™ SOFTWARE PACKAGE

Meets and exceeds minimum ANSI Level 1 standard for COBOL (X3.23-1974).

Runs under ISIS-II on Intellec or Intellec Series II Microcomputer Development Systems.

Compiler compiles COBOL source programs into an intermediate code which is optimized for speed and memory space.

Includes execution run-time interpreter and an interactive debugger.

Powerful extensions for interactive programming.

Can Link/Call routines written in PL/M-80, FORTRAN-80 and 8080/8085 Assembly Language.

FORMS utility program allows the user to design and test CRT screen format input by generating COBOL source code for the data descriptions defining that CRT screen format.

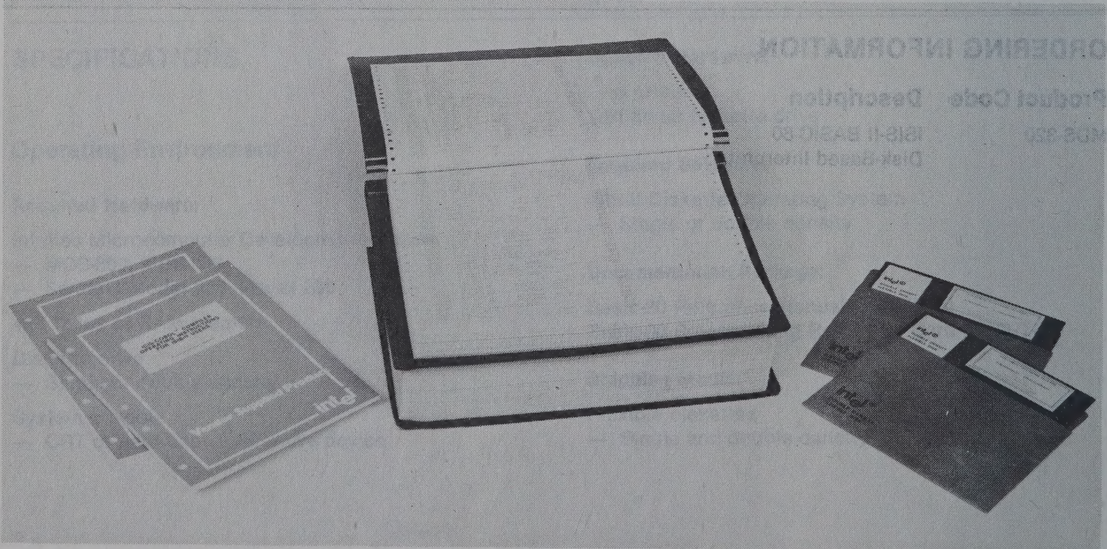
Compile-time option available to flag any non-ANSI standard features for portability.

Tested using U.S. Dept. of Navy COBOL validation system.

iCIS-COBOL, an acronym for Intel's Compact Interactive Standard COBOL, is a package designed to provide a powerful interactive business language to users of Intel's Intellec and Intellec Series II Microcomputer Development Systems. iCIS-COBOL contains the most relevant parts of the ANSI 74 standard plus extra extensions to make this product especially useful to Intellec users. The compiler provides a feature to optionally disallow the iCIS-COBOL extensions and rigidly enforce the ANSI 74 specification. This will prove beneficial to users who may need to port COBOL programs from the Intellec system to any other ANS Level 1 COBOL compiler.

iCIS-COBOL Compiler generates object code for a COBOL "virtual machine." This code is designed for optimum representation of COBOL verbs and data types. The code generated is interpreted by a Run-Time System. This consists of an interpreter which emulates the COBOL virtual machine and interfaces to the ISIS-II operating system and the CRT.

After an application program has been tested and is ready for production use, it is possible to link it permanently to the Run-Time System to form a free-standing ISIS-II loadable program.



LANGUAGE FEATURES

COBOL consists of twelve different modules implemented either to Level 1 or Level 2 as defined in the ANSI specification X3.23. iCIS-COBOL includes the following modules implemented to Level 1:

Nucleus
Table Handling
Sequential I/O
Relative I/O
Indexed I/O
Library
Interprogram Communication

Extensions to ANSI Specification:

- *Advanced screen formatting and data entry facilities.* These include protected and unprotected data, cursor manipulation, and numeric vet.
- *Run time input of filenames.* The actual value of the external filename may be moved to a file identifier location prior to OPENing the file, avoiding the need for an external linking mechanism.
- *Line sequential files.* Variable length records separated by carriage return/line feed saves space on disk and allows iCIS-COBOL programs to process files output by a text editor.
- *Hexadecimal literals.* These may be used to define control characters to output to special peripheral devices.
- *Rapid development facilities.* During development, compiled programs may be loaded directly by the Run-Time System "fast load" facility, thus avoiding the time otherwise spent in linking.
- *Interactive debugging.* Interactive debugging permits the setting of breakpoints, examination and modification of store, etc., at run time. Each COBOL statement is identified by a four-digit hexadecimal number.
- *Lower case.* This is permitted in COBOL words and comments, thus helping to produce easy to read documentation in the program.

INTERACTIVE CRT HANDLING

Intel has taken COBOL — traditionally a batch processing language — and extended it to become interactive. iCIS-COBOL offers many facilities for automatically formatting a CRT screen and facilitating input keying.

The user can format the screen of any system console (CRT) into protected and unprotected fields by using standard COBOL statements. The screen layout may be defined in the DATA DIVISION. An ACCEPT statement nominates a record description which permits input to the character positions corresponding to variables identified by data-names. These may be separated by FILLERs to position them on the screen. Conversely, a DISPLAY outputs only from non-FILLER fields in the record description which it nominates. The programmer can easily build up complex conversations for data entry and transaction processing.

When data is being keyed in, the operator has full cursor manipulation facilities, each variable acting as a tab stop. Non-numeric digits may not be keyed into fields defined as PIC 9. Finally, when the operator has checked that the data is correct, the RETURN key is pressed and processing continues.

SCREEN LAYOUT AND FORMAT FACILITIES	CURSOR CONTROL FACILITIES
Screen as a record description	HOME to the start of the first data field on the screen
FILLER	→ Forward space
REDEFINES	← Backward space
AT line:column	↓ Forward field
Character highlighting	↑ Backward field
Clear screen	C/R Release the screen of data
Numeric vet for PIC fields	L/F Left Fill numeric field
	(The actual keys used vary according to CRT keyboard)

FORMS UTILITY

A majority (up to 80%) of debugging time can be spent in designing, coding and testing the screen form input/output of a COBOL program. The FORMS utility included in the iCIS-COBOL package significantly reduces this debugging time.

Using the FORMS program, the user may:

- Store an image copy on disk of the form he has defined for subsequent use.
- Generate iCIS-COBOL source code for the data descriptions required to define the form just created. This may then be included in an iCIS-COBOL program using COPY.
- Choose to generate a checkout program which allows duplication of the many machine conversations which would take place during a run of the application which is being designed.

COMPILE TIME DIRECTIVES

- ANS

  If specified, the Compiler will accept only those iCIS-COBOL language statements that conform to the ANS 74 standard.
- RESEQ

  If specified, the Compiler generates COBOL sequence numbers, renumbering each line in increments of 10.
- NOINT

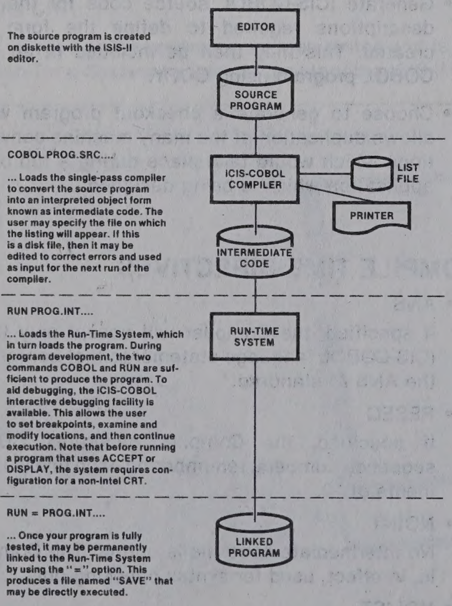
  No intermediate code file is output. The Compiler is, in effect, used for syntax checking only.
- NOLIST

  No list file is produced; used for fast compilation of "clean" programs.

- COPYLIST
  The contents of the file(s) nominated in COPY statements are listed.
- NOFORM
  No form feed or page headings are to be output by the Compiler in the list file.
- ERRLIST
  The listing is limited to those COBOL lines containing syntax errors together with the associated error message(s).
- INT (external-file-name)
  Specifies the file to which the intermediate code is to be directed.
- LIST (external-file-name)
  Specifies the file to which the listing is to be directed.
- FORM (integer)
  Specifies the number of COBOL lines per page of listing.
- NOECHO
  Error lines are echoed on the console unless this directive is specified.

BENEFITS

- Brings COBOL to Intellec Microcomputer Development Systems.
  - COBOL is the industry standard high-level language for business-oriented applications.
  - Most COBOL programs are self-documenting.
  - Conversational verbs and phrases and common business terminology make COBOL easy to learn, use and maintain.
  - More business and application programs are written in COBOL than any other language.
- Meets and exceeds ANS Level 1 COBOL standard.
  - Assures portability to and from all computers supporting ANS Level 1 COBOL.
  - Extensive testing and validation using U.S. NAVY COBOL VALIDATION SYSTEM assures functionality for all Level 1 features.
- iCIS-COBOL software package provides an easy to use, efficient and friendly environment for COBOL program development.
  - CONFIGURATOR program allows the user to reconfigure the software for any non-standard, non-Intel CRT.
  - Interactive debugger provides features aimed at a CRT based system (rather than batch-oriented).
  - FORMS utility program reduces total program development time by 30%.
  - All iCIS-COBOL utilities make use of CRT cursor control.
- Adds value to an Intellec development system.
  - COBOL applications programs developed using iCIS-COBOL software package will increase utilization of Intellec development systems.



The source program is created on diskette with the ISIS-II editor.

COBOL PROG.SRC....

... Loads the single-pass compiler to convert the source program into an interpreted object form known as intermediate code. The user may specify the file on which the listing will appear. If this is a disk file, then it may be edited to correct errors and used as input for the next run of the compiler.

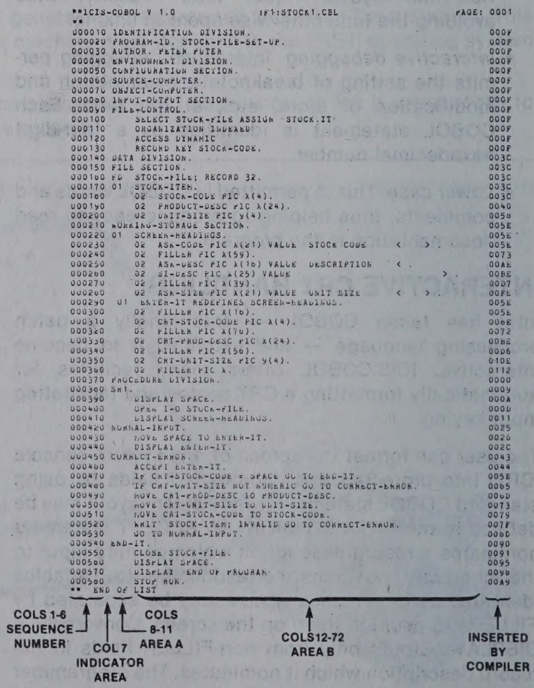
RUN PROG.INT....

... Loads the Run-Time System, which in turn loads the program. During program development, the two commands COBOL and RUN are sufficient to produce the program. To aid debugging, the iCIS-COBOL interactive debugging facility is available. This allows the user to set breakpoints, examine and modify locations, and then continue execution. Note that before running a program that uses ACCEPT or DISPLAY, the system requires configuration for a non-Intel CRT.

RUN = PROG.INT....

... Once your program is fully tested, it may be permanently linked to the Run-Time System by using the "=" option. This produces a file named "SAVE" that may be directly executed.

Figure 1. Program Development Cycle



```
**ICIS-COBOL V 1.0                :F1:STOCK1.CBL                    PAGE: 0001
**
000010 IDENTIFICATION DIVISION.                                          000F
000020 PROGRAM-ID. STOCK-FILE-SET-UP.                                    000F
000030 AUTHOR. PETER PUTER                                               000F
000040 ENVIRONMENT DIVISION.                                             000F
000050 CONFIGURATION SECTION.                                            000F
000060 SOURCE-COMPUTER.                                                  000F
000070 OBJECT-COMPUTER.                                                  000F
000080 INPUT-OUTPUT SECTION.                                             000F
000090 FILE-CONTROL.                                                     000F
000100     SELECT STOCK-FILE ASSIGN "STOCK.IT"                           000F
000110     ORGANIZATION INDEXED                                          000F
000120     ACCESS DYNAMIC                                                000F
000130     RECORD KEY STOCK-CODE.                                        000F
000140 DATA DIVISION.                                                    003C
000150 FILE SECTION.                                                     003C
000160 FD  STOCK-FILE; RECORD 32.                                        003C
000170 01  STOCK-ITEM.                                                   003C
000180     02  STOCK-CODE PIC X(4).                                      003C
000190     02  PRODUCT-DESC PIC X(24).                                   0040
000200     02  UNIT-SIZE PIC 9(4).                                       0058
000210 WORKING-STORAGE SECTION.                                          005E
000220 01  SCREEN-HEADINGS.                                              005E
000230     02  ASK-CODE PIC X(21) VALUE "STOCK CODE      <    >".         005E
000240     02  FILLER PIC X(59).                                         0073
000250     02  ASK-DESC PIC X(16) VALUE "DESCRIPTION     <".             00AE
000260     02  SI-DESC PIC X(25) VALUE "                        >".      00BE
000270     02  FILLER PIC X(39).                                         00D7
000280     02  ASK-SIZE PIC X(21) VALUE "UNIT SIZE       <    >".        00FE
000290  01  ENTER-IT REDEFINES SCREEN-HEADINGS.                          005E
000300     02  FILLER PIC X(16).                                         005E
000310     02  CRT-STOCK-CODE PIC X(4).                                  006E
000320     02  FILLER PIC X(76).                                         0072
000330     02  CRT-PROD-DESC PIC X(24).                                  00BE
000340     02  FILLER PIC X(56).                                         00D6
000350     02  CRT-UNIT-SIZE PIC 9(4).                                   010E
000360     02  FILLER PIC X.                                             0112
000370 PROCEDURE DIVISION.                                               0000
000380 SR1.                                                              0009
000390     DISPLAY SPACE.                                                000A
000400     OPEN I-O STOCK-FILE.                                          000D
000410     DISPLAY SCREEN-HEADINGS.                                      0011
000420 NORMAL-INPUT.                                                     0025
000430     MOVE SPACE TO ENTER-IT.                                       0026
000440     DISPLAY ENTER-IT.                                             002C
000450 CORRECT-ERROR.                                                    0043
000460     ACCEPT ENTER-IT.                                              0044
000470     IF CRT-STOCK-CODE = SPACE GO TO END-IT.                       005B
000480     IF CRT-UNIT-SIZE NOT NUMERIC GO TO CORRECT-ERROR.             0065
000490     MOVE CRT-PROD-DESC TO PRODUCT-DESC.                           006D
000500     MOVE CRT-UNIT-SIZE TO UNIT-SIZE.                              0073
000510     MOVE CRT-STOCK-CODE TO STOCK-CODE.                            0079
000520     WRITE STOCK-ITEM; INVALID GO TO CORRECT-ERROR.                007F
000530     GO TO NORMAL-INPUT.                                           008D
000540 END-IT.                                                           0090
000550     CLOSE STOCK-FILE.                                             0091
000560     DISPLAY SPACE.                                                0095
000570     DISPLAY "END OF PROGRAM"                                      0096
000580     STOP RUN.                                                     00A9
**  END OF LIST
```

Figure 2. Sample Program Listing Showing Source Format

SPECIFICATIONS

Operating Environment

Required Hardware:

Intellec Microcomputer Development System
— Model 800
— Series II Model 220, Model 230

48KB of Memory

Dual Diskette Drives
— Single or Double Density

System Console
— Intel or non-Intel CRT

Recommended Hardware:

64KB of Memory

Double Density Dual Diskette Drives

Optional Hardware:

Line Printer

Required Software:

ISIS-II Diskette Operating System
— Single or Double Density

Optional Software:

ISIS-II CREDIT (CRT-Based Text Editor)

Documentation Package

iCIS-COBOL Language Reference Manual (9800927-01)

iCIS-COBOL Compiler Operating Instructions for ISIS-II Users (9800928-01)

iCIS-COBOL Pocket Reference (9800929-01)

Shipping Media

Flexible Diskettes
— Single and Double Density

ORDERING INFORMATION:

Product Code	Description
MDS-380	iCIS-COBOL Software Package

MCS-48 DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec microcomputer development system to support MCS-48 development

MCS-48 assembler provides conditional assembly and macro capability

Takes advantage of powerful ISIS-II file handling and storage capabilities

Provides assembler output in standard Intel hex format

The MCS-48 assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes, and provides both conditional and macroassembler programming. Output may be loaded either to an ICE-49 module for debugging or into a Universal PROM Programmer for 8748 PROM programming. The MCS-48 assembler operates under the ISIS-II operating system on Intellec Microcomputer Development systems.

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FUNCTIONAL DESCRIPTION

The MCS-48 assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. The ability to refer to program addresses with symbolic names eliminates the errors of hand translation and makes it easier to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify which portions of the master source document should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices. Macro capability allows the programmer use of a single label to define a routine. The MCS-48 assembler will assemble the code required by the reserved routine whenever the macro label is inserted in the text. Output from the assembler is in standard Intel hex format. It may be either loaded directly to an in-circuit emulator (ICE-49) module for integrated hardware/software debugging, or loaded into a Universal PROM Programmer for 8748 PROM programming. A sample assembly listing is shown in Table 1.

```
ISIS-II 8048 MACROASSEMBLER, V1.0                               PAGE 1

LOC   OBJ                      SEQ           SOURCE STATEMENT

                                 1   ;DECIMAL ADDITION ROUTINE. ADD BCD NUMBER
                                 2   ;AT LOCATION 'BETA' TO BCD NUMBER AT 'ALPHA' WITH
                                 3   ;RESULT IN 'ALPHA.' LENGTH OF NUMBER IS 'COUNT' DIGIT
                                 4   ;PAIRS. (ASSUME BOTH BETA AND ALPHA ARE SAME LENGTH
                                 5   ;AND HAVE EVEN NUMBER OF DIGITS OR MSD IS 0 IF
                                 6   ;ODD)
                                 7   INIT     MACRO     AUGND,ADDND,CNT
                                 8            MOV       R0, #AUGND
                                 9   L1:      MOV       R1, #ADDND
                                10            MOV       R2, #CNT
                                11            ENDM
                                12   ;
0001E                           13   ALPHA    EQU       30
0028                            14   BETA     EQU       40
0032                            15   COUNT    EQU       5
0100                            16            ORG       100H
                                17            INIT      ALPHA, BETA, COUNT
0100  B81E                      18 +          MOV       R0, #ALPHA
0102  B928                      19 + L1:      MOV       R1, #BETA
0104  BA32                      20 +          MOV       R2, #COUNT
0106  97                        21            CLR       C
0107  F0                        22   LP:      MOV       A, @R0
0108  71                        23            ADDC      A, @R1
0109  57                        24            DA        A
010A  A1                        25            MOV       @R0, A
010B  18                        26            INC       R0
010C  19                        27            INC       R1
010D  EA07                      28            DJNZ      R2, LP
                                              END
USER SYMBOLS
ALPHA  0001E    BETA  0028    COUNT  0005    LP  0107
L1     0102

ASSEMBLY COMPLETE. NO ERRORS


ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V1.0                  PAGE 1

SYMBOL CROSS REFERENCE

 ALPHA  13#   17
 BETA   14#   17
 COUNT  15#   17
 INIT    7#   17
 L1     19#
 LP     22#   28
```

Table 1. Sample MCS-48 Diskette-Based Assembly Listing

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec Microcomputer Development System
32K RAM (non-macro use)
48K RAM (use of macro facility)
One or two Floppy disk drives
— Single or Double density
System Console
— CRT or interactive hardcopy device

Required Software

ISIS-II Diskette Operating System

Optional Hardware

ICE-49 In-Circuit Emulator
Line Printer
Universal PROM Programmer with 8748 personality card

Shipping Media

Diskette

Reference Manuals

9800255 — MCS-48 and UPI-41 Assembly Language Programming Manual (SUPPLIED)

9800236 — Universal PROM Mapper Operator's Manual

9800306 — ISIS-II User's Guide

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code	Description
MDS-D48	Diskette-based assembler for MCS-48 family of microprocessors.

8086/8088 SOFTWARE DEVELOPMENT PACKAGE

PL/M-86 high level programming language

ASM86 macro assembler for 8086/8088 assembly language programming

LINK86 and LOC86 linkage and relocation utilities

CONV86 converter for conversion of 8080/8085 assembly language source code to 8086/8088 assembly language source code

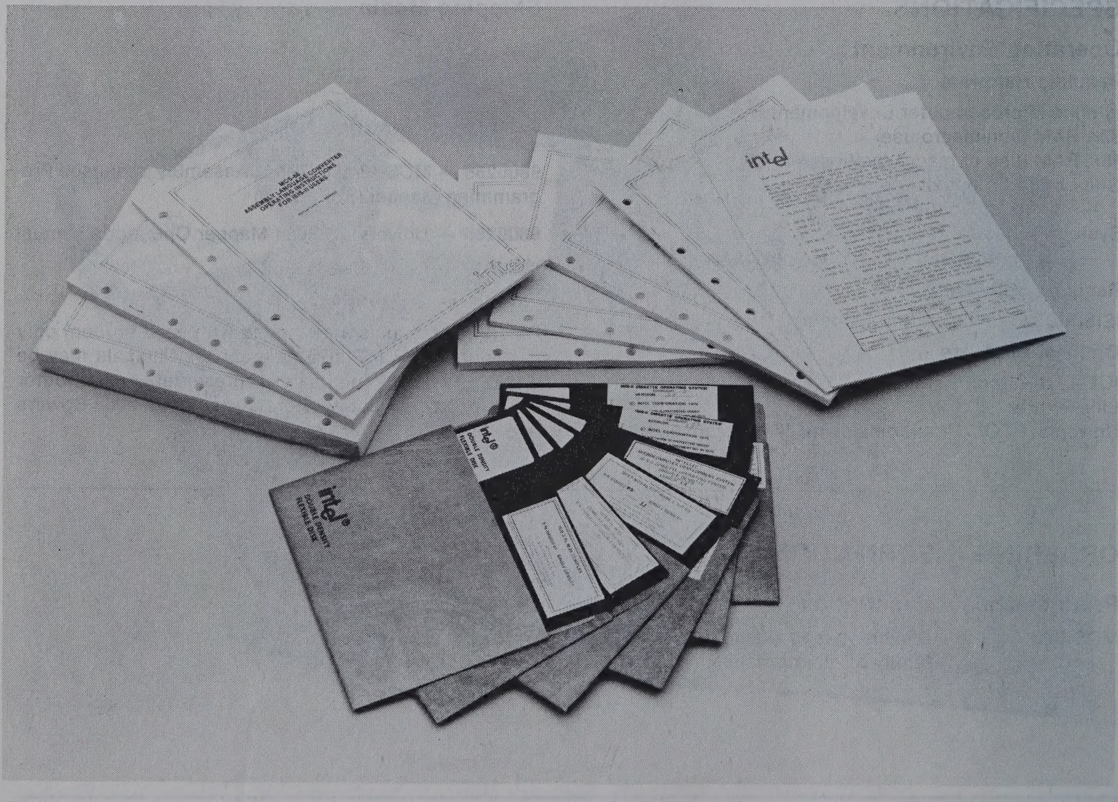
OH86 object-to-hexadecimal converter

LIB86 library manager

The 8086/8088 software development package provides a set of software development tools for the 8086 and the 8088 microprocessors and iSBC 86/12 single board computer. The package operates under the ISIS-II operating system on Intellec Microcomputer Development Systems—Model 800 or Series II—thus minimizing requirements for additional hardware or training for Intel Microcomputer Development System users.

The package permits 8080/8085 users to efficiently convert existing programs into 8086/8088 object code from either 8080/8085 assembly language source code or PL/M-80 source code.

For the new Intel Microcomputer Development System user, the package operating on an Intellec Model 230 Microcomputer Development System provides total 8086/8088 software development capability.



PL/M-86 HIGH LEVEL PROGRAMMING LANGUAGE

Sophisticated new compiler design allows user to achieve maximum benefits of 8086/8088 capabilities

Language is upward compatible from PL/M-80, assuring MCS-80/85 design portability

Supports 16-bit signed integer and 32-bit floating point arithmetic

Produces relocatable and linkable object code

Supports full extended addressing features of the 8086 and the 8088 microprocessors

Code optimization assures efficient code generation and minimum application memory utilization

Like its counterpart for MCS-80/85 program development, PL/M-86 is an advanced structured high level programming language. PL/M-86 is a new compiler created specifically for performing software development for the Intel 8086 and 8088 Microprocessors.

PL/M-86 has significant new capabilities over PL/M-80 that take advantage of the new facilities provided by the 8086 and the 8088 microprocessors, yet the PL/M-86 language remains upward compatible from PL/M-80.

With the exception of interrupts, hardware flags, and time-critical code sequences, PL/M-80 programs may be recompiled under PL/M-86 with little or no conversion required. PL/M-86, like PL/M-80, is easy to learn, facilitates rapid program development, and reduces program maintenance costs.

PL/M is a powerful, structured high level algorithmic language in which program statements can naturally express the program algorithm. This frees the programmer to concentrate on the system implementation without concern for burdensome details of assembly language programming (such as register allocation, meanings of assembler mnemonics, etc.).

The PL/M-86 compiler efficiently converts free-form PL/M language statements into equivalent 8086/8088 machine instructions. Substantially fewer PL/M statements are necessary for a given application than if it were programmed at the assembly language or machine code level.

Since PL/M programs are implementation problem oriented and more compact, use of PL/M results in a high degree of engineering productivity during project development. This translates into significant reductions in initial software development and follow-on maintenance costs for the user.

FEATURES

Major features of the Intel PL/M-86 compiler and programming language include:

- **Supports Five Data Types**
  - Byte: 8-bit unsigned number
  - Word: 16-bit unsigned number
  - Integer: 16-bit signed number
  - Real: 32-bit floating point number
  - Pointer: 16-bit or 32-bit memory address indicator
- **Block Structured Language**
  - Permits use of structured programming techniques
- **Two Data Structuring Facilities**
  - Array: Indexed list of same type data elements
  - Structure: Named collection of same or different type data elements
  - Combinations of Each: Arrays of structures or structures of arrays
- **Relocatable and Linkable Object Code**
  - Permits PL/M-86 programs to be developed and debugged in small modules. These modules can be easily linked with other PL/M-86 or ASM86 object modules and/or library routines to form a complete application system
- **Built-In String Handling Facilities**
  - Operates on byte strings or word strings
  - Six Functions: MOVE, COMPARE, TRANSLATE, SEARCH, SKIP, and SET
- **Automatic Support for 8086 Extended Addressing**
  - Three compiler options offer a separate model of computation for programs up to 1-Megabyte in size
- **Support for ICE-86 Emulator and Symbolic Debugging**
  - Debug option for inclusion of symbol table in object modules for In-Circuit Emulation with symbolic debugging

- **Numerous Compiler Options**
  - — A host of 26 compiler options including:
    - Conditional compilation
    - Included file or copy facility
    - Two levels of optimization
    - Intra-module and inter-module cross reference
    - Arbitrary placement of compiler and user files on any available combination of disk drives
- **Reentrant and Interrupt Procedures**
  - — May be specified as user options

BENEFITS

PL/M-86 is designed to be an efficient, cost-effective solution to the special requirements of 8086/8088 Microcomputer Software Development, as illustrated by the following benefits of PL/M-86 use:

- **Reduced Learning Effort** — PL/M-86 is easy to learn and to use, even for the novice programmer.
- **Earlier Project Completion** — Critical projects are completed much earlier than otherwise possible because PL/M-86, a structured high-level language, increases programmer productivity.
- **Lower Development Cost** — Increases in programmer productivity translate immediately into lower software development costs because less programming resources are required for a given programmed function.
- **Increased Reliability** — PL/M-86 is designed to aid in the development of reliable software (PL/M-86 programs are simple statements of the program algorithm). This substantially reduces the risk of costly correction of errors in systems that have already reached full production status, as the more simply stated the program is, the more likely it is to perform its intended function.
- **Easier Enhancements and Maintenance** — Programs written in PL/M tend to be self-documenting, thus easier to read and understand. This means it is easier to enhance and maintain PL/M programs as the system capabilities expand and future products are developed.
- **Simpler Project Development** — The Intellec Development Systems offer a cost-effective hardware base for the development of 8086 and 8088 designs. PL/M-86 and other elements of ISIS-II and the 8086/8088 Software Development Package are all that is needed for development of software for the 8086 and the 8088 microcomputers and iSBC 86/12 single board computer. This further reduces development time and costs because expensive (and remote) time sharing of large computers is not required. Present users of Intel Intellec Development Systems can begin to develop 8086 and 8088 designs without expensive hardware reinvestment or costly retraining.

SAMPLE PROGRAM

```
STATISTICS: DO;

/*The procedure in this module computes the mean and
variance of an array of data, X, of length N + 1, according
to the method of Kahan and Parlett (University of Cali-
fornia, Berkeley, Memo no. UCB/ERL M77/21.*/

STAT:  PROCEDURE(X$PTR,N,MEAN$PTR,
       VARIANCE$PTR) PUBLIC;

DECLARE
       (X$PTR,MEAN$PTR,VARIANCE$PTR) POINTER,
       X BASED X$PTR (1) REAL,
       N INTEGER,
       MEAN BASED MEAN$PTR REAL,
       VARIANCE BASED VARIANCE$PTR REAL,
       (M,Q,DIFF) REAL,
       I INTEGER;

M = X(0);
Q = 0.0;

DO  I = 1 TO N;
      DIFF = X(I) – M;
      M = M + DIFF/FLOAT(I + 1);
      Q = Q + DIFF*DIFF*FLOAT(I)/FLOAT(I + 1);
END;

MEAN = M;
VARIANCE = Q/FLOAT(N);

END STAT;

END STATISTICS;
```

ASM86 MACRO ASSEMBLER

A new assembler that encourages well-designed and well-structured programs

ASM86 is highly mnemonic and compact, with most mnemonics representing several distinct machine instructions

ASM86 will generate optimal code

Powerful and flexible text macro facility with three macro listing options to aid debugging

High-level data structuring such as "records" and "structures"

Powerful "EQU" (equate) facility allows complex expressions to be represented as a single symbol

Enhanced data handling capabilities

Fully detailed set of error messages

The 8086/8088 assembly language is "strongly typed". This means it performs extensive checks on the usage of variables and labels. The assembler uses the attributes which are derived explicitly when a variable or label is first declared, then makes sure that each use of a symbol in later instructions conforms to the usage defined for that symbol when it was declared.

Compared to earlier assemblers, ASM86 supports substantially improved flexibility in data definition and manipulation:

- STRUCTURES
- RECORDS
- PROCEDURES
- ARRAYS

Its capabilities allow very sophisticated goals and significantly simplified coding to be achieved with a straightforward use of the language.

For example a data RECORD smaller than a word may be defined as a collection of named bit-fields and operators for manipulating these subfields are automatically defined when the record is declared. Bit-fields within a record may be referenced directly by name.

Powerful string manipulation instructions permit direct transfers to or from memory or the accumulator. They can be prefixed with a repeat operator for repetitive execution with a count-down and a condition test. These operations automatically decrement or increment the relevant indexes to memory, depending on the direction flag.

The assembler fully supports the 8086/8088 addressing modes by providing for complex address expressions involving base and index registers and field offsets. A powerful EQU facility allows the use of simplified synonyms for complicated expressions which may occur throughout a module.

The 8086/8088 assembly language includes approximately 100 instruction mnemonics. From these few mnemonics, the assembler can generate over 3,800 distinct machine instructions. These instructions are differentiated by the assembler's ability to evaluate the "TYPE" of the operands to the instruction and then generate the proper machine instruction. ASM86 will generate the shortest machine instruction possible given no forward referencing or given explicit information as to the characteristics of the forward referenced symbol.

ASM86 provides a detailed set of error messages which may appear both in the regular list file and the error print file. As a debugging feature, the list file may include a detailed listing of the user symbol table.

ASM86 allows the user power and flexibility, and is fully compatible with LINK86, LOC86, QRL86 and LIB86.The ASM86 operator's manual includes details on linking ASM86 programs with programs written in PL/M-86.

ASM86 implements directives which reflect the high level orientation of the 8086 and the 8088 architecture.

CONV 86

MCS-80/85 to MCS-86 ASSEMBLY LANGUAGE CONVERTER UTILITY PROGRAM

Translates 8080/8085 Assembly Language Source Code to 8086/8088 Assembly Language Source Code

Provides a fast and accurate means to convert 8080/8085 programs to the 8086 and the 8088, facilitating program portability

Automatically generates proper ASM-86 directives to set up a "virtual 8080" environment that is compatible with PL/M-86.

In support of Intel's commitment to software portability, CONV86 is offered as a tool to move 8080/8085 programs to the 8086 and the 8088. A comprehensive manual, "MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users" (9800642), covers the entire conversion process. Detailed methodology of the conversion process is fully described therein.

CONV86 will accept as input an error-free 8080/8085 assembly-language source file and optional controls, and produce as output, optional PRINT and OUTPUT files.

The PRINT file is a formatted copy of the 8080/8085 source and the 8086/8088 source file with embedded caution messages.

The OUTPUT file is an 8086/8088 source file.

CONV86 issues a caution message when it detects a potential problem in the converted 8086/8088 code.

A transliteration of the 8080/8085 programs occurs, with each 8080/8085 construct mapped to its exact 8086/8088 counterpart:

—Registers
—Condition flags
—Instructions
—Operands
—Assembler directives
—Assembler control lines
—Macros

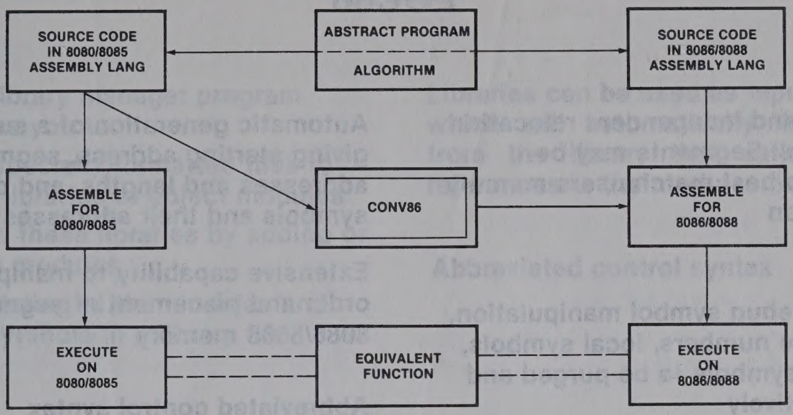
Because CONV86 is a transliteration process, there is the possibility of as much as a 15%-20% code expansion over the 8080/8085 code. For compactness and efficiency it is recommended that critical portions of programs be re-coded in 8086/8088 assembly language.

Also, as a consequence of the transliteration, some manual editing may be required for converting instruction sequences dependent on:

-instruction length, timing, or encoding
-interrupt processing
-PL/M parameter passing conventions

} mechanical editing procedures for these are suggested in the converter manual.

The accompanying diagram illustrates the flow of the conversion process. Initially, the abstract program may be represented in 8080/8085 or 8086/8088 assembly language to execute on that respective target machine. The conversion process is porting a source destined for the 8080/8085 to the 8086 or the 8088 via CONV86.


SOURCE CODE IN 8080/8085 ASSEMBLY LANG
ABSTRACT PROGRAM
ALGORITHM
SOURCE CODE IN 8086/8088 ASSEMBLY LANG
ASSEMBLE FOR 8080/8085
CONV86
ASSEMBLE FOR 8086/8088
EXECUTE ON 8080/8085
EQUIVALENT FUNCTION
EXECUTE ON 8086/8088

PORTING 8080/8085 SOURCE CODE TO THE 8086/8088

LINK86

Automatic combination of separately compiled or assembled 8086/8088 programs into a relocatable module

Automatic selection of required modules from specified libraries to satisfy symbolic references

Extensive debug symbol manipulation, allowing line numbers, local symbols, and public symbols to be purged and listed selectively

Automatic generation of a summary map giving results of the LINK86 process

Abbreviated control syntax

Relocatable modules may be merged into a single module suitable for inclusion in a library

Supports "incremental" linking

Supports type checking of public and external symbols

LINK86 combines object modules specified in the LINK86 input list into a single output module. LINK86 combines segments from the input modules according to the order in which the modules are listed.

Support for incremental linking is provided since an output module produced by LINK86 can be an input to another link. At each stage in the incremental linking process, unneeded public symbols may be purged.

LINK86 supports typechecking of public and external symbols reporting an error if their types are not consistent.

LINK86 will link any valid set of input modules without any controls. However, controls are available to control the output of diagnostic information in the LINK86 process and to control the content of the output module.

LINK86 allows the user to create a large program as the combination of several smaller, separately compiled modules. After development and debugging of these component modules the user can link them together, locate them using LOC86, and enter final testing with much of the work accomplished.

LOC86

Automatic and independent relocation of segments. Segments may be relocated to best match users memory configuration

Extensive debug symbol manipulation, allowing line numbers, local symbols, and public symbols to be purged and listed selectively

Automatic generation of a summary map giving starting address, segment addresses and lengths, and debug symbols and their addresses

Extensive capability to manipulate the order and placement of segments in 8086/8088 memory

Abbreviated control syntax

Relocatability allows the programmer to code programs or sections of programs without having to know the final arrangement of the object code in memory.

LOC86 converts relative addresses in an input module to absolute addresses. LOC86 orders the segments in the input module and assigns absolute addresses to the segments. The sequence in which the segments in the input module are assigned absolute addresses is determined by their order in the input module and the controls supplied with the command.

LOC86 will relocate any valid input module without any controls. However, controls are available to control the output of diagnostic information in the LOC86 process, to control the content of the output module, or both.

The program you are developing will almost certainly use some mix of random access memory (RAM), read-only memory (ROM), and/or programmable read-only memory (PROM). Therefore, the location of your program affects both cost and performance in your application. The relocation feature allows you to develop your program on the Intellec development system and then simply relocate the object code to suit your application.

OH86

Converts an 8086/8088 absolute object module to symbolic hexadecimal format

Facilitates preparing a file for later loading by a symbolic hexadecimal loader, such as the iSBC Monitor or Universal PROM Mapper

Converts an absolute module to a more readable format that can be displayed on a CRT or printed for debugging

The OH86 command converts an 8086/8088 absolute object module to the hexadecimal format. This conversion may be necessary to format a module for later loading by a hexadecimal loader such as the iSBC 86/12 monitor or Universal Prom Mapper. The conversion may also be made to put the module in a more readable format that can be displayed or printed.

The module to be converted must be in absolute format; the output from LOC86 is in absolute format.

LIB86

LIB86 is a library manager program which allows you to:

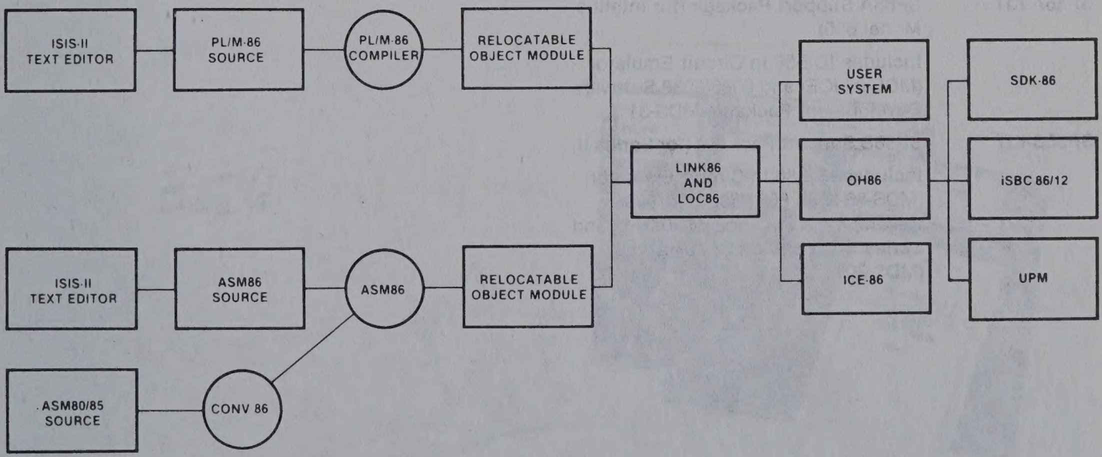
- **Create specially formatted files to contain libraries of object modules**
- **Maintain these libraries by adding or deleting modules**
- **Print a listing of the modules and public symbols in a library file**

Libraries can be used as input to LINK86 which will automatically link modules from the library that satisfy external references in the modules being linked

Abbreviated control syntax

Libraries aid in the job of building programs. The library manager program, LIB86, creates and maintains files containing object modules. The operation of LIB86 is controlled by commands to indicate which operation LIB86 is to perform. The commands are:

CREATE — creates an empty library file
ADD — adds object modules to a library file
DELETE — deletes modules from a library file
LIST — lists the module directory of library files
EXIT — terminates the LIB86 program and returns control to ISIS-II


ISIS-II TEXT EDITOR
PL/M-86 SOURCE
PL/M-86 COMPILER
RELOCATABLE OBJECT MODULE
ISIS-II TEXT EDITOR
ASM86 SOURCE
ASM86
RELOCATABLE OBJECT MODULE
ASM80/85 SOURCE
CONV 86
LINK86 AND LOC86
USER SYSTEM
OH86
ICE-86
SDK-86
iSBC 86/12
UPM

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec Microcomputer Development System

— MDS-800, MDS-888
— Series II
64K Bytes of RAM Memory

Dual Diskette Drives

— Single or Double* Density

System Console

— CRT or Hardcopy Interactive Device

Optional Hardware

Universal PROM Programmer
Line Printer*
ICE-86™*

Required Software

ISIS-II Diskette Operating System

— Single or Double* Density

*Recommended

Documentation Package

PL/M-86 Programming Manual (9800466)
ISIS-II PL/M-86 Compiler Operator's Manual (9800478)
MCS-86 User's Manual (9800722)
MCS-86 Software Development Utilities Operating Instructions for ISIS-II Users (9800639)
MCS-86 Macro Assembly Language Reference Manual (9800640)
MCS-86 Macro Assembler Operating Instructions for ISIS-II Users (9800641)
MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users (9800642)
Universal PROM Programmer User's Manual (9800819)

Flexible Diskettes

— Single and Double* Density

ORDERING INFORMATION

Part Number	Description
MDS-311	8086/8088 Software Development Package

Also available in the following development support packages:

Part Number	Description
SP86A-KIT	SP86A Support Package (for Intellec Model 800) Includes ICE-86 In-Circuit Emulator (MDS-86-ICE) and 8086/8088 Software Development Package (MDS-311)
SP86B-KIT	SP86B Support Package (for Series II) Includes ICE-86 In-Circuit Emulator (MDS-86-ICE), 8086/8088 Software Development Package (MDS-311), and Series II Expansion Chassis (MDS-201).

8089 ASSEMBLER SUPPORT PACKAGE

8089 I/O processor program generation on the Intellec Microcomputer Development System.

Relocatable object module compatible with the 8086 and 8088 Microprocessors.

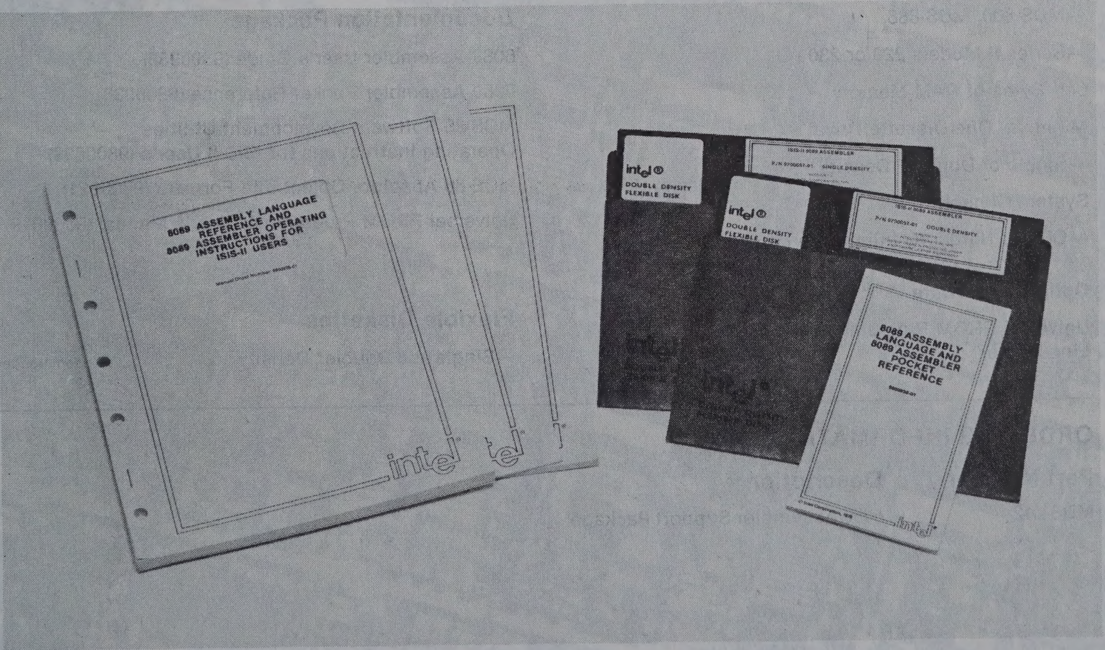
Supports 8089-based addressing modes with a structure facility that enables easy access to based data.

Fully detailed set of error messages.

Includes software development utilities to facilitate 8089 design.

- **—LINK86:** Combines 8086 or 8088 object modules with 8089 object modules and resolves external references.
- **—LOC86:** Assigns absolute memory addresses to 8089 object modules.
- **—OH86:** Converts 8086/8088/8089 object code to symbolic hexadecimal format.
- **—UPM86:** A PROM programming aid which has been updated to support PROM programming for 8086, 8088 and 8089 applications.

The 8089 Assembler Support Package extends Intellec microcomputer development system support to the 8089 I/O Processor. The assembler translates 8089 assembly language source instructions into appropriate machine operation codes. The 8089 Assembler Support Package allows the programmer to fully utilize the capabilities of the 8089 I/O Processor.


8089 ASSEMBLY LANGUAGE REFERENCE AND
8089 ASSEMBLER OPERATING INSTRUCTIONS FOR ISIS-II USERS
intel
DOUBLE DENSITY FLEXIBLE DISK
ISIS-II 8089 ASSEMBLER
SINGLE DENSITY
DOUBLE DENSITY
8089 ASSEMBLY LANGUAGE AND 8089 ASSEMBLER POCKET REFERENCE

8089 ASSEMBLER SUPPORT PACKAGE

FUNCTIONAL DESCRIPTION

The 8089 Assembler Support Package contains the 8089 assembler (ASM89) as well as LINK86 and LOC86—relocation and linkage utilities, OH86—8086/8088/8089 object code to hexadecimal converter, and UPM86—PROM programming software updated to program object code in the 8086 formats. ASM89 translates symbolic 8089 assembly language instructions into the appropriate machine operation codes. The ability to refer to program addresses with symbolic names eliminates the errors of hand translation and makes it easier to modify programs when adding or deleting instructions.

ASM89 provides relocatable object module compatibility with the 8086 and 8088 microprocessors. This object module compatibility, along with the 8086/8088 relocation and linkage utilities, facilitates the designing of the 8089 into an 8086 or 8088 system.

ASM89 fully supports the based addressing modes of the 8089. A structure facility in the assembler provides easy access to based data. The structure facility allows the user to define a template that enables accessing of based data symbolically.

A sample assembly listing is shown in table 1.

```
8089 ASSEMBLER                                                          PAGE    1

ISIS-II 8089 ASSEMBLER V1.0 ASSEMBLY OF MODULE CONSOL
OBJECT MODULE PLACED IN :F0:CONSOL.OBJ
ASSEMBLER INVOKED BY ASM89 CONSOL.SRC

0000                    1 CONSOLE  SEGMENT
                        2
                        3 ; INITIALIZE 8275 CRT AND 8279 KEYBOARD CONTROLLERS
                        4
                        5 CONTROL       STRUC
                        6   ; 8275 PORTS
0000                    7   PARA75:  DS   1               ; PARAMETER PORT
0001                    8   NULL01:  DS   1
0002                    9   STAT75:  DS   1               ; STATUS/COMMAND PORT
                       10
                       11   ; 8279 PORTS
0003                   12   NULL02:  DS   3
0006                   13   STAT79:  DS   1               ; STATUS/COMMAND PORT
0007                   14 CONTROL       ENDS
                       15
0000   1130 0040       16   MOVI  GA,4000H              ; SET PORT BASE ADDRESS
0004   0A4C 02 00      17   MOVBI [GA].STAT75,0         ; INITIALIZE 8275
0008   0A4C 00 4F      18   MOVBI [GA].PARA75,4FH
000C   0A4C 00 D3      19   MOVBI [GA].PARA75,0D3H
0010   0A4C 00 6A      20   MOVBI [GA] PARA75,6AH
0014   0A4C 00 19      21   MOVBI [GA].PARA75,19H
                       22
0018   0A4C 06 00      23   MOVBI [GA].STAT79,0         ; INITIALIZE 8279
001C   0A4C 06 30      24   MOVBI [GA].STAT79,30H
                       25
0020                   26 CONSOLE ENDS
                       27
                       28         END
8089 ASSEMBLER                                                          PAGE    2

SYMBOL TABLE
------------

 DEFN VALUE TYPE  NAME
----- ----- ----  ----

    1  0000  SYM  CONSOLE
    5  0000  STR  CONTROL
    8  0001  SYM  NULL01
   12  0003  SYM  NULL02
    7  0000  SYM  PARA75
    9  0002  SYM  STAT75
   13  0006  SYM  STAT79

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

Table 1. Sample 8089 Assembly Listing

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec Microcomputer Development System

—MDS-800, MDS-888

—Series II Models 220 or 230

64K Bytes of RAM Memory

Minimum One Diskette Drive

—Single or Double* Density

System Console

—CRT or Hardcopy Interactive Device

Optional Hardware

Universal PROM Programmer*
Line Printer*

Required Software

ISIS-II Diskette Operating System

—Single or Double* Density

Documentation Package

8089 Assembler User's Guide (9800938)

8089 Assembler Pocket Reference (9800936)

MCS-86 Software Development Utilities Operating Instructions for ISIS-II User's (9800639)

MCS-86 Absolute Object File Formats (9800821)

Universal PROM Programmer User's Manual (9800819)

Flexible Diskettes

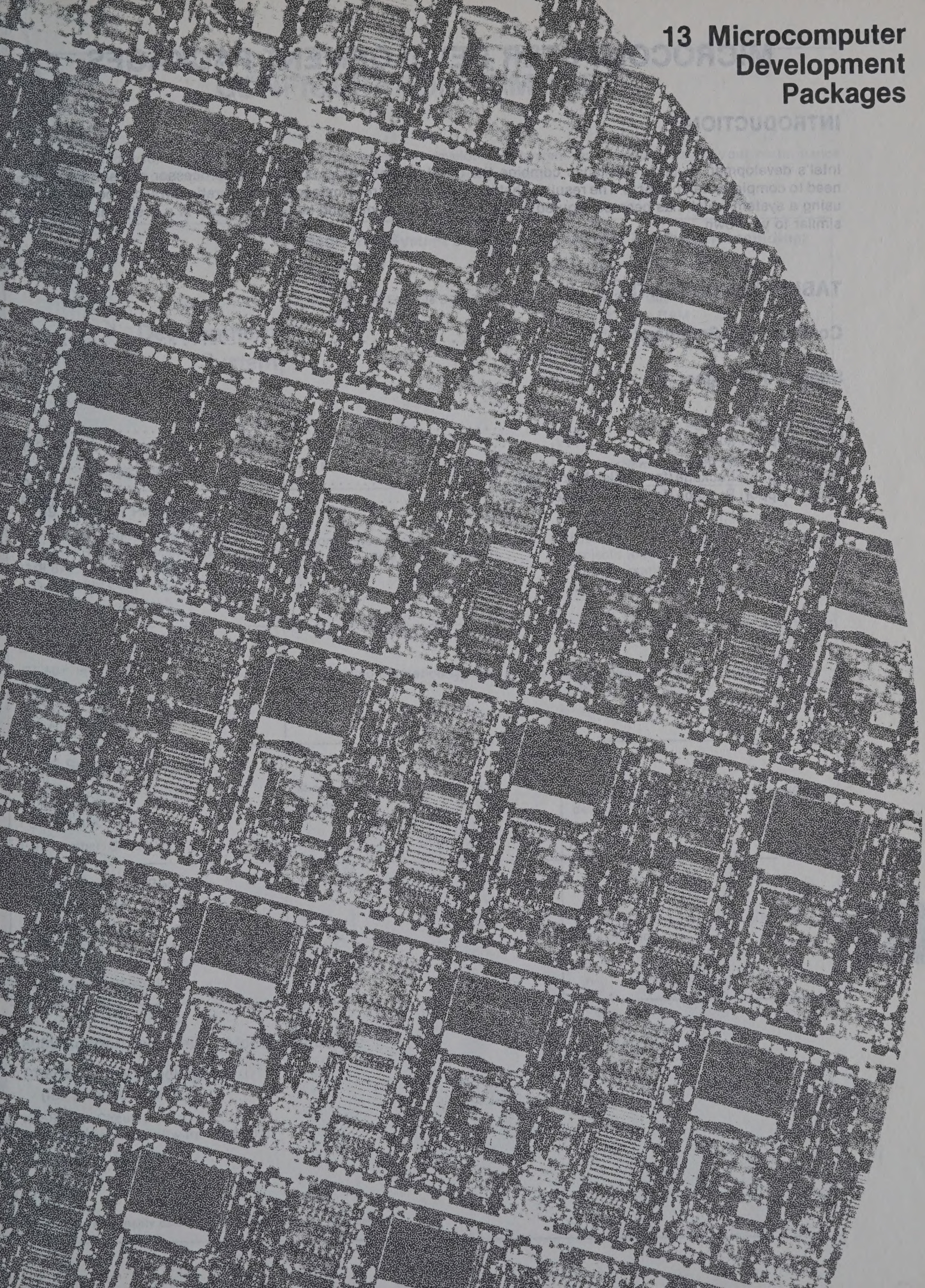
—Single and Double* Density

*Recommended

ORDERING INFORMATION:

Part Number	Description
MDS-312	8089 Assembler Support Package

13 Microcomputer Development Packages



MICROCOMPUTER DEVELOPMENT PACKAGES

INTRODUCTION

Intel's development support packages combine the development products that microprocessor system designers need to complete their projects. The result is that by using an Intel recommended configuration, you can be assured of using a system which has been configured for optimum performance and has been proven in a design environment similar to your own.

TABLE OF CONTENTS

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Support Packages

SP49 Support Package 13-4
SP80 Support Package 13-6
SP85 Support Package 13-8
SP86A Support Package (for Intellec Model 800) 13-10
SP86B Support Package (for Intellec Series II) 13-10

CONFIGURATION SUMMARY

For a complete development configuration, simply select the development system model (top) that fits your performance needs and the support package (left) for each of the microprocessors in your design.

Development System **Support Packages**	**Model 220 System Including:** Integral CRT Keyboard 250K Byte Flexible Disk Drive 32K Bytes RAM Part Number: MDS-220	**Model 230 System Including:** Integral CRT Keyboard 1M-Byte Dual Flexible Disk Drives 64K Bytes RAM PROM Programmer* Part Number: MDS-230
SP49 Support Package ICE-49™ In-Circuit Emulator MCS-48™ Software Support Package 8748/8741 Universal PROM Programmer Personality Card Part Number: SP49-KIT	Recommended configuration for 8048, 8049, 8035, 8039, 8748, and 8021 development.	Optional configuration for 8048, 8049, 8035, 8039, 8748, and 8021 development projects that can benefit from the added versatility and capacity of the dual double density disk drives.
SP80 Support Package ICE-80™ In-Circuit Emulator PL/M-80 Compiler FORTRAN-80 Compiler Part Number: SP80-KIT	Minimum configuration for 8080 development.	Recommended configuration for 8080 development.
SP85 Support Package ICE-85™ In-Circuit Emulator PL/M-80 Compiler FORTRAN-80 Compiler Part Number: SP85-KIT	Minimum configuration for 8085 development.	Recommended configuration for 8085 development.
SP86B Support Package (for Intellec® Series II) ICE-86™ In-Circuit Emulator 8086 Development Software (MDS-311) Series II Expansion Chassis (MDS-201) Part Number: SP86B-KIT		Required configuration for 8086 development.

8086 Support for Intellec Model 800 Users:

SP86A Support Package (for Intellec® 800)

ICE-86™ In-Circuit Emulator
8086 Development Software (MDS-311)

Part Number: SP86A-KIT

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*Requires a personality card for each EPROM type in your design.

SP49 SUPPORT PACKAGE

Development support for 8048, 8049, 8035, 8039, 8748 and 8021 including:

MCS-48 Software Support Package

ICE-49™ in-circuit emulator

8748/8741 Universal PROM Programmer personality card.

Flexible disk-based assembler provides conditional assembly and macro capability.

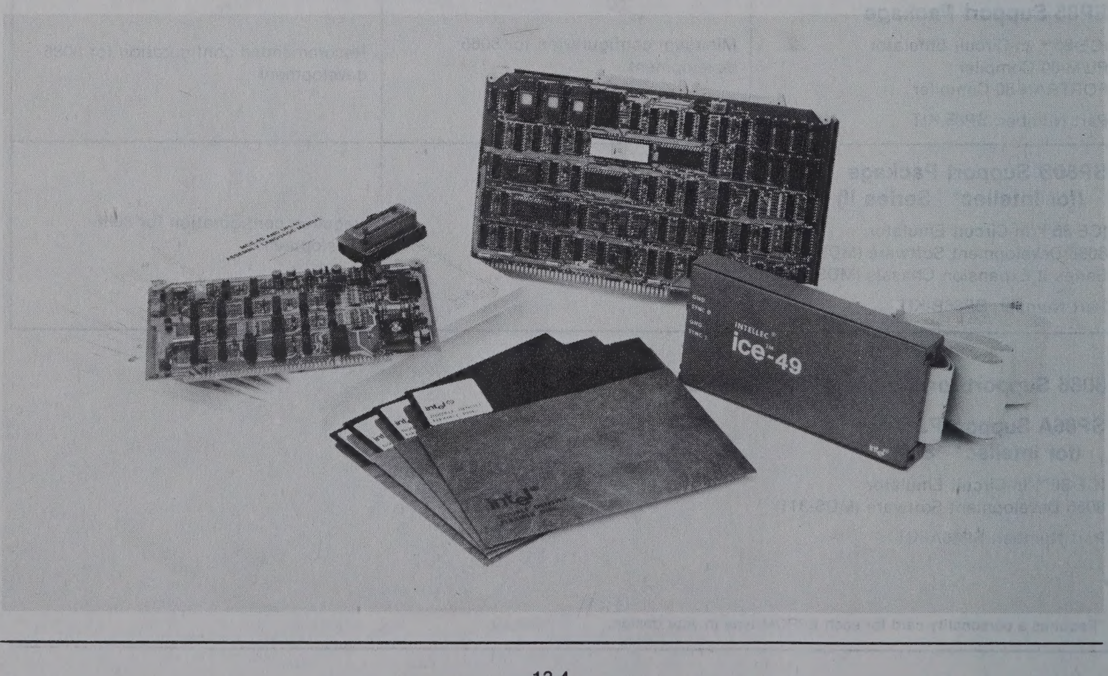
ICE-49™ module provides real-time emulation and instruction trace.

Full symbolic debugging for program labels or variables.

Software development begins using MCS-48 diskette-based software support which includes the MCS-48 assembler and the ISIS-II operating system for the Intellec® Microcomputer Development System. The assembler translates symbolic 8048/8049 assembly language instructions into the appropriate machine operation codes, and provides both conditional and macro assembler features. The output may be loaded to an in-circuit emulator module for software execution and debugging in the Intellec environment.

The ICE-49 module can also interface with the prototype system through a cable terminating in an MCS-48 pin-compatible plug which replaces the 8048 or 8049 device in the prototype. Powerful debug capability is extended into the MCS-48 system while ICE-49 debug hardware and software remain inside the Intellec system. With the ICE-49 plug in place, the designer can execute his program in real-time while collecting up to 255 instruction cycles of real-time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available within the ICE-49 module to emulate the MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags and I/O ports. Symbolic reference capability alows the designer to design and use symbols rather than absolute values when examining and modifying memory, registers, flags and I/O ports in this system.

Assembler output may also be programmed into an 8748 EPROM microcomputer using the Intel® Universal PROM Programmer and the UPP-848 personality card. This allows the reliable in-system verification of the design and a means of producing prototype products without waiting for a ROM programmed 8048.



SP49 SUPPORT PACKAGE SPECIFICATIONS

Hardware and Software Required

DS002 or DS003 System Package or Equivalent

System Clock

Crystal controlled 6.0 MHz internal, 3.0 MHz internal or user supplied TTL external; software selectable.

ICE-49 Electrical Characteristics

DC Power Requirements

V_{CC} = +5V ±5%
I_{CC} = 10A max; 7.0A typ
V_{DD} = +12V ±5%
I_{DD} = 79 mA max; 45 mA typ
V_{BB} = −10V ±5%
I_{BB} = 20 mA max

Input Impedance — @ ICE-49 user socket pins:
V_{IL} = 0.8V (max), I_{IL} = −1.6 mA,
V_{IH} = 2.0V (min), I_{IH} = 40 μA
For Bus:
V_{IL} = 0.8V (max), I_{IL} = −250 μA
V_{IH} = 2.0V (min), I_{IH} = 20 μA

Output Impedance — @ ICE-49 user socket pins:
P1, P2:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = V_{CC} (10K pullup)
For Bus:
V_{OL} = 0.5V (max), I_{OL} = 25 mA
V_{OH} = 2.4V (min), I_{OH} = −10 mA
Others:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = 2.4V (max), I_{OH} = −400 μA

Environmental Characteristics

Operating Temperature — 0°C to 40°C (Room Temperature)

Operating Humidity — Up to 95% relative humidity without condensation

Reference Manuals (supplied)

ICE-49 Operator's Manual **(9800632)**
MCS-48/UPI-141 Assembly Language Programming Manual **(9800255)**
MCS-48/UPI-41 Assembly Language Programming Manual **(9800255)**
Universal PROM Mapper Operator's Manual **(9800236)**
ISIS-II User's Guide **(9800306)**

ORDERING INFORMATION

Part Number	Description
SP49-KIT	SP49 Support Package. MCS-48 family support kit for 8048, 8049, 8035, 8039, 8748, 8021, and 8022 development. Includes ICE-49 in-circuit emulator (MDS-49-ICE) Software Support package (MDS-D48), and 8748/8741 personality card (UPP-848).

SP80 SUPPORT PACKAGE

Development support for 8080 microprocessor designs, including:

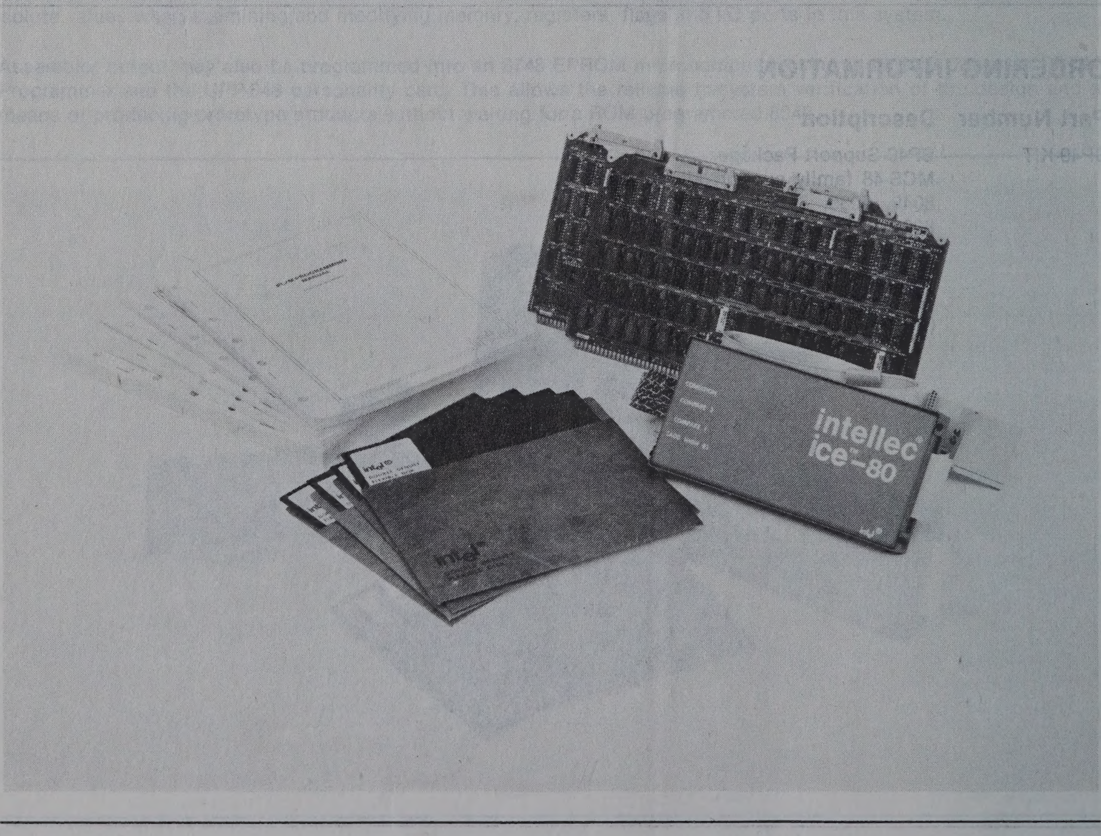
- **PL/M-80 structured high-level programming language compiler for system software development.**
- **ANS 77 FORTRAN-80 compiler for mathematically oriented software development.**
- **ICE-80™ in-circuit emulator**

Programs written in PL/M, FORTRAN, and assembly language can be linked together and relocated.

ICE-80 emulation connects Intellec® system resources to a user's prototype.

Full symbolic debugging is available for program labels or variables.

The SP80 Support Package combines the software and hardware components required for 8080 development using an Intellec Microcomputer Development system. The package includes an ICE-80 in-circuit emulator and the PL/M-80 and FORTRAN-80 high-level programming languages.



SP80 SUPPORT PACKAGE SPECIFICATIONS

Operating Environment

Required Hardware

DS002 System Package or equivalent is required

DS003 System Package is recommended

Emulation Clock

User's system clock or ICE-80 adaptor socket.

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$
$I_{CC} = 10A$ max; 7A typ
$V_{DD} = +12V \pm 5\%$
$I_{DD} = 80$ mA max; 45 mA typ
$V_{BB} = -10V \pm 5\%$
$I_{BB} = 1$ mA max; 1 μA typ

Environmental Characteristics

Operating Temperature — 0°to 40°C

Operating Humidity — Up to 95% relative humidity without condensation.

Reference Manuals (supplied)

FORTRAN-80 Programming Manual (9800481)
ISIS-II FORTRAN-80 Compiler Operator's Manual (9800480)
FORTRAN-80 Programming Reference Card (9800547)
PL/M-80 Programming Manual (980026)
ISIS-II PL/M-80 Compiler Operator's Manual (9800300)
ICE-80 Operator's Manual (9800185)

ORDERING INFORMATION

Part Number	Description
SP80-KIT	SP80 Support Package Includes ICE-80 In-circuit emulator (MDS-80-ICE), PL/M-80 High-Level Programming Language (MDS-PLM), and FORTRAN-80 Compiler (MDS-301)

SP85 SUPPORT PACKAGE

Development support for 8085 microprocessor designs, including:

- **PL/M-80 structured high-level programming language compiler for system software development.**
- **ANS 77 FORTRAN-80 compiler for mathematically oriented software development.**
- **ICE-85™ in-circuit emulator**

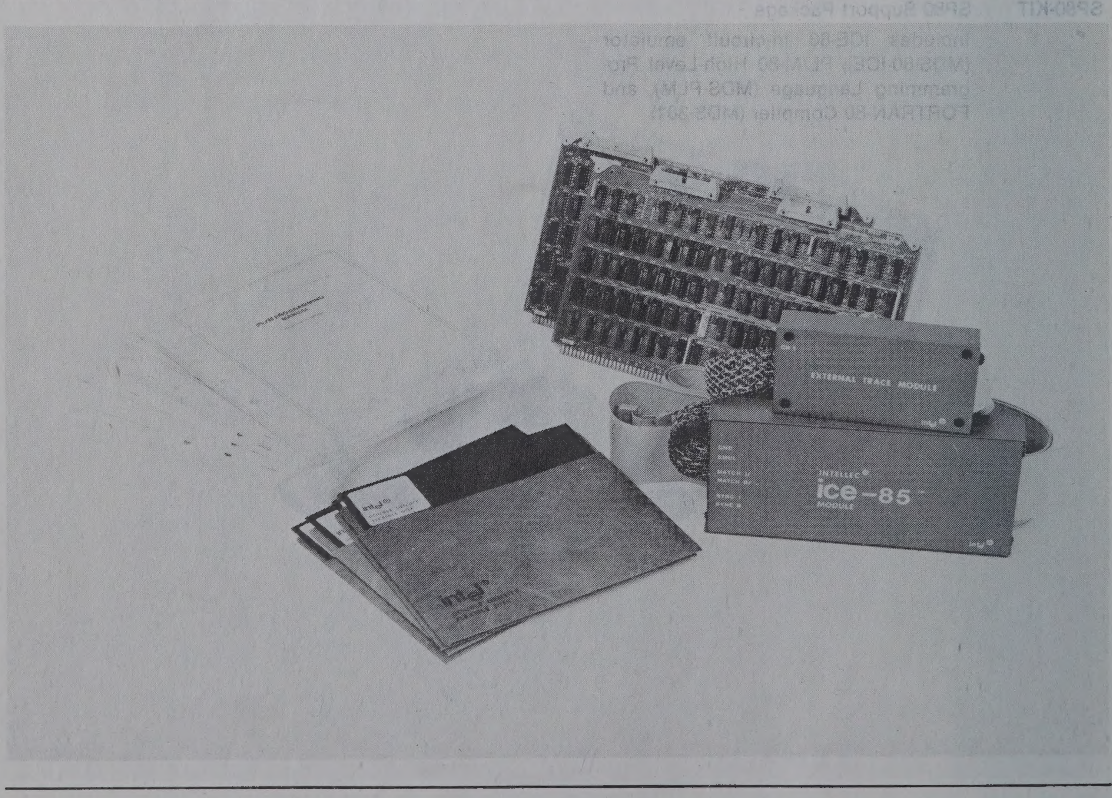
Programs written in PL/M, FORTRAN, and assembly language can be linked together and relocated.

ICE-85 emulation connects Intellec® system resources to a user's prototype.

Full symbolic debugging is available for program labels or variables.

External trace module extends emulation capability to prototype system peripheral activity.

The SP85 Support Package combines the software and hardware components required for 8085 development using an Intellec Microcomputer Development system. The package includes an ICE-85 in-circuit emulator and the PL/M-80 and FORTRAN-80 high-level programming languages.



SP85 SUPPORT PACKAGE SPECIFICATIONS

Operating Environment

Required Hardware

DS002 System Package or equivalent is required.

DS003 System Package is recommended.

Emulation Clock

User's system clock or ICE-85 adaptor socket (6.144 MHz crystal)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$
$I_{CC} = 12A$ max; 10A typ
$V_{DD} = +12V \pm 5\%$
$I_{DD} = 80$ mA max; 60 mA typ
$V_{BB} = -10V \pm 5\%$
$I_{BB} = 30$ mA max; 10 μA typ

Environmental Characteristics

Operating Temperature — 0°to 40°C

Operating Humidity — Up to 95% relative humidity without condensation.

Reference Manuals (supplied)

FORTRAN-80 Programming Manual (9800481)
ISIS-II FORTRAN-80 Compiler Operator's Manual (9800480)
FORTRAN-80 Programming Reference Card (9800547)
PL/M-80 Programming Manual (980026)
ISIS-II PL/M-80 Compiler Operator's Manual (9800300)
ICE-85 Operator's Manual (9800463)

ORDERING INFORMATION

Part Number	Description
SP85-KIT	SP85 Support Package Includes ICE-85 In-circuit emulator (MDS-85-ICE), PL/M-80 High-Level Programming Language (MDS-PLM), and FORTRAN-80 Compiler (MDS-301)

SP86A/SP86B SUPPORT PACKAGE

Full development support for 8086 microprocessor designs, including:

- **8086/8088 Software Development Package for high-level language or assembly language programming**
- **ICE-86 in-circuit emulation**
- **Expansion chassis for development support on Intellec® Series II Microcomputer Development System**

Programs written in PL/M and assembly language can be linked together and relocated.

Programs written in 8080/8085 assembly language can be converted to 8086/8088 assembly language.

ICE-86 emulation provides fully symbolic debugging for program labels or variables.

The SP86A and SP86B Support Packages combine the software and hardware components required for 8086 development using an Intellec Microcomputer Development System. The basic components are an 8086 Software Development Package and ICE-86 in-circuit emulator. The SP86B version of the kit includes an expansion chassis to provide additional board slots and power for the Intellec Series II.

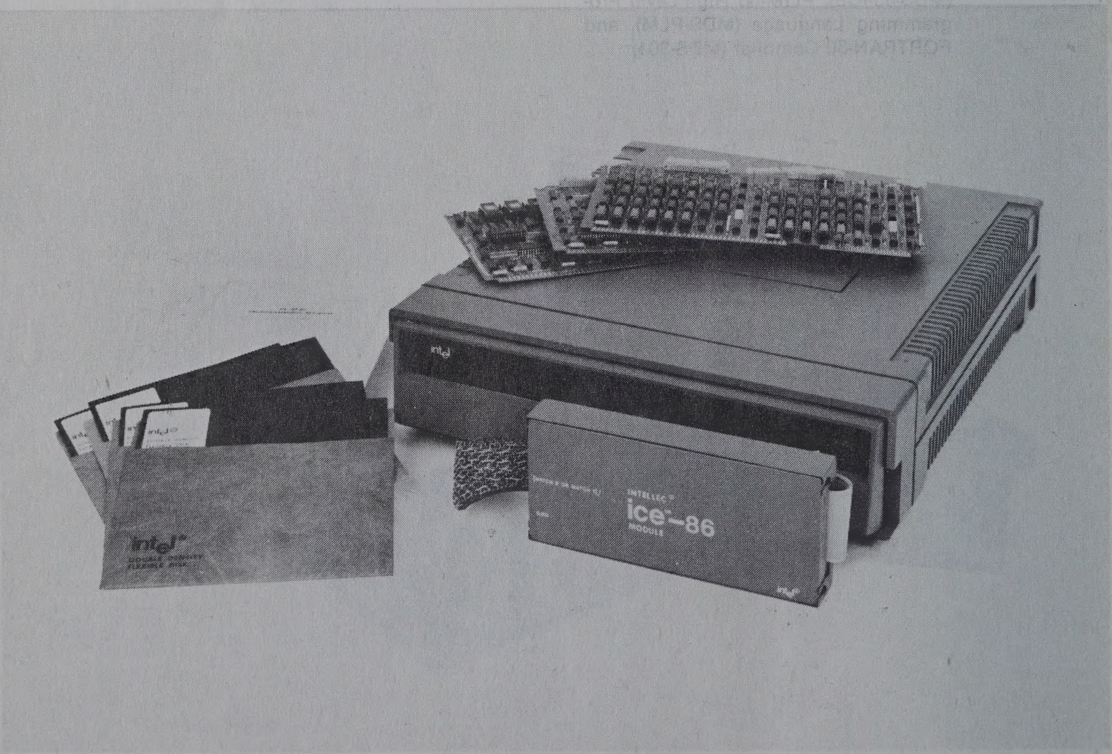


Figure 1. SP86B Support Package

SP86A AND SP86B SUPPORT PACKAGE SPECIFICATIONS

Operating Environment

Required Hardware

DS003 System Package or equivalent.

Environmental Characteristics

Operating Temperature: 0°C to 40°C

Operating Humidity: Up to 95% relative humidity without condensation.

Expansion Chassis Dimensions

Width — 17.37 in. (44.12 cm)
Height — 4.81 in. (17.22 cm)
Depth — 19.13 in. (48.59 cm)

Reference Manuals (supplied)

PL/M-86 Programming Manual (9800466)

ISIS-II PL/M-86 Compiler Operator's Manual (9800478)

MCS™-86 User's Manual (9800694)

MCS-86 Software Development Utilities Operating Instructions for ISIS-II Users (9800639)

MCS-86 Assembly Language Reference Manual (9800640)

MCS-86 Assembler Operating Instructions for ISIS-II Users (9800641)

MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users (9800642)

MCS-86 Absolute Object File Formats (9800821)

Universal PROM Programmer User's Manual (9800819A)

ICE-86 Operating Instructions (9800714A)

Electrical Characteristics

DC Power Supply

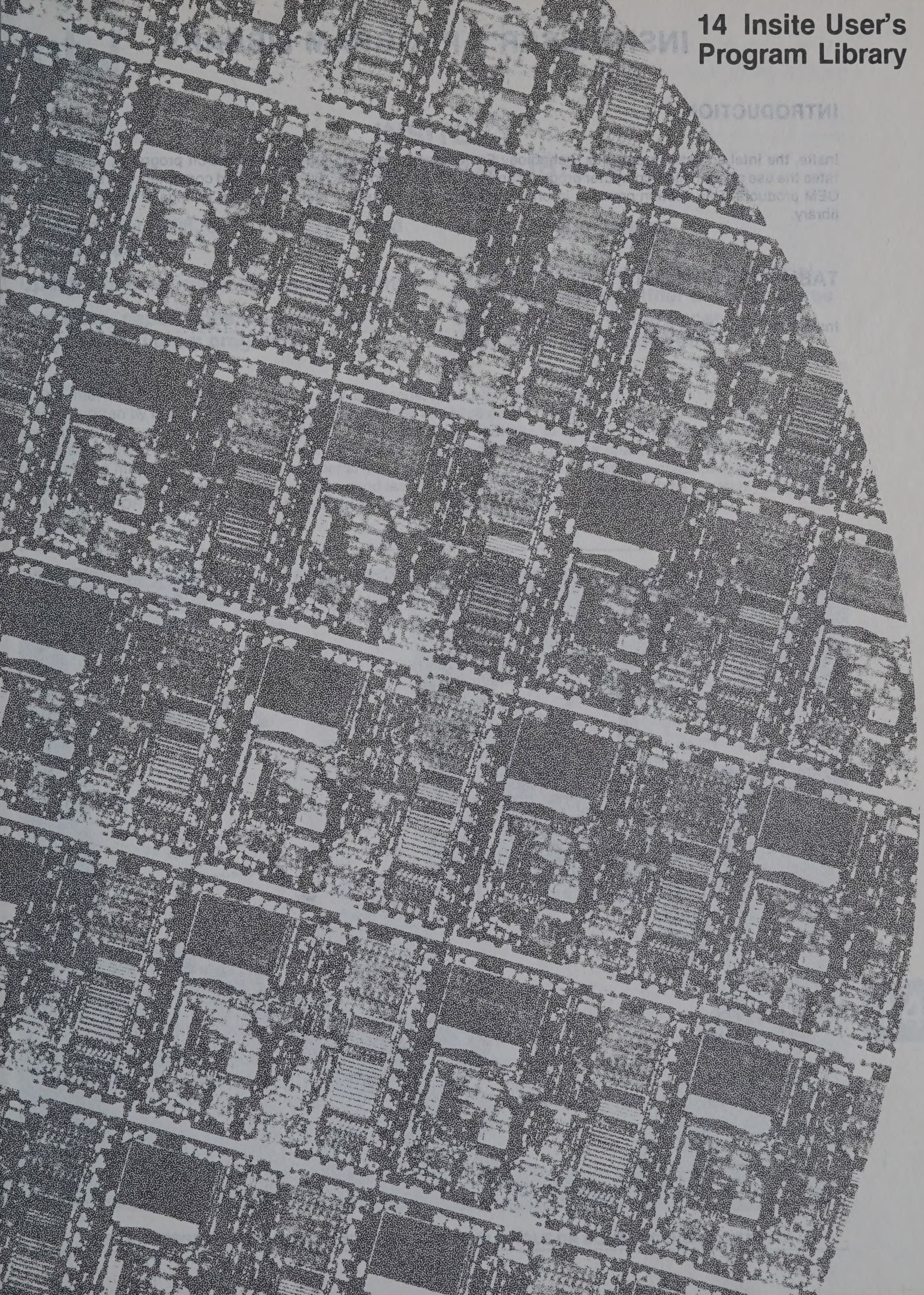
Voltage	Expansion Chassis Amps Supplied	ICE-86 In-Circuit Emulator Amps Required	
		Maximum	Typical
+5 +5% −4%	24	15	11
+12 ± 5%	2.0	0.12	0.08
−12 ± 5%	0.3	none	none
−10 ± 5%	1.0	0.015	0.012

AC Requirements — 50-60 Hz, 115/230 V_{AC}

ORDERING INFORMATION

Part Number	Description
SP86A-KIT	SP86A Support Package for Intellec Model 800 Includes ICE-86 In-Circuit Emulator (MDS-86-ICE) and 8086/8088 Software Development Package (MDS-311).
SP86B-KIT	SP86B Support Package for Intellec Series II Includes ICE-86 In-Circuit Emulator (MDS-86-ICE), 8086/8088 Software Development Package (MDS-311), and Series II Expansion Chassis (MDS-201).

14 Insite User's Program Library



INSITE USER'S PROGRAM LIBRARY

INTRODUCTION

Insite, the Intel software Index and Technology Exchange with almost 600 contributor 8-bit programs, further facilitates the use of Intel microcomputer products and the integration of iSBC 80 single board computers and systems into OEM products. This section provides information describing Insite and included partial listings of the 8-bit program library.

TABLE OF CONTENTS

Insite User's Program Library 14-3

INSITE™
USER'S PROGRAM LIBRARY

Programs for 8008, 8048, 8080, 8085 and 8086 processors

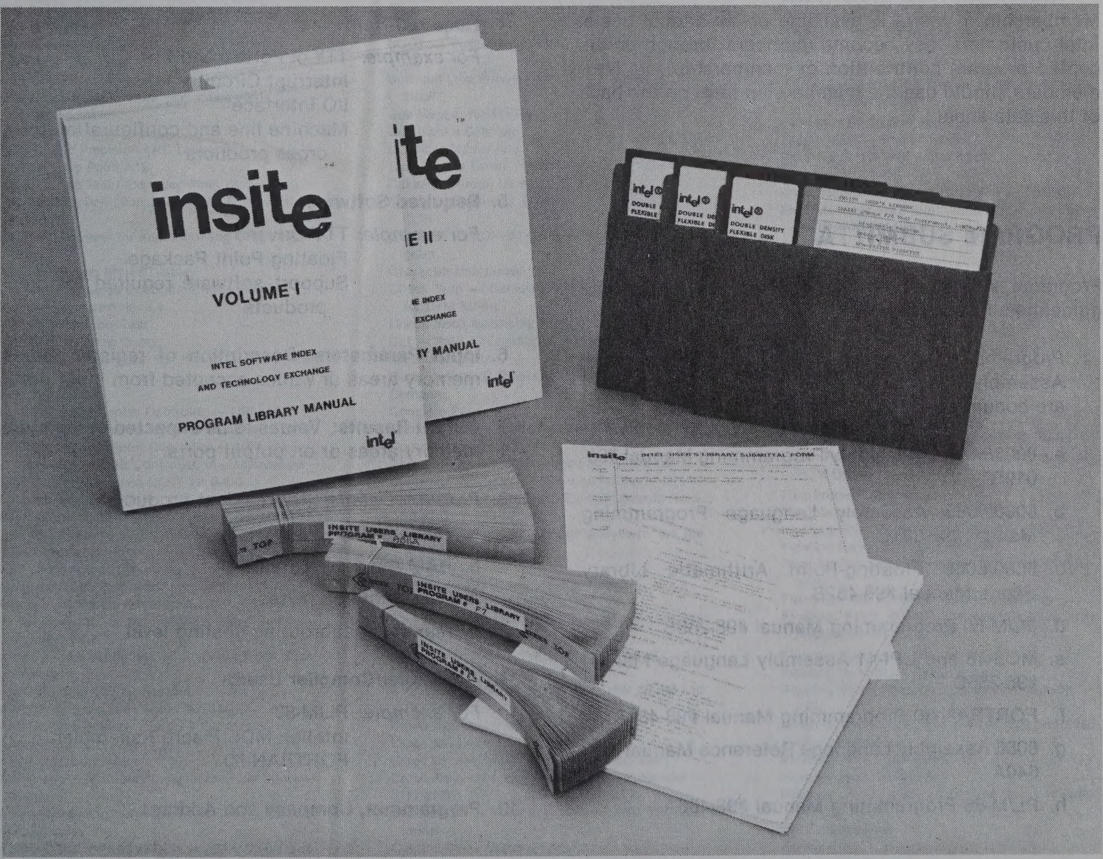
Updates of new programs sent bi-monthly

Diskettes, paper tapes, and listings available for library programs

Hundreds of programs

For each accepted program submittal, Insite$_e$ will provide either a one-year free membership, five free paper tapes, or three programs on diskette

Insite$_e$, Intel's Software Index and Technology Exchange, is a collection of programs, subroutines, procedures, and macros written by users of Intel's 8008, 8048, 8080, 8085 and 8086 microcomputers, iSBC-80 OEM computer systems, and Intellec® development systems. Thanks to customer contributions to Insite$_e$, Intel is able to make these programs available to all users of Intel microcomputers. By taking advantage of the availability of these general-purpose routines, the microcomputer design engineer and programmer can save many hours of programming and debugging time. The library of programs also serves as a good learning tool for those unfamiliar with Intel assembly language or PL/M-80 and FORTRAN-80, Intel's high-level languages for the 8008, 8080 and 8085 microcomputers.


insite
VOLUME I
INTEL SOFTWARE INDEX AND TECHNOLOGY EXCHANGE
PROGRAM LIBRARY MANUAL
intel
INSITE USERS LIBRARY PROGRAM
INSITE USERS LIBRARY SUBMITTAL FORM

LIBRARY PROGRAMS AVAILABLE ON PAPER TAPE AND SINGLE OR DOUBLE DENSITY DISKETTE

INSITE PROGRAM LIBRARY MANUAL

Each member will be sent the Program Library Manual consisting of an abstract for each program indicating the function of the routine, required hardware and software, and memory requirements.

User's Library members will be updated bi-monthly with abstracts of new programs submitted to Insit$_e$ during the subscription period. Please refer to the Intel OEM Price List or contact the nearest Regional Sales Office for yearly subscription fee.

PROGRAM LIBRARY SERVICES

PAPER TAPES, DISKETTES OR SOURCE LISTINGS are available for every program in Insit$_e$. Diskettes are available on single or double density.

MEMBERSHIP

Membership in Insit$_e$ is available on an annual basis. Intel customers may become members through an accepted program contribution or membership fee. New members should use the membership form on the back of this data sheet.

PROGRAM SUBMITTAL

Programs submitted for our review must follow the guidelines listed below:

1. Programs must be written in a standard Intel Assembly Language or PL/M-80. These languages are documented in the following manuals:
   a. 8008/MCS-8 Assembly Programming Manual #98-019B
   b. 8080/8085 Assembly Language Programming Manual #98-301C
   c. 8080/8085 Floating-Point Arithmetic Library User's Manual #98-452B
   d. PL/M-80 Programming Manual #98-268B
   e. MCS-48 and UPI-41 Assembly Language Manual #98-255C
   f. FORTRAN-80 Programming Manual #98-481A
   g. 8086 Assembly Language Reference Manual #98-640A
   h. PL/M-86 Programming Manual #98-466A
2. A source listing of the program must be included. This must be the output listing of a compile or assembly. All accepted programs must be capable of compilation or assembly by Intel standard compilers or assemblers. No consideration will be given to partial programs or duplication of existing programs.
3. A test program which assures the validity of the contributed program must be included. This must show the correct operation of the program.
4. A source paper tape or diskette of the contributed program is required. This will be used for the reproduction of tapes for other members.

Complete the Submittal Form as follows: (please type or print)

1. **Processor** (check appropriate box).
2. **Program Title:** Name and brief description of program function.
3. **Function:** Detailed description of operations performed by the program. Attach additional pages if necessary.
4. **Required Hardware:**

   For example: TTY or Ports 0 and 1
   Interrupt Circuitry
   I/O Interface
   Machine line and configuration for cross products
5. **Required Software:**

   For example: TTY Driver
   Floating Point Package
   Support software required for cross products
6. **Input Parameters:** Description of register values, memory areas or values accepted from input ports.
7. **Output Results:** Values to be expected in registers, memory areas or on output ports.
8. *Program Details:* (for resident products only)
   a. Register modified
   b. RAM required (bytes)
   c. ROM required (bytes)
   d. Maximum subroutine nesting level
9. **Assembler/Compiler Used:**

   For example: PL/M-80
   Intellec MDS Macro Assembler
   FORTRAN-80
10. **Programmer, Company and Address.**

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3M — DCD1 Cassette Tape Drive Monitor Routines
5 Level (BAUDOT) to 8 Level (ASCII) Paper Tape Conversion
8-Bit Multiply and Divide
8-Bit Random Number Generator
8-Digit LED Display Controller — UPI-41
12 × 12 Multiply
16-Bit CRC for Polynomial X16 + X12 + X5 + 1
16-Bit Division — 16-Bit Result
16-Bit Division — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 32-Bit Result
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16-Bit Square Root Routine
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4040 Cross Assembler for Intellec 8/MOD80 and MDS-800
8008 Cross Assembler for 8085-MACRO Definition — M8008 SRC
8008 Cross Inverse Assembler for HP2100
8008 Disassembler
8008 Macro Assembler Version 2.0
8008 Macro Definition Set for Assembly on PDP-11
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8048-DIV — Division Routine
8048-Seven Segment Display Interface Subroutines — Scan
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8048 Tune Generator
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8080 Cross Assembler for Tektronics 4051
8080 Disassembler
8080 Disassembler
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8080 Floating Point A*B
8080 Floating Point Extended Math Package
8080 Floating Point Package with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
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Algebraic Compare Subroutine
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AP29 "Using the 8085 Serial I/O Lines"
APL Graphic Display on a 5 × 7 Dot Matrix
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Arithmetic — Multiple Precision for PL/M Conventions
Array Addressing Subroutine and Calling Macro
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Basic Interpreter, LLL/Chernack
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BCD To/From Binary Conversion
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BCD Up/Down Counter
Bin to BCD Conversion Routine
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Block — Large Hex File into PROM Length Blocks Converter
BOOT — Bootstrap Loading and Program Patching
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Calendar Subroutine
Card Reader Driver, Hollerith to ASCII Conversion
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CERROR — PL/M-80 Compiler Error Display Program
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Flexible Name List Manager
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Hewlett Packard Calculator to MDS800 I/O Control Program — HPIO
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HEX-File Format to OBJ.-File Format with Symbol Table — HEXSYM
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HEX to Decimal Conversion
HEX File into PROM Length Blocks Converter — Block
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I8080 Cross Assembler for Intel 8080/8085 Microprocessors
IBM Selectric Input Program
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I-Command — Insert Data in HEX Form from TTY into RAM
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K, Program Trap and Dump Routine
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PROMPT48 Interactive Controller — REMOTE48

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SMPY16: 16-Bit 2's Complement Signed Multiplication
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Stage2
Statement Counter
Step
String Manipulation Package
Structured Assembler for 8080

insite™ INTEL® USER'S LIBRARY SUBMITTAL FORM

☐ 8008 ☐ 8048 ☐ 8080/8085 ☐ 8086 ☐ Other ____________________ (Use additional sheets if necessary)

Program Title

Function

Required Hardware

Required Software

Input arameters

Output Results

Registers Modified:	Programmer:
RAM Required:	Company:
ROM Required:	Address:
Maximum Subroutine Nesting Level:	City:
Assembler/Compiler Used:	State:

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Symbol Table Inserter for AB22
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Tally R2050 HSPTR Driver
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Tape Labeler for MDS
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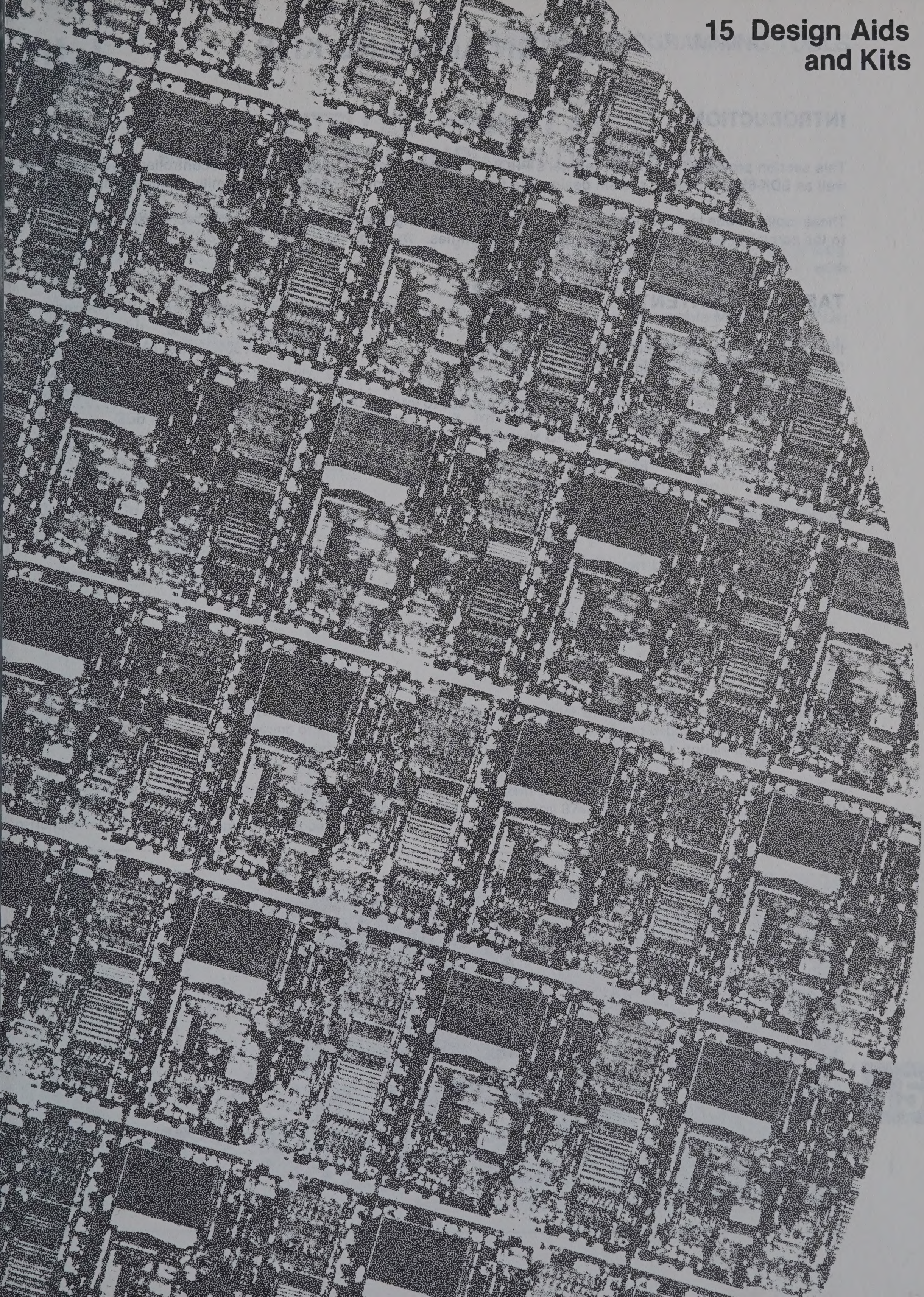
Terminet 300
Terminet 1200
Text Editor, Enhanced MDS, X111
Text Editor
Text Processor
Text Storage Program
Thermocouple Linearization (Type J)
Thumbwheel SBC 80/10 Test Program
Tic-Tac-Toe
Tic-Tac-Toe (3 Dimensional)
Time Sharing Communications
TIMIT — Interrupt Driven Real Time Clock Routine
T.I. Silent 700 Interface — Intellec MDS
T.I. Silent 700 SBC 80 Monitor Interface
TRACE — Program Trace and Debugger
Trace & Register Print Out
Trace Routine
Trace Version 7.0
Transformation Routine for Coordinate Digits from EID into X-Y Coordinates of CRT (EID-CALMA)
TTY Binary Dump Routine
TTY Binary Load Routine
TTY Diagnostic
Type
Type — List File on Console by Page
Type K.T.C. Linearizer
UPI-41 8-Digit LED Display Controller
UPI-41 LRC Printer Controller
UPI-41 — Olivetti 20-Column Printer Controller
UPI-41A — 8278 Keyboard/Display Controller
UPI-41A Combination I/O Device
UPI-41H Sensor Matrix Controller
UPP-41A — 8295 Dot Matrix Printer Controller
Utility Macros for 8080
VDU Darts
Video Driver
Wipe — File Deleter
Word Game, The
WRITEP — Output Procedures for PL/M-80
WRMIN — RMX Minimal Terminal Output

15 Design Aids and Kits



DESIGN AIDS AND KITS

INTRODUCTION

This section provides information in Intel's PROMPT 48 design aid for single chip microcontroller development, as well as SDK-85 and SDK-86 system design kits for use in prototyping 8085 and 8086 family designs, respectively.

These tools provide low cost methods of building, programming, testing and evaluating microprocessor designs prior to the committment to complete development capabilities.

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SDK-85 MCS-85 System Design Kit 15-8
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SDK-C86 System Design Kit Software and Cable Interface to Intellec Development System 15-20

INTELLEC® PROMPT 48™ MCS-48™ MICROCOMPUTER DESIGN AID

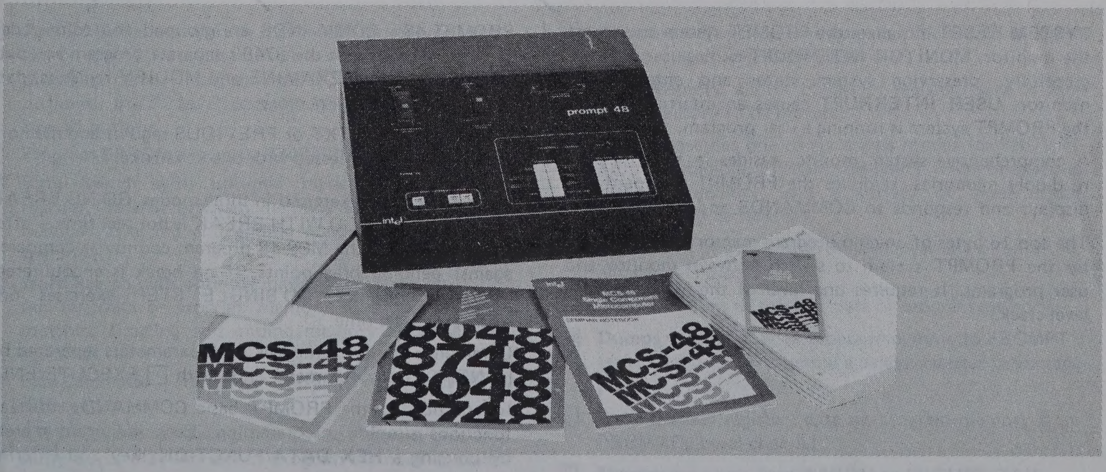
- Complete Design Aid and EPROM Programmer for revolutionary MCS-48™ Single Component Computers including:

CPUs	8-bit MCS-48™: 8748, 8035
Program Memory	1K byte erasable, reprogrammable on-chip (8748), expandable. 1K byte RAM in PROMPT™ system.
Register Memory	64 bytes RAM on-chip, expandable
Data Memory	256 bytes RAM in PROMPT™ system, expandable
I/O	27 TTL compatible I/O lines on-chip, expandable
Control	On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack
Power	Single +5 VDC system

- Low Cost
- Simplifies microcomputing — enter, run, debug, and save machine language programs with calculator-like ease
- Complete with two removable MCS-48™ CPUs:
  - 8748 CPU with erasable, reprogrammable program memory on-chip
  - 8035 CPU program memory is off-chip
- Integral keyboard and displays (no teletypewriter or CRT terminal required)
- Extensive PROMPT 48™ monitor allows system I/O, bus and memory expansion
- Intellec® Microcomputer Development System compatible
- Comprehensive Design Library

Intellec PROMPT 48 is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

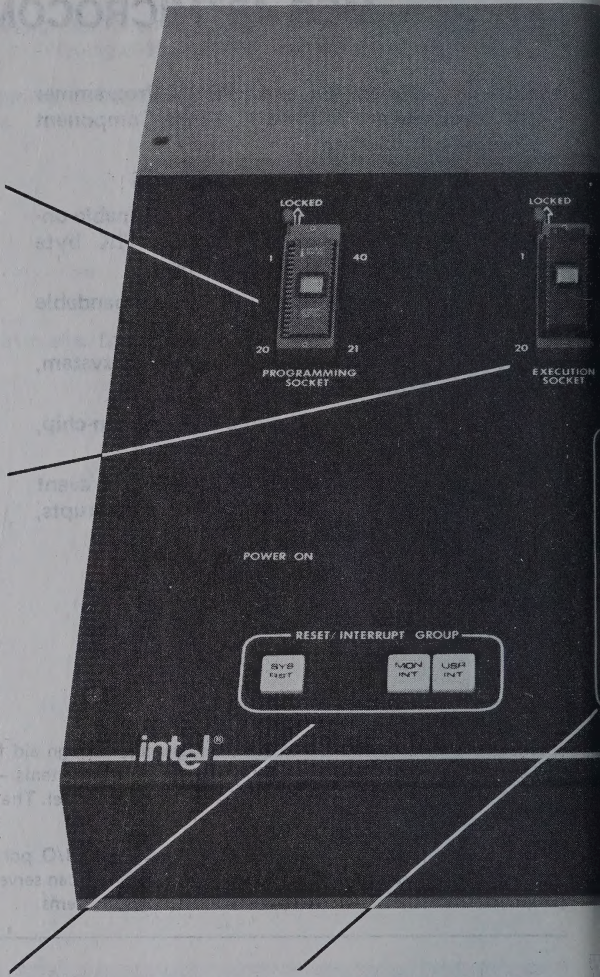
PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1k bytes provided internally. PROMPT 48 can serve as an economical 8748 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.



The 8748 is the first microcomputer fully integrated on one component. All elements of a computing system are provided, including CPU, RAM, I/O, timer, interrupts and erasable, reprogrammable non-volatile program memory. PROMPT's **PROGRAMMING SOCKET** programs this revolutionary "smart PROM" — the 8748 — in a highly reliable, convenient manner. A fail-safe interlock ensures the device is properly inserted before applying programming pulses. Each location may be individually programmed, one byte at a time. A read-before-write programming algorithm prevents device damage by inadvertently programming unerased memory.

The **EXECUTION SOCKET** accepts an 8035 or an 8748. Both are supplied with each PROMPT 48, and either can serve as heart of the PROMPT system. There are no processors within the PROMPT 48 mainframe, which instead contains monitor ROM and RAM, user RAM, peripherals, drivers, and sophisticated control circuitry.

Once a processor is seated in the execution socket and power is applied the PROMPT system comes to life. One can select various access modes such as program execution from PROMPT system RAM, or from on-chip PROM. Thus programs can first be executed from PROMPT RAM with the 8035 processor. When debugging is complete, the 8035 (execution socket) processor can program the 8748 (programming socket) processor. Finally, a programmed 8748 processor can be exercised by itself from the execution socket. The execution socket processor runs either monitor or user programs.



SYSTEM RESET initializes the PROMPT system and enters the monitor. **MONITOR INTERRUPT** exits a user program gracefully, preserving system status and entering the monitor. **USER INTERRUPT** causes an interrupt only if the PROMPT system is running a user program.

A comprehensive system monitor resides in four 1K byte read-only memories. It drives the PROMPT keyboard and displays and responds to COMMANDS and FUNCTIONS.

The top 16 bytes of on-chip program memory must be used by the PROMPT system to switch between monitor and user programs. It requires one level of the MCS-48 eight-level stack.

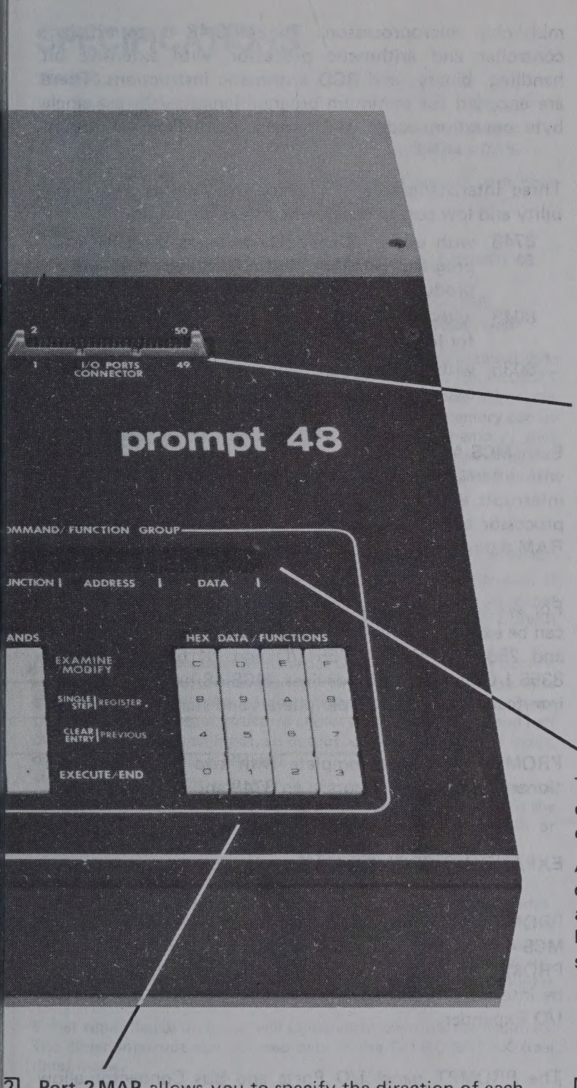
PROMPT 48's **COMMANDS** are grouped and color-coded to simplify access to the 8748's separate program and data memory. You can EXAMINE and MODIFY registers, data memory or program memory.

Then either the NEXT or PREVIOUS register and memory locations can be accessed with one keystroke.

Programs can be exercised in three modes. GO NO BREAK runs in real time. GO WITH BREAK is not real time — after each instruction the MCS-48 program counter is compared against pending breakpoints. If no break is encountered, execution resumes. GO SINGLE STEP exercises one instruction at a time.

Commands are like sentences, with parameters separated by [,] NEXT. Each command ends with [.] EXECUTE/END.

In addition to the PROMPT basic COMMANDs, thirteen functions simplify programming. Each is started merely by pressing a **HEX DATA/FUNCTIONs** key and entering parameters as required.



An optional cable, PROMPT-SER, directly connects the PROMPT system to virtually any terminal via a rear access slot. Another cable, PROMPT-SPP, allows programs and data to be downloaded from the Intellec Microcomputer Development System to the PROMPT system for debugging.

You enjoy easy access to the pins of the executing processor via this **I/O PORTS and BUS CONNECTOR**. Only the EA external access, SS single step and X1, X2 clock inputs are reserved for the PROMPT system.

Thus program or data memory may be expanded beyond that provided on-chip or in the PROMPT system. I/O ports can be expanded, as with the 8243, or peripheral controllers can be memory-mapped. The I/O ports and Bus connector allows the execution socket processor to be directly interfaced to your prototype system, yet be controlled from the PROMPT panel.

The **COMMAND/FUNCTION GROUP** panel keyboard and displays completely control PROMPT 48 — a teletypewriter or CRT terminal is not needed.

A hyphen prompting character appears whenever a command or function can be entered. Addresses and data are shown whenever EXAMINing registers and memory. Parameters for COMMANDs and FUNCTIONs are also shown.

2 **Port 2 MAP** allows you to specify the direction of each pin on port 2. Port 2 is multiplexed to address external program memory and expand I/O. Thus it must be buffered; the P2 MAP command establishes the direction of buffering.

3 **Program EPROM** programs 8748 EPROMs.

4 **Byte Search with optional mask** sweeps through register, data or program memory searching for byte matches. Starting and ending memory addresses are specified.

5 **Word Search with optional mask** sweeps through register, data or program memory searching for word matches. Starting and ending memory addresses are specified.

6 **Hex Calculator** computes hexadecimal sums and differences.

7 **8748 Program for Debug** is similar to Program EPROM, but ensures that the top of program memory contains monitor reentry code for debugging.

8 **Compare** will verify any portion of EPROM program memory against PROMPT memory.

9 **Move Memory** allows blocks of register, data or program memory to be moved.

A **Access** specifies one of six access modes for PROMPT 48. For example, EPROM, PROMPT RAM or external program memory, and a variety of input/output options may be selected.

B **Breakpoint** allows you to set and clear any or all of the eight breakpoints.

C **Clears** portions of register, data or program memory.

D **Dumps** register, data, or program memory to PROMPT's serial channel, for example a teletypewriter paper tape punch.

E **Enter** (reads) register, data or program memory from PROMPT's serial channel.

F **Fetches** programs from EPROM to PROMPT RAM.

PROMPT 48^{TM} SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 48 simplifies the programming of MCS-48 systems. Like the 8748 it is radically new, highly integrated, and expandable. Like the MCS-48 family, it is low cost, and ideal for small applications and programs. It is a design aid, not a development system with sophisticated software and peripherals.

"PROMPT" stands for PROgraMming Tool. It is a programmer for 8748 EPROMs, and a versatile aid for debugging MCS-48 programs. Programs can be entered via its integral panel keyboard, programming socket, or serial channel. Almost any terminal can be interfaced to the serial channel, including a teletypewriter, CRT, or the Intellec Microcomputer Development System.

Programs, written first in assembly language, are entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Most MCS-48 operations can be specified with only two keystrokes.

Once entered, routines can be exercised one instruction (single step) or many instructions at a time. The principal MCS-48 register — the accumulator — is displayed while single-stepping. Programs can be executed in real-time (GO NO BREAK) or with as many as eight different breakpoints (GO WITH BREAK).

PROMPT 48 is a complete, fully assembled and powered microcomputer system including program memory, data memory, I/O and system monitor beyond that available on MCS-48 single component computers. 1K bytes of PROMPT system RAM serve as "writable program memory" — a ROM simulator for the program memory on each MCS-48 computer. 256 bytes of PROMPT system RAM serve as "external data memory," beyond the 64 register bytes on each MCS-48 computer. Users may further expand program or data memory via the panel I/O PORTS and BUS CONNECTOR.

The PROMPT 48 manual includes chapters for the reader with little or no programming experience. Topics treated range from number systems to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPs — simplify microcomputer concepts.

PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles and application notes, make the Intellec PROMPT 48 ideal for the newcomer to microcomputing.

THE REVOLUTIONARY MCS 48^{TM} SINGLE COMPONENT COMPUTER

Advances in n-channel MOS technology allow Intel, for the first time, to integrate into one 40-pin component all computer functions:

8-bit CPU
1K x 8-bit EPROM/ROM Program Memory
64 x 8-bit RAM Data Memory
27 Input/Output Lines
8-bit Timer/Event Counter

More than 90 instructions — each one or two cycles — make the single chip MCS-48 equal in performance to most multi-chip microprocessors. The MCS-48 is an efficient controller and arithmetic processor, with extensive bit handling, binary, and BCD arithmetic instructions. These are encoded for minimum program length: 70% are single byte operation codes, and none is more than two bytes.

Three interchangeable, pin-compatible devices offer flexibility and low cost in development and production:

8748	with user-programmable and erasable EPROM program memory for prototype and pre-production systems
8048	with factory-programmed mask ROM memory for low-cost, high volume production
8035	without program memory, for use with external program memories

Each MCS-48 processor operates on a single +5V supply, with internal oscillator and clock driver, and circuitry for interrupts and resets. Extra circuitry is in the 8048 ROM processor to allow low power standby operation: the 64 x 8 RAM data memory can be independently powered.

For systems requiring additional compatibility, the MCS-48 can be expanded with the new 8243 I/O expander, 8155 I/O and 256 byte RAM, 8755 I/O and 2K byte EPROM or 8355 I/O and 2K ROM devices. MCS-48 processors readily interface to MCS-80/85 peripherals and standard memories.

PROMPT 48 comes complete with two of these revolutionary MCS-48 processors — an 8748 and an 8035.

EXPANDING PROMPT 48^{TM}

PROMPT 48 may be expanded beyond the resources on the MCS-48 single component computer and those in the PROMPT system. External program and data memory may be interfaced and input/output ports added with the 8243 I/O Expander.

The PROMPT panel I/O Ports and Bus Connector allow easy access to all MCS-48 pins except those reserved for control by the PROMPT system, namely EA external access, SS single step, and X1, X2 clock inputs.

A Specialized PROM Programmer Kit, the PROMPT-SPP, allows PROMPT 48 to serve as an economical 8748 Specialized PROM Programmer peripheral in Intellec 800 Microcomputer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec 800 Microcomputer Development System.

PROMPT 48 can be fully controlled either by the panel keyboard and displays, or remotely by a serial channel. Thus a teletypewriter or CRT can be used but neither is required. Full remote control by a serial channel means users can download and debug programs using the PROMPT 48 together with an Intellec 800 Microcomputer Development System.

SPECIFICATIONS

TIMING

Basic Instruction	5 μsec
Cycle Time	$t_{CY} = 5\ \mu$sec
Clock	3 MHz ± 0.1%

Any PROMPT 48 system can be modified to operate with basic instruction and $t_{CY} = 2.5\ \mu$sec, 6 MHz clock.

MEMORY BYTES

	Maximum	On Chip	In PROMPT 48
Register	64	64	0
Data	3328	0	256
Program	4096	1024 EPROM	1024 RAM

The 8748 contains 64 bytes of register memory, no external data memory, and 1024 bytes of EPROM program memory. The PROMPT system provides 256 bytes of external data memory, and 1024 bytes of RAM program memory. PROMPT RAM program memory can be used in place of the On-Chip EPROM program memory; thus programs less than 1024 bytes may be designed. For larger programs additional memory can be directly interfaced to the MCS-48 bus via the PROMPT panel I/O Ports and Bus Connector.

I/O PORTS

All MCS-48 I/O Ports are accessible on the PROMPT panel connector.

BUS is a true bidirectional 8-bit port with associated strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or a non-latching input port. Input and output lines cannot be mixed.

PORTS 1 AND 2 are each 8 bits wide. Data written to these ports is latched and remains unchanged until written. As inputs these lines are not latching. The lines of ports 1 and 2 are called quasibidirectional. A special output structure allows each line of port 1 and half of port 2 to serve as an input, an output, or both. Any mix of input, output, and both lines is allowed.

Three pins — T0, T1 and INT — can serve as inputs; T0 can be designated as a clock output. Input/Output can be expanded via the PROMPT panel connector with a special I/O expander (8243) or standard peripherals.

RESET and INTERRUPTS

RESET initializes the PROMPT system and enters the monitor. MONITOR INTERRUPT exits a user program gracefully, preserving system status and entering the monitor. USER INTERRUPT causes an interrupt only if the PROMPT system is running a user program. The processor traps to location 3_{16}. The MCS-48 timer/event counter is not used by the PROMPT system and is available to the user.

Either timer flag or interrupt will signal when overflow has occurred. The timer interrupt can be used only in the GO NO BREAK (real time) mode.

EPROM PROGRAMMING

PROMPT 48 provides a programming socket to directly program 8748s. Programs are loaded into the PROMPT RAM program memory via keyboard, EPROM, teletypewriter, or other serial interface.

A fail-safe interlock ensures programming pulses are applied only if the device is properly inserted. Inadvertent reprogramming is prevented by a read-before-write programming algorithm. Each location may be individually programmed, one byte at a time.

PANEL I/O PORTS and BUS CONNECTORS

All MCS-48 pins, except five, are accessible on the I/O Ports and Bus Connector. The five reserved for PROMPT system control are EA external access, SS single step, X1, X2 crystal inputs, and 5 V.

Due to internal buffering of the MCS-48 bus, access times will be negligibly degraded by the PROMPT system. Since MCS-48 processors do not communicate internal address gate status, bus data must be driven out if neither PSEN nor RD is asserted.

SYSTEM DEVICES

Both user programs and the PROMPT monitor enjoy access to system devices: serial I/O, panel displays and keyboard. These are memory-mapped to program memory addresses beyond 2K.

The SERIAL I/O port (data 820_{16}, control 821_{16}) is defined by software and jumpers for 110 baud, 20 mA current loop, but can easily be jumpered for other baud rates and RS232C levels. Asynchronous or synchronous transmission, data format, control characters, and parity can be programmed.

Software is used to debounce the PANEL KEYBOARD (data 810_{16}). The monitor's input routines (see SOFTWARE DRIVERS) provide this debouncing and can be called from user programs.

Eight display ports (data $810\text{-}817_{16}$) allow each of the PANEL DISPLAYS to be written from user programs. Data written on a display device will time out after a fixed interval. Displays must be refreshed on a polled or interrupt-driven basis. User programs can call SOFTWARE DRIVERS which provide this capability.

COMMANDS

- ☐ GO
  - ☐ Single Step
  - ☐ With Break
  - ☐ No Break
- ☐ Examine/Modify
  - ☐ Register
  - ☐ Data
  - ☐ Program

  Memory

☐ Open Previous/Clear Entry ⊡ Next ⊡ Execute/End

FUNCTIONS

- **2** Port 2 Map
- **3** Program EPROM (8748)
- **4** Search (R, D or P)* Memory for 1 byte, optional mask
- **5** Search (R, D or P) Memory for 2 bytes, optional mask
- **6** Hexadecimal Calculator +, –
- **7** 8748 Program EPROM for Debug
- **8** Compare EPROM with memory
- **9** Move Memory (R, D or P)
- **A** Access
- **B** Breakpoint
- **C** Clear Memory (R, D or P)
- **D** Dump Memory (R, D or P)
- **E** Enter (Read) Memory (R, D or P)
- **F** Fetch EPROM Program Memory

*R, D or P is Register, Data or Program.

SOFTWARE DRIVERS

Panel Keyboard In: KBIN, KDBIN

Panel Display Out: DGS6, DGOUT, HXOUT, BLK, REFS, ENREF

Serial Channel: CI, CO, RI, PO, CSTS

CONNECTORS

Serial I/O: 3M 3462-0001 Flat Crimp/AMP 88106-1 Flat Crimp/TI H312113 Solder/AMP 1-583485-5 Solder.

Panel I/O Ports and Bus Connector: 3M 3425 Flat Crimp. A complete cable set including wirewrap header for prototyping is included with each PROMPT.

EQUIPMENT SUPPLIED

PROMPT 48 mainframe with two MCS-48 processors (8748, 8035), display/keyboard, EPROM Programmer, power supply, cabinet and ROM-based monitor.

110 VAC power cable, 110 or 220 VAC, fuse, Panel I/O Ports and Bus Connector cable set, PROMPT 48 User's Manual, PROMPT 48 Monitor Listing, Reference Cardlet, PROMPT 48 Programming Pads, MCS-48 Microcomputer User's Manuals, MCS-48 Assembly Language Manual, PROMPT 48 Schematics.

ORDERING INFORMATION

PROMPT-48	Complete PROMPT 48, set 110 VAC
PROMPT-48-220V	Complete PROMPT 48, set 220 VAC
PROMPT-SER	Serial cable connects PROMPT to TTY, CRT
PROMPT-SPP	Specialized PROM Programmer Kit connects PROMPT 48 to Intellec 800 Microcomputer Development System for EPROM programming.

Additional PROMPT 48 Programming Pads (98-401) and manuals (98-402) may be ordered from Intel Literature Department.

PHYSICAL CHARACTERISTICS

Maximum Height:	13.5 cm (5.3 in.)
Width:	43.2 cm (17 in.)
Maximum Depth:	43.2 cm (17 in.)
Weight:	9.6 kg (21 lb.)

ELECTRICAL REQUIREMENTS

Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC).

Frequency is 47-63 Hz.

ENVIRONMENTAL

Operating Temperature:	0°C to +40°C
Non-Operating Temperature:	–20°C to +65°C

SDK-85
MCS-85 SYSTEM DESIGN KIT

Complete single board microcomputer system including CPU, memory, and I/O

Easy to assemble, low cost, kit form

Extensive system monitor software in ROM

Interactive LED display and keyboard

Large wire-wrap area for custom interfaces

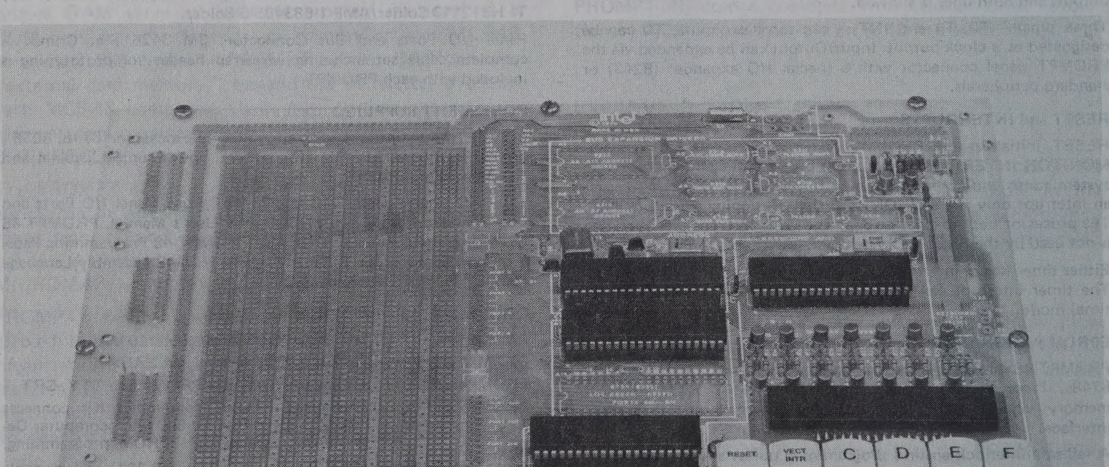
Popular 8080A instruction set

Interfaces directly with TTY

High performance 3 MHz 8085A CPU (1.3 μs instruction cycle)

Comprehensive design library included

The SDK-85 MCS-85 System Design Kit is a complete single board microcomputer system in kit form. It contains all components required to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included is a preprogrammed ROM containing a system monitor for general software utilities and system diagnostics. The complete kit includes a 6-digit LED display and a 24-key keyboard for a direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal. The SDK-85 is an inexpensive, high performance prototype system that has designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-85 is a complete 8085A microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, capacitors, and sockets are included. Assembly time varies from three to five hours, depending on the skill of the user. The SDK-85 functional block diagram is shown in Figure 1.

8085A Processor

The SDK-85 is designed around Intel's 8085A microprocessor. The Intel 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software upward compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085A (CPU), 8156 (RAM), and 8355/8755 (ROM/PROM). A block diagram of the 8085A microprocessor is shown in Figure 2.

System Integration — The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

Addressing — The 8085A uses a multiplexed data bus. The 16-bit address is split between the 8-bit address bus and the 8-bit address/data bus. The on-chip address latches of 8155/8156/8355/8755 memory products allows a direct interface with the 8085A.

System Monitor

A compact but powerful system monitor is supplied with the SDK-85 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

Communications Interface

The SDK-85 communicates with the outside world through either the on-board LED display/keyboard combination, or the user's TTY terminal (jumper selectable).

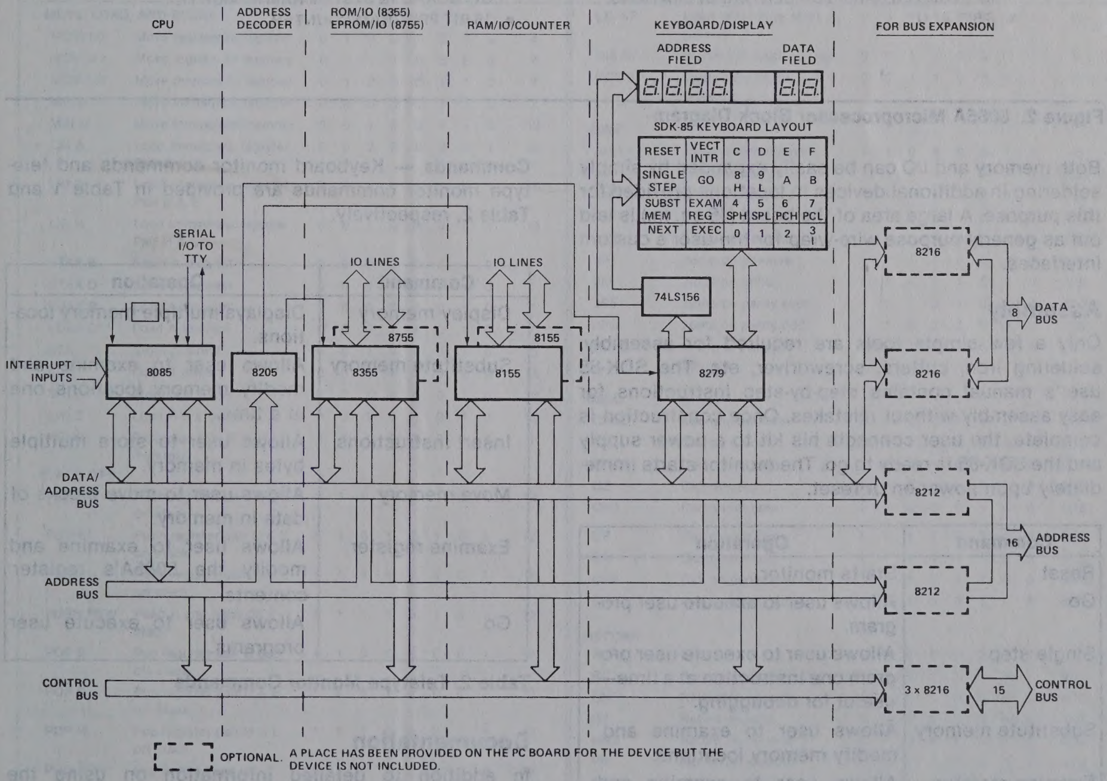
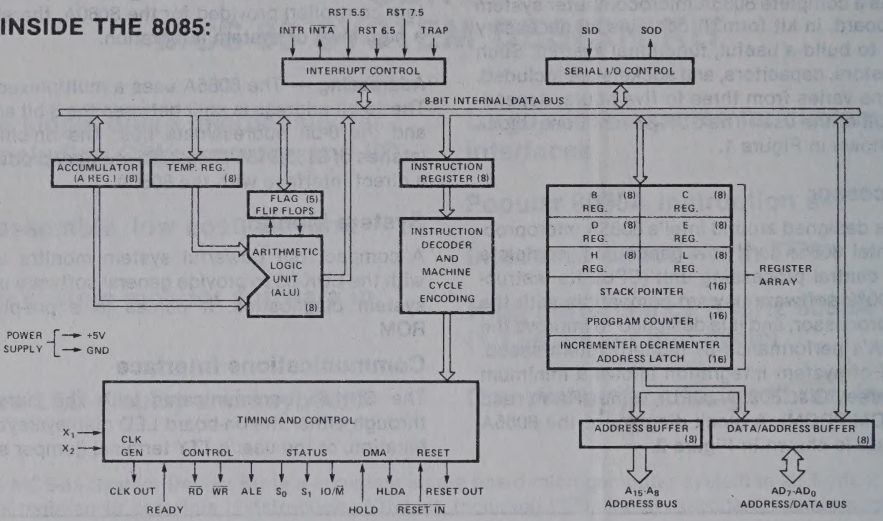

CPU
ADDRESS DECODER
ROM/IO (8355)
EPROM/IO (8755)
RAM/IO/COUNTER
KEYBOARD/DISPLAY
FOR BUS EXPANSION
ADDRESS FIELD
DATA FIELD
SDK-85 KEYBOARD LAYOUT
RESET
VECT INTR
C
D
E
F
SINGLE STEP
GO
8 H
9 L
A
B
SUBST MEM
EXAM REG
4 SPH
5 SPL
6 PCH
7 PCL
NEXT
EXEC
0
1
2
3
SERIAL I/O TO TTY
IO LINES
IO LINES
74LS156
8216
8
DATA BUS
8216
INTERRUPT INPUTS
8085
8205
8755
8355
8155
8155
8279
DATA/ ADDRESS BUS
8212
16
ADDRESS BUS
ADDRESS BUS
8212
CONTROL BUS
3 x 8216
15
CONTROL BUS
OPTIONAL. A PLACE HAS BEEN PROVIDED ON THE PC BOARD FOR THE DEVICE BUT THE DEVICE IS NOT INCLUDED.

Figure 1. SDK-85 System Design Kit Functional Block Diagram

INSIDE THE 8085:


INTR
INTA
RST 5.5
RST 6.5
RST 7.5
TRAP
INTERRUPT CONTROL
SID
SOD
SERIAL I/O CONTROL
8-BIT INTERNAL DATA BUS
ACCUMULATOR (A REG.) (8)
TEMP. REG. (8)
FLAG (5) FLIP FLOPS
ARITHMETIC LOGIC UNIT (ALU) (8)
INSTRUCTION REGISTER (8)
INSTRUCTION DECODER AND MACHINE CYCLE ENCODING
B REG. (8)
C REG. (8)
D REG. (8)
E REG. (8)
H REG. (8)
L REG. (8)
STACK POINTER (16)
PROGRAM COUNTER (16)
INCREMENTER DECREMENTER ADDRESS LATCH (16)
REGISTER ARRAY
POWER SUPPLY
+5V
GND
TIMING AND CONTROL
X1
X2
CLK GEN
CONTROL
STATUS
DMA
RESET
CLK OUT
READY
RD
WR
ALE
S0
S1
IO/M
HOLD
HLDA
RESET IN
RESET OUT
ADDRESS BUFFER (8)
DATA/ADDRESS BUFFER (8)
A15-A8 ADDRESS BUS
AD7-AD0 ADDRESS/DATA BUS

- SEVEN 8-BIT REGISTERS. SIX OF THEM CAN BE LINKED IN REGISTER PAIRS FOR CERTAIN OPERATIONS.
- 8-BIT ALU.
- 16-BIT STACK POINTER (STACK IS MAINTAINED OFFBOARD IN SYSTEM RAM MEMORY).
- 16-BIT PROGRAM COUNTER.

Figure 2. 8085A Microprocessor Block Diagram

Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (45 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-85 user's manual contains step-by-step instructions for easy assembly without mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-85 is ready to go. The monitor starts immediately upon power-on or reset.

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program.
Single step	Allows user to execute user program one instruction at a time—useful for debugging.
Substitute memory	Allows user to examine and modify memory locations.
Examine register	Allows user to examine and modify 8085A's register contents.
Vector interrupt	Serves as user interrupt button.

Table 1. Keyboard Monitor Commands

Commands — Keyboard monitor commands and teletype monitor commands are provided in Table 1 and Table 2, respectively.

Command	Operation
Display memory	Displays multiple memory locations.
Substitute memory	Allows user to examine and modify memory locations one at a time.
Insert instructions	Allows user to store multiple bytes in memory.
Move memory	Allows user to move blocks of data in memory.
Examine register	Allows user to examine and modify the 8085A's register contents.
Go	Allows user to execute user programs.

Table 2. Teletype Monitor Commands

Documentation

In addition to detailed information on using the monitors, the SDK-85 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-85 is shown in Figure 3 and listed in the Specifications section under Reference Manuals.

Intel delivers a unique new microcomputer, the 8085. It's like the 8080. Only better.
intel
MCS 85
MCS-85 System Design Kit

Figure 3. SDK-85 Design Library

8085A INSTRUCTION SET

Table 3 contains a summary of processor instructions used for the 8085A microprocessor.

Mnemonic	Description	Instruction Code^2								Clock^3 Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
MOVE, LOAD, AND STORE										
MOVr1r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M.r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r.M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack. H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12

continued

Mnemonic[1]	Description	Instruction Code[2]								Clock[3] Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

Mnemonic[1]	Description	Instruction Code[2]								Clock[3] Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupts	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085 INSTRUCTIONS										
RIM	Read interrupt mask	0	0	1	0	0	0	0	0	4
SIM	Set interrupt mask	0	0	1	1	0	0	0	0	4

Notes

1. All mnemonics copyright © Intel Corporation 1977.
2. DDD or SSS: B = 000, C = 001, D = 010, E = 011, H = 100, L = 101, Memory = 110, A = 111.
3. Two possible cycle times. (6/12) indicates instruction cycles dependent on condition flags.

Table 3. Summary of 8085A Processor Instructions

SPECIFICATIONS

Central Processor

CPU — 8085A

Instruction Cycle — 1.3 μs

Tcy — 330 ns

Memory

ROM — 2K bytes (expandable to 4K bytes) 8355/8755A

RAM — 256 bytes (expandable to 512 bytes) 8155

Addressing

ROM — 0000-07FF (expendable to 0FFF with an additional 8355/8755A)

RAM — 2000-20FF (2800-28FF available with an additional 8155)

Note

The wire-wrap area of the SDK-85 PC board may be used for additional custom memory expansion up to the 64K-byte addressing limit of the 8085A.

Input/Output

Parallel — 38 lines (expandable to 76 lines)

Serial — Through SID/SOD ports of 8085A. Software generated baud rate.

Baud Rate — 110

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — 20 mA current loop TTY

Note
By populating the buffer area of the board, the user has access to all bus signals that enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts

Three Levels
(RST 7.5) — Keyboard interrupt
(RST 6.5) — TTL input
(INTR) — TTL input

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Pre-programmed 8755A or 8355 ROM
Addresses — 0000–07FF
Monitor I/O — Keyboard/display or TTY (serial I/O)

Physical Characteristics

Width — 12.0 in. (30.5 cm)
Height — 10 in. (25.4 cm)
Depth — 0.50 in. (1.27 cm)
Weight — approx. 12 oz

Electrical Characteristics

DC Power Requirement (power supply not included in kit)

Voltage	Current
V_{CC} 5V ±5%	1.3A
V_{TTY} – 10V ± 10%	0.3A (V_{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0-55°C

Reference Manuals

9800451 — SDK-85 User's Manual (SUPPLIED)
9800366 — MCS-85 User's Manual (SUPPLIED)
9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)
8085/8080 Assembly Language Reference Card (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SDK-85	MCS-85 system design kit

SDK-86
MCS-86 SYSTEM DESIGN KIT

Complete single board microcomputer system including CPU, memory, and I/O

Easy to assemble kit form

High performance 8086 16-bit CPU

Interfaces directly with TTY or CRT

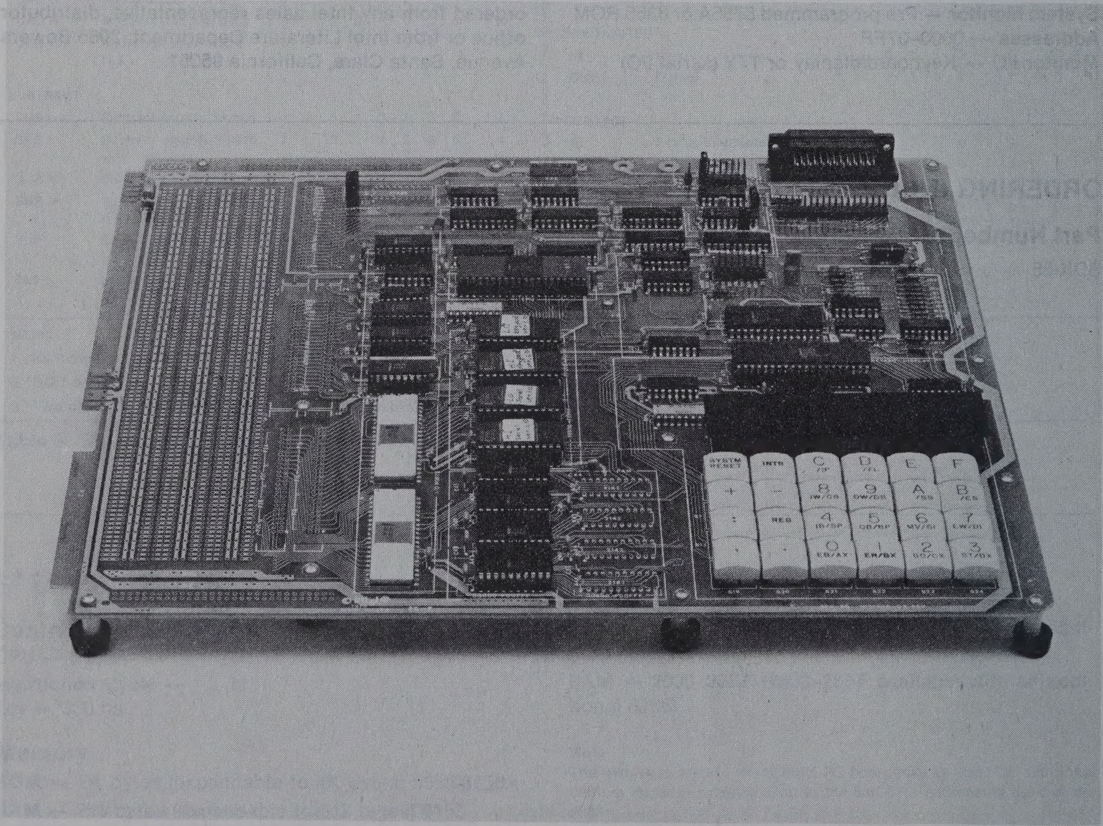
Interactive LED display and keyboard

Wire wrap area for custom interfaces

Extensive system monitor software in ROM

Comprehensive design library included

The SDK-86 MCS-86 System Design Kit is a complete single board 8086 microcomputer system in kit form. It contains all necessary components to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included are preprogrammed ROMs containing a system monitor for general software utilities and system diagnostics. The complete kit includes an 8-digit LED display and a mnemonic 24-key keyboard for direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal, CRT terminal, or the serial port of an Intellec system. The SDK-86 is a high performance prototype system with designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-86 is a complete MCS-86 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, and sockets are included. Assembly time varies from 4 to 10 hours, depending on the skill of the user. The SDK-86 functional block diagram is shown in Figure 1.

8086 Processor

The SDK-86 is designed around Intel's 8086 microprocessor. The Intel 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor features attributes of both 8-bit and 16-bit microprocessors in that it addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. Additional features of the 8086 include the following:

- Direct addressing capability to one megabyte of memory
- Assembly language compatibility with 8080/8085
- 14 word × 16-bit register set with symmetrical operations
- 24 operand addressing modes
- Bit, byte, word, and block operations
- 8 and 16-byte signed and unsigned arithmetic in binary or decimal mode, including multiply and divide
- 5 MHz clock rate
- MULTIBUS compatible system interface

A block diagram of the 8086 microprocessor is shown in Figure 2.

System Monitor

A compact but powerful system monitor is supplied with the SDK-86 to provide general software utilities and system diagnostics. It comes in preprogrammed read only memories (ROMs).

Communications Interface

The SDK-86 communicates with the outside world through either the on-board light emitting diode (LED) display/keyboard combination or the user's TTY or CRT terminal (jumper selectable), or by means of a special mode in which an Intellec development system transports finished programs to and from the SDK-86. Memory may be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (22 square inches) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly: soldering iron, cutters, screwdriver, etc. The SDK-86 assembly manual contains step-by-step instructions for easy assembly with a minimum of mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-86 is ready to go. The monitor starts immediately upon power-on or reset.

Commands — Keyboard mode commands, serial port commands, and Intellec slave mode commands are summarized in Table 1, Table 2, and Table 3, respectively. The SDK-86 keyboard is shown in Figure 3.

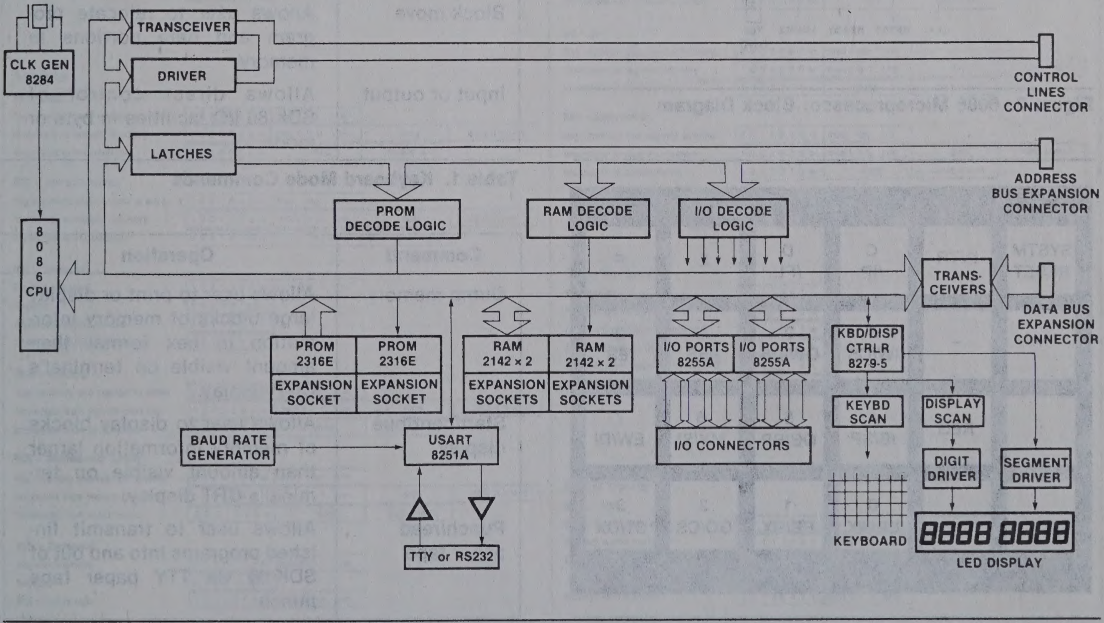

TRANSCEIVER
CLK GEN 8284
DRIVER
CONTROL LINES CONNECTOR
LATCHES
ADDRESS BUS EXPANSION CONNECTOR
8086 CPU
PROM DECODE LOGIC
RAM DECODE LOGIC
I/O DECODE LOGIC
TRANS-CEIVERS
DATA BUS EXPANSION CONNECTOR
PROM 2316E
PROM 2316E
EXPANSION SOCKET
EXPANSION SOCKET
RAM 2142 × 2
RAM 2142 × 2
EXPANSION SOCKETS
EXPANSION SOCKETS
I/O PORTS 8255A
I/O PORTS 8255A
KBD/DISP CTRLR 8279-5
KEYBD SCAN
DISPLAY SCAN
I/O CONNECTORS
BAUD RATE GENERATOR
USART 8251A
DIGIT DRIVER
SEGMENT DRIVER
KEYBOARD
8888 8888
LED DISPLAY
TTY or RS232

Figure 1. SDK-86 System Design Kit Functional Block Diagram

Documentation

In addition to detailed information on using the monitors, the SDK-86 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-86 is shown in Figure 4 and listed in the specifications section under Reference Manuals.

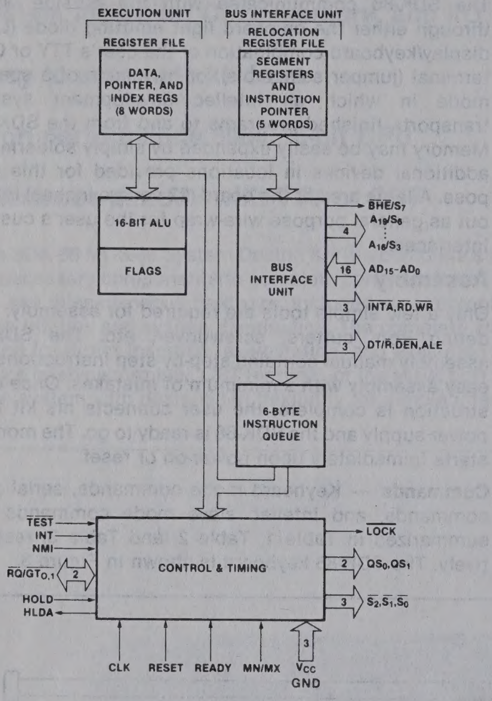

EXECUTION UNIT
BUS INTERFACE UNIT
REGISTER FILE
RELOCATION REGISTER FILE
DATA, POINTER, AND INDEX REGS (8 WORDS)
SEGMENT REGISTERS AND INSTRUCTION POINTER (5 WORDS)
16-BIT ALU
FLAGS
BUS INTERFACE UNIT
BHE/S7
A19/S6
A16/S3
4
16
AD15-AD0
3
INTA,RD,WR
3
DT/R,DEN,ALE
6-BYTE INSTRUCTION QUEUE
TEST
INT
NMI
RQ/GT0,1
2
HOLD
HLDA
CONTROL & TIMING
LOCK
2
QS0,QS1
3
S2,S1,S0
3
CLK
RESET
READY
MN/MX
VCC
GND

Figure 2. 8086 Microprocessor Block Diagram

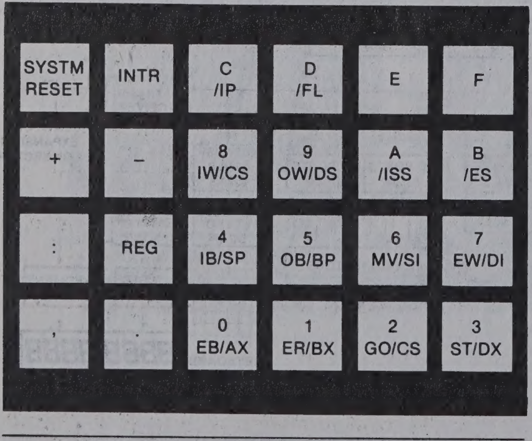

SYSTM RESET
INTR
C /IP
D /FL
E
F
+
–
8 IW/CS
9 OW/DS
A /ISS
B /ES
:
REG
4 IB/SP
5 OB/BP
6 MV/SI
7 EW/DI
,
.
0 EB/AX
1 ER/BX
2 GO/CS
3 ST/DX

Figure 3. SDK-86 Keyboard

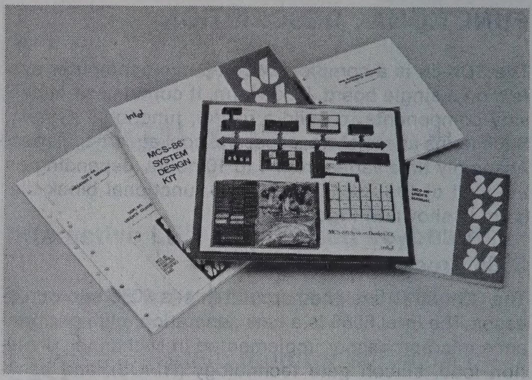

intel
MCS-86 SYSTEM DESIGN KIT

Figure 4. SDK-86 Design Library

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program, and causes it to halt at predetermined program stop. Useful for debugging.
Single step	Allows user to execute user program one instruction at a time. Useful for debugging.
Substitute memory	Allows user to examine and modify memory locations in byte or word mode.
Examine register	Allows user to examine and modify 8086 register contents.
Block move	Allows user to relocate program and data portions in memory.
Input or output	Allows direct control of SDK-86 I/O facilities in byte or mode.

Table 1. Keyboard Mode Commands

Command	Operation
Dump memory	Allows user to print or display large blocks of memory information in hex format than amount visible on terminal's CRT display.
Start/continue display	Allows user to display blocks of memory information larger than amount visible on terminal's CRT display.
Punch/read paper tape	Allows user to transmit finished programs into and out of SDK-86 via TTY paper tape punch.

Table 2. Serial Mode Commands

8086 INSTRUCTION SET

Table 4 contains a summary of processor instructions used for the 8086 microprocessor.

Mnemonic and Description	Instruction Code			
Data Transfer				
MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate to register	1 0 1 1 w reg	data	data if w=1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT=Translate byte to AL	1 1 0 1 0 1 1 1			
LEA=Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS=Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES=Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF=Load AH with flags	1 0 0 1 1 1 1 1			
SAHF=Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF=Push flags	1 0 0 1 1 1 0 0			
POPF=Pop flags	1 0 0 1 1 1 0 1			
Arithmetic				
ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w=1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w=1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA=ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA=Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w=1	
SBB = Subtract with borrow				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w=1	
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG=Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		

Mnemonic and Description	Instruction Code			
CMP = Compare:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w=01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w=1	
AAS=ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS=Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL=Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL=Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM=ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV=Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV=Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD=ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW=Convert byte to word	1 0 0 1 1 0 0 0			
CWD=Convert word to double word	1 0 0 1 1 0 0 1			
Logic				
NOT=Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL=Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR=Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR=Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL=Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR=Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL=Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR=Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	
String Manipulation				
REP=Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w			
STOS = Stor byte/wd frm AL/A	1 0 1 0 1 0 1 w			
Control Transfer				
CALL = Call:				
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		

continued

Mnemonic and Description	Instruction Code		
JMP = Unconditional Jump:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg. adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ=Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE=Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG=Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE=Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA=Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE=Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO=Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS=Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ=Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE=Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG=Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	
JNB/JAE=Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp	
JNBE/JA=Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp	
JNP/JPO=Jump on not par/par odd	0 1 1 1 1 0 1 1	disp	
JNO=Jump on not overflow	0 1 1 1 0 0 0 1	disp	

Mnemonic and Description	Instruction Code	
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNS=Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP=Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE=Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE=Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ=Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT = Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO=Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET=Interrupt return	1 1 0 0 1 1 1 1	
Processor Control		
CLC=Clear carry	1 1 1 1 1 0 0 0	
CMC=Complement carry	1 1 1 1 0 1 0 1	
STC=Set carry	1 1 1 1 1 0 0 1	
CLD=Clear direction	1 1 1 1 1 1 0 0	
STD=Set direction	1 1 1 1 1 1 0 1	
CLI=Clear interrupt	1 1 1 1 1 0 1 0	
STI=Set interrupt	1 1 1 1 1 0 1 1	
HLT=Halt	1 1 1 1 0 1 0 0	
WAIT=Wait	1 0 0 1 1 0 1 1	
ESC=Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK=Bus lock prefix	1 1 1 1 0 0 0 0	

Notes

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 0 then "count" in (CL)
x = don't care.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL) register.
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics © Intel, 1978

Table 4. 8086 Instruction Set Summary

SPECIFICATIONS

Central Processor

CPU — 8086-4

Note

May be operated at 2.5 MHz or 5 MHz, jumper selectable, for use with 8086.

Memory

ROM — 8K bytes 2316/2716

RAM — 2K bytes (expandable to 4K bytes) 2142

Addressing

ROM — FE000-FFFFF

RAM — 0-7FF (800-FFF available with additional 2142's)

Note

The wire-wrap area of the SDK-86 PC board may be used for additional custom memory expansion.

Input/Output

Parallel — 48 lines (two 8255A's)

Serial — RS232 or current loop (8251A)

Baud Rate — selectable from 110 to 4800 baud

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — 20 mA current loop TTY or RS232

Note

The user has access to all bus signals which enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts (256 vectored)

Maskable
Non-maskable
TRAP

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Preprogrammed 2716 or 2316 ROMs

Addresses — FE000–FFFFF

Monitor I/O — Keyboard/display or TTY or CRT (serial I/O)

Physical Characteristics

Width — 13.5 in. (34.3 cm)

Height — 12 in. (30.5 cm)

Depth — 1.75 in. (4.45 cm)

Weight — approx. 24 oz. (3.3 kg)

Electrical Characteristics

DC Power Requirement

(Power supply not included in kit)

Voltage	Current
V_{CC} 5V ± 5%	3.5A
V_{TTY} − 12V ± 10%	0.3A
	(V_{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0–50°C

Reference Manuals

9800697A — SDK-86 MCS-86 System Design Kit Assembly Manual

9800722 — MCS-86 User's Manual

9800640A — 8086 Assembly Language Programming Manual

8086 Assembly Language Reference Card

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

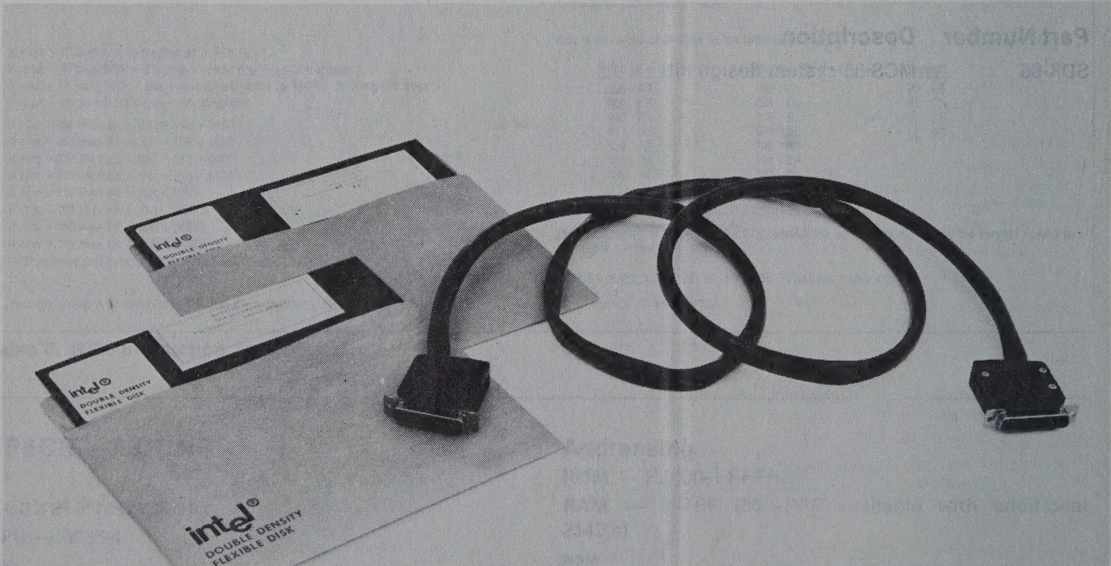
Part Number	Description
SDK-86	MCS-86 system design kit

SDK-C86

MCS-86™ SYSTEM DESIGN KIT SOFTWARE AND CABLE INTERFACE TO INTELLEC® DEVELOPMENT SYSTEM

- **Provides the Software and Hardware Communications Link Between an Intellec® Development System and the SDK-86**
- **Intellec® System Files can be Accessed and Down loaded to the SDK-86 Resident Memory**
- **Data in SDK-86 Memory can be Uploaded and Saved in Intellec® System Files**
- **Enhances and Extends the Power and Usefulness of the SDK-86**
- **Allows the SDK-86 to Become an Execution Vehicle for ISIS-II Developed 8086 Object Code Using the MDS-311 Software Cross Development Package**
- **All SDK-86 Serial Port Mode Commands Become Available at Console of the Intellec® System**

The SDK-C86 product provides the software and hardware link for using the SDK-86 monitor in conjunction with an Intellec® Development System while adding features of data transfer between SDK-86 memory and Intellec® System files. The user may enter programs and data into the SDK-86 and then save them on a diskette. Also, programs and data may be created on the Intellec® System using the MDS-311 cross development software package, then loaded into the SDK-86 for testing and checkout. This provides a real time execution environment of the SDK-86 as a peripheral to the Intellec® System.


intel DOUBLE DENSITY FLEXIBLE DISK
intel DOUBLE DENSITY FLEXIBLE DISK
intel DOUBLE DENSITY FLEXIBLE DISK

HARDWARE

There are two serial ports on the Intellec® System back panel, TTY and CRT. Assuming that one of the ports is used for the Intellec® console, the SDK-C86 cable can plug into the unused port. The SDK-86 is jumper selectable to accept either the CRT (RS232) or TTY (20mA current loop) signals.

The edge connector on the SDK-86 has the MULTIBUS™ form factor. No signals are connected to the fingers except the power supply traces. Therefore, the SDK-86 can plug directly into the Intellec® motherboard to obtain power while using the SDK-C86 cable as the communication link.

SOFTWARE

Two programs must be invoked to operate in the SDK-86 slave mode. One program runs on the SDK-86, and another runs in any ISIS-II environment that includes a diskette drive.

The serial I/O monitor is installed on the SDK-86 and operates as though it was talking to a terminal. The software in the Intellec® allows the Intellec®, with a console device, to behave as if it were a terminal to the SDK-86.

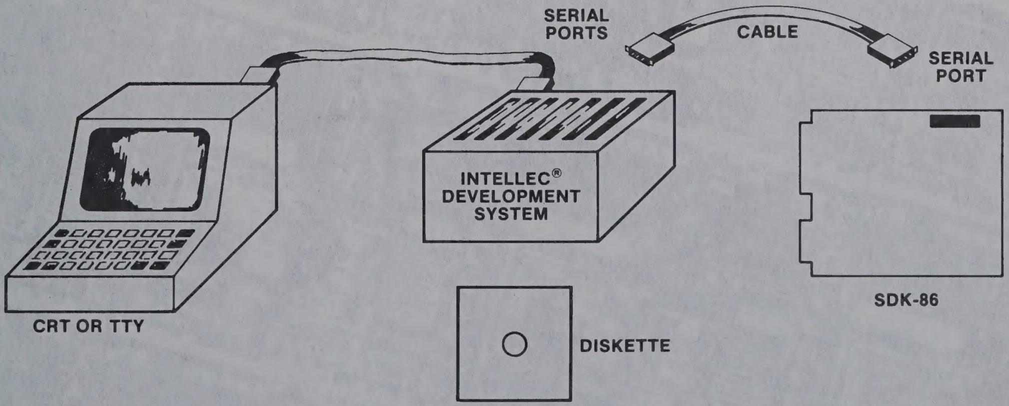
The SDK-C86 software program in the Intellec reads the console input device, then passes the character to the SDK-86 through the serial port. It also receives the characters from the SDK-86 and displays them at the console output device. Besides the basic transfer function, this program also recognizes and performs the Upload and Download functions.

COMMAND MODES

- Transparent: In this mode, the SDK-C86 software passes all characters through without any processing. All the commands of the SDK-86 monitor (except paper tape commands) are available and will function in exactly the same manner as if the terminal were attached directly to the serial port of the SDK-86.
- Upload/Download: In this mode the SDK-C86 software, in the Intellec®, recognizes the mnemonic for Upload or Download from the terminal. It "translates" the Download command to an R (Read hexadecimal tape) command and the Upload command to a W (Write hexadecimal tape). The R and W commands are then passed on to the SDK-86 monitor. Using these paper tape commands allows for a checksummed transfer of data between the Intellec® and the SDK-86 memory.

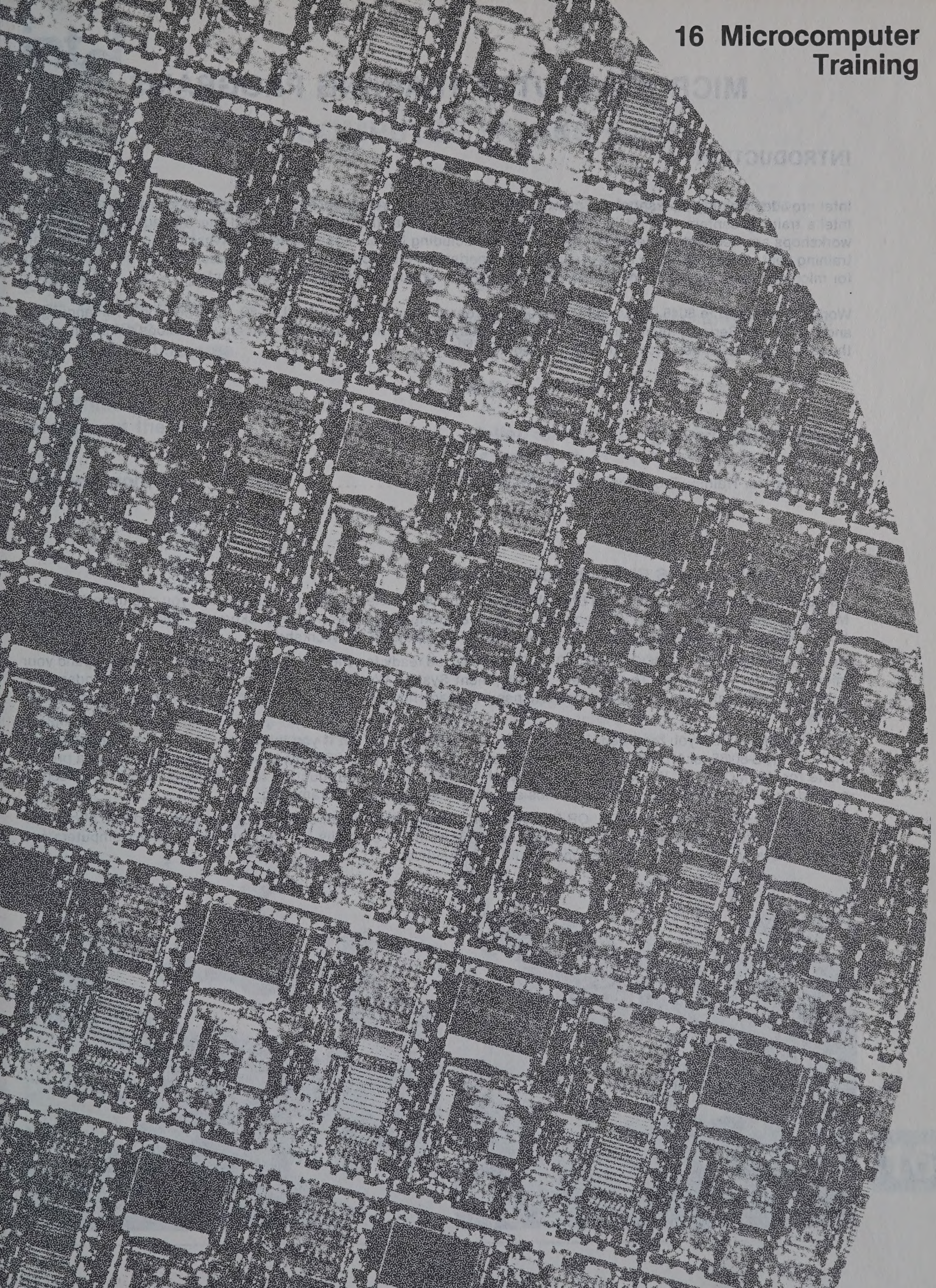
COMMAND SUMMARY

- Reset — starts the SDK-86 monitor.
- Execute with Breakpoint (G) — Allows you to execute a user program and cause it to halt at a predetermined program step — useful for debugging.
- Single Step (N) — allows you to execute a user program one instruction at a time — useful for debugging.
- Substitute Memory (S, SW) — allows you to examine and modify memory locations in byte or word mode.
- Examine Register (X) — allows you to examine and modify the 8086's register contents.
- Block Move (M) — allows you to relocate program and data portions in memory.
- Input or Output (I, IW, O, OW) — allows direct control of the SDK-86's I/O facilities in byte or word mode.
- Display Memory (D) — allows you to print or display large blocks of memory information in HEX format.
- Load (L) — allows you to load hex format object files into SDK-86 memory from an Intellec.
- Transfer (T) — allows you to save contents of SDK-86 memory in a hex format object file in the Intellec.



SDK-86/Intellec® Slave Mode Configuration

16 Microcomputer Training



MICROCOMPUTER TRAINING PROGRAMS

INTRODUCTION

Intel provides training workshops for most of its microcomputer related products. Workshops are given regularly at Intel's training centers located in the San Francisco Bay area, the Boston area and the Chicago area. Selected workshops are frequently offered in other locations including Dallas, Los Angeles and Washington, D.C. areas. The training centers are staffed by highly trained and experienced instructors. This section describes the overall program for microcomputer training and provides outlines for the various workshops offered by Intel.

Workshops cover the 8048, 8080, 8085 and 8086 microprocessor families and PL/M-80, PL/M-86 high level languages and the Intellec Series II microcomputer development systems. Introductory and concept workshops are provided for those with limited experience with these products.

TABLE OF CONTENTS

Microcomputer Training Programs 16-3

WHICH WORKSHOPS SHOULD YOU ATTEND?

As a DESIGN ENGINEER or SYSTEM ENGINEER with a basic knowledge of digital electronics you might start with the MCS-48 or MCS-80/85, or PL/M Workshop. If you lack a strong digital electronics background start with the Introduction to Microcomputers Workshop or the Single Board Computer iSBC Workshop.

As an EXPERIENCED MICROCOMPUTER USER you may be ready for one of the advanced workshops to expand your microcomputer knowledge. The Intellec® Development System Workshop would be appropriate if you understand microcomputers and programming and now need to learn how to use the Intellec® Microcomputer Development System.

As a PROGRAMMER you may want to start with a PL/M Workshop, but if you intend to use assembly language the MCS-48, MCS-80/85, or MCS-86 Workshop would be appropriate. The MCS-80/85 Workshop is suggested as a prerequisite for the MCS-86/88 Workshop. You may wish to consider the Introduction to Microcomputers if you need to expand your knowledge in digital electronics and machine language programming.

As a MANAGER, ADMINISTRATOR, OR PROJECT MANAGER, wishing an overview of this new field, the Microcomputer Concepts Workshop would be suitable, or if you want more details the Introduction to Microcomputers and Intellec Development System Workshops should be considered.

MICROCOMPUTER WORKSHOPS

Courses presented at training centers and customer facilities

Training center locations
- **Boston area**
- **Chicago area**
- **Santa Clara area**

Scheduled on a continuing basis throughout the year

Evening workshop

On-site courses tuned to customer requirements

System demonstration

Hands-on laboratory sessions reinforce lecture

Training center class size limited

Intellec microcomputer development systems with in-circuit emulators used in laboratory

Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel offers a selection of workshops designed to provide users with the tools for making optimum use of Intel microcomputers in system development.

Introduction to Microcomputers

Intended for engineers, scientists, and other technical people with limited computer and digital electronics background, this workship introduces the student to fundamental computer concepts including binary arithmetic, digital logic elements, registers, accumulators, memory addresses, and overall microcomputer organization. The operation of the Intel® 8085 (microprocessor) is then explained along with its instruction set and example programs. Stacks, subroutines, interrupts, I/O interfacing, and high level languages are also introduced. The basics of microcomputer programming are learned with an SDK-85 System Design Kit by developing a program to generate tones on a loudspeaker, and then expanding the program to select musical notes with a keyboard interfaced via the 8279 Programmable Keyboard/Display chip. An SDK-85 Kit (valued at $300) is **yours to keep** when you complete the workshop.

LENGTH: 4 days

TUITION: $695 (includes SDK-85 Kit)

COURSE OUTLINE:

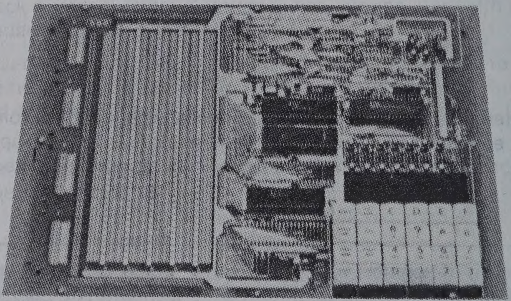
Day 1
Introduction to Microcomputers
Computer Organization
Instruction Execution
Lab — Using Microcomputers

Day 2
Elementary Programming
Microcomputer Interfacing
Lab — Audio Oscillator Using Digital Techniques

Day 3
Computer Arithmetic
Conditional Jumps
Stacks and Subroutines
Push/Pop
Lab —Using Monitor Routine

Day 4
Interrupts
Computer Kit Hardware
Memory Systems
Decimal Arithmetic
Lab

SPECIAL OFFER!



Included in the price of the course is an SDK-85 kit which includes:

3 MHz 8085 CPU (enhanced 8080)
Keyboard — 24 keys
Display — 6 digits
Monitor ROM 2048 bytes
RAM Memory 256 bytes
38 I/O lines
Teletype interface
Complete documentation

NOTE: See page 12 for complete schedule.

iSBC™ Single Board Computer Workshop

This introductory course provides the engineer or programmer with hands-on experience in implementing a board level system with iSBC™ products. Students will work with a variety of I/O boards and will have both digital and analog lab experiments. Programming is done on an Intellec® Microcomputer Development System using Fortran, PL/M 80 or assembly language.

ATTENDEES: The student should have some programming experience.

LENGTH: 5 days.

TUITION: $675

COURSE OUTLINE:

- **Processor Boards**
- **Multibus Operation**
- **Master/Slave**
- **Peripheral Chip Programming**
  - **8251A Programmable Communications**
  - **8253 Programmable Interval Timer**
  - **8255A Programmable Peripheral Interface**
  - **8259A Programmable Interrupt Controller**
- **Debugging with ICE-85™**
- **Configuring Board Options**
- **Software Development**
  - **Credit Editor**
  - **PL/M**
  - **Fortran**
  - **Assembler**

NEW

Microcomputer Concepts Workshop

This workshop is intended for project leaders, managers, administrative staff, or anyone who needs an overview of microprocessor and microcomputer concepts, but lacks the time or need to attend a more in-depth workshop such as the MCS-80/85™ Workshop. Microcomputer terminology, buzzwords, and fundamental programming concepts are explained. A machine language programming example is demonstrated using the SDK-85 System Design Kit. The hardware and software development process is explained, and then a high level language demonstrated using an Intellec® Development System. Intel microcomputers and the appropriate areas for application of each is reviewed. Both a microcomputer chip design, and an iSBC-80™ Single Board Computer design are discussed. Hardware and software trade-offs are explained.

LENGTH: 2 days **TUITION:** $295

COURSE OUTLINE:

Day 1
Terminology
Microcomputer System Organization
Memory
Serial, Parallel Input/Output
Laboratory Using SDK-85
Single Board Computer Overview
Dedicated vs. Standard Computer Selection

Day 2
Introduction to Software
Development System Overview
Laboratory Programming in BASIC
Reliability, Testing, Timing
Application Topics

Intellec® Development System Operation

This lab-intensive workshop teaches the student how to operate the Intellec Microcomputer Development System and the ISIS (Intel Systems Implementation Supervisor) disk operating system. Laboratory operations include editing data files, assembling and compiling programs, using relocation and linkage facilities, and identifying the correct documentation. Some of this material is included in the intermediate level workshops. This is not a programming course.

ATTENDEES: A programmer who will be using the Intellec System. In addition, the technician, programmer-aid, or clerk who needs to operate the Intellec system can benefit from this course.

LENGTH: 3 days. **TUITION:** $395

COURSE OUTLINE:

Day 1
Introduction
System Overview
Running a Program
Using Text Editor
ISIS Disk System

Day 2
Introduction to Fortran
Compiling a Program
Link/Locate
ICE-85™ Demonstration

Day 3
Programming Aids
System Tuning
Maintenance Overview
Manual Review

MCS-80/85™ System Workshop

This workshop will prepare the student to design and develop a system using the Intel® 8080/8085 microprocessors through the use of lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and In-Circuit Emulator.

ATTENDEES: The design engineer, programmer, or one who is familiar with the binary number system and basic logic functions.

LENGTH: 5 days

TUITION: $625

COURSE OUTLINE:

Day 1
Introduction
a. Microprocessor System
  1. Function
  2. Organization
  3. Programming
b. Central Processor Overview
  1. Functional Sections
  2. Programming Model
  3. Execution Sequence

Assembly Language Instructions
a. Input/Output
b. Register/Memory Reference
c. Arithmetic, Logical, Rotates

Input/Output Techniques
a. Programmed I/O
b. Interrupt I/O
c. Direct Memory Access

Programmed Input/Output
a. Status Request
b. Command
c. Data Transfer

Development System
a. Function
b. System Monitor
c. Disk Operating System

Debugging With the System Monitor
a. Break Points
b. Examine Registers

Laboratory
a. Using the System Monitor
b. Program Instruction Sequences
c. Debugging and Break Points

Day 2
Basic CPU Timing
a. Instruction Fetch
b. Bus Structure
c. Read/Write Timing

Subroutines
a. Invocation
b. Stack Memory
c. Parameters

Interrupt System
a. Description
b. RST Instruction
c. Service Subroutines

Disk Operating System Modules
a. Macro Assembler
b. Text Editor
c. File Utility Commands

Laboratory
a. Using the Disk Operating System
b. Program Assembly and /Execution

Day 3
Programming Techniques
a. Branch Tables
b. Direct Load/Store Instructions
c. Special Purpose Instructions

8085 Timing
a. Ready/Wait
b. DMA/Hold

8085 Interrupts
a. RST 5.5, 6.5, 7.5
b. Trap
c. RIM, SIM

8080 vs. 8085
a. 8080 Chip Set
  1. 8228/8238 System Controller
  2. 8224 Clock Generator
b. 8080 Bus Structure
c. 8080 Instruction Timing

Memory Interfacing
a. RAM/ROM/PROM Address Decoding
b. 8708 PROM/8185 RAM

Laboratory
a. Program Design Using Development System
b. Program DEBUG Under Disk Operating System

Day 4
8085 CPU Set
a. 8085 Bus Structure
b. 8355/8755 ROM/EPROM and I/O
c. 8155 RAM/Timer and I/O

I/O Design
a. Memory-mapped
b. 8255 Parallel Interface
c. 8251 Serial Interface

In-Circuit Emulator
a. Prototype Development
b. Resource Sharing
c. Mapping Commands
d. Utility Commands
e. Debug Commands
f. Emulation Syntax

Laboratory
a. Use of the In-Circuit Emulator for System Debugging

Day 5
Relocation and Linkage
a. ISIS-II LINK and LOCATE Commands
b. Relocatable Libraries
c. Parameter Passing
d. System Design

Macros
Single Board Computers
a. Use as a System Component
b. Parallel I/O Options
c. Serial I/O Options
d. Interrupt System
e. Family Boards

PL/M-80 Language/Software Design Workshop

This workshop will prepare the student for designing, developing and debugging modular PL/M-80 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and In-Circuit Emulator.

ATTENDEES: The design engineer, programmer, or one who is familiar with the binary number system and basic logic functions. Prior programming experience will assist the student in obtaining maximum benefit from the course.

PREREQUISITE: Introduction to Microcomputers or MCS-80/85™ System Workshops is recommended.

LENGTH: 5 days. **TUITION:** $675

COURSE OUTLINE:

Day 1

Introduction

a. Preview of Course
b. Overview of PL/M, Linking and Relocation
c. Why use a High Level Language

Definitions

Symbols, Identifiers, Reserved Words, Comments, Data Elements, Expressions, Statements, Declarations

Data Elements

Variables, Subscripted Variables, Data type, Constants

Operators, Operations and Priorities

Arithmetic and Boolean

Evaluating Expressions

Statements

Redefine, Basic, Conditional

Assignment

a. Implement a Given Algorithm in PL/M

Day 2

ISIS-II Disc Operating System

a. Components of System

ISIS-II File Structure

a. System Files
b. User Files
c. Device Files
d. Directory and File Attributes

ISIS-II Commands

a. CUSPS — Commonly Used System Programs
b. Directory and Attribute Commands
c. Rename and Delete Commands
d. Creating System and User Discs

Credit Editor

ISIS-II PL/M 80 Compiler

a. Invoking PL/M
b. Compiler Options

ISIS-II Locate

a. Invoking Locate

Laboratory

a. Introduction to ISIS-II Disc Operating System
b. Creating a PL/M Source File
c. Compiling a PL/M Program
d. Locating and Executing a PL/M Program

Day 3

Review

Procedures

a. Declaration
b. Invocation
c. Program Construction

Data References

a. Based Variables
b. Variable Equivalencing

Blocks

a. Concept and Use
b. Scope of Declarations

Predeclared Procedures

a. TIME, MOVE, LENGTH, LAST and SIZE Procedures
b. Type Transfers
c. Shifts and Rotates

Laboratory

a. Compile and Locate Program
b. Execute Program

Day 4

Review

Modular Implementation

a. Compilation Modules
b. Modular Programming

ISIS-II Link

a. Invoking Link
b. Link Options
c. Assembly Object Modules

In-Circuit Emulator

a. Definition
b. System Overview
  1. Memory and I/O Mapping
  2. Breakpoint Capability
  3. Dynamic Tracing
  4. Control Block

In-Circuit Emulator Software Driver

a. Modes
b. Commands

System Debugging Examples

System Demonstration

Laboratory

a. Locate
b. Load and Emulate Using In-Circuit Emulator

Day 5

Review

Interrupt Procedures

Reentrant Procedures

ISIS-II Librarian

a. Creating a Library
b. Managing a Library
  1. Adding Modules
  2. Deleting Modules

ISIS-II System Interfaces

a. System Library

Discussion of Selected Programs

Laboratory

a. Create a Library
b. Link Object to a Library

PL/M-86 Language/Software Design Workshop

This workshop will prepare the student for designing, developing and-debugging modular PL/M-86 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and SDK-86.

ATTENDEES: The design engineer, programmer, or one who is familiar with the binary number system and basic logic functions. Prior programming experience will assist the student in obtaining maximum benefit from the course.

PREREQUISITE: MCS-86™ System Workshop is recommended.

LENGTH: 5 days **TUITION:** $675

COURSE OUTLINE:

Day 1

Introduction
- a. Preview of Course
- b. Overview of PL/M, Linking and Relocation
- c. Why Use a High Level Language

Definitions

Symbols, Identifiers, Reserved Words, Comments, Data Elements, Expressions, Statements, Declarations

Data Elements

Variables, Subscripted Variables, Constants

Data Types

Logical, Integer, Real

Operators, Operations and Priorities

Arithmetic and Boolean

Evaluating Expressions

Statements

Redefine, Basic, Conditional

Laboratory
- a. Introduction to ISIS-II Disc Operating System
- b. Compiling a PL/M Program
- c. Locating and Executing a PL/M Program

Day 2

Procedures
- a. Declaration
- b. Invocation
- c. Program Construction

ISIS-II Disc Operating system
- a. Components of System

ISIS-II File Structure

ISIS-II Commands
- a. CUSPS — Commonly Used System Programs
- b. Directory and Attribute Commands
- c. Rename and Delete Commands
- d. Creating System and User Discs

Credit Editor

ISIS-II PL/M 86 Compiler
- a. Invoking PL/M
- b. Compiler Options

ISIS-II LOC86
- a. Invoking LOC86

Laboratory
- a. Implement a PL/M Program

Day 3

Review

Data References
- a. Based Variables
- b. Variable Equivalencing
- c. Pointer Type

Blocks
- a. Concept and Use
- b. Scope of Declarations
- c. Modular Compilation
- d. Modular Program

ISIS-II LINK86
- a. Invoking LINK86
- b. Link Options
- c. Assembly Object Modules

Built-In Facilities

Laboratory
- a. Compile Program Modules
- b. Link and Locate Modules
- c. Execute Program

Day 4

Review

ISIS-II LIB86
- a. Creating a Library
- b. Managing a Library
  - 1 . Adding Modules
  - 2. Deleting Modules

Laboratory

Character String Handling

Interrupt Procedures

Reentrant Procedures

Day 5

ICE-86

Discussion of Selected Programs

Laboratory
- a. Execution and Debugging of Selected Programs

MCS-86/88™ System Workshop

This workshop will prepare the student to develop assembly language programs and design systems based on the Intel® 8086/8088 microprocessor through the use of lecture, demonstration, and laboratory "hands-on" experience with the SDK-86 and the Intellec® Microcomputer Development System.

ATTENDEE: The design engineer or programmer who needs an introduction to the 8086 family or the new 8088 microcomputer.

PREREQUISITE: Introduction to Microcomputers, MCS-80/85™ System, or equivalent assembly language programming experience.

LENGTH: 5 days

TUITION: $625

COURSE OUTLINE:

Day 1

Introduction

a. Microcomputer System
   1. Function
   2. Memory Organization
   3. Interfacing

b. Central Processor Overview
   1. Programming
   2. Instruction Format

Assembly Language Instruction

a. Register and Data Operations
   1. 8-Bit
   2. 16-Bit

b. I/O Operations

System Design Kit (SDK-86)

a. Demonstration
b. Debugging

Laboratory

a. Using the SDK-86 and Keyboard Monitor

8086/8088 CPUs

a. Block Diagram
b. Signal Description
c. System Design

Day 2

Review

CPU Architecture

a. Addressing Modes

Programming Exercises

Development System

a. ISIS
b. Editor
c. MDS-311 Software

Day 3

Review

Laboratory

a. Using the Development System

Interrupt System

a. Description
b. Signal Pins

Day 4

Review

Programming for Large Systems

a. Segmentation Registers
b. Assembler

Programming

a. Arithmetic
b. String Operators

Laboratory

a. Assembler Programming
b. Download Using Serial Monitor

CPU Timing

a. Read Cycle
b. Memory Access Time
c. Write Cycle

8284 — Clock Generator

8288 — Bus Controller

8282/3 — Octal Latch

8286/7 — Octal Transceiver

Day 5

Other 8086 Configurations

Introduction to PL/M-86

Application Techniques

ICE-86™ Demonstration

Advanced MCS-86/88™ System Workshop

This advanced course reviews material presented in the intermediate level MCS-86/88 System Workshop, and then proceeds to investigate more advanced topics. This workshop will prepare the student to program the 8086/8088 and 8089 components in assembly language. The design and programming of large systems, use of Link, Locate, and Library, Input/Output controllers, and ICE-86™ In-Circuit Emulator are included.

ATTENDEES: The assembly language or PL/M programmer who needs a complete understanding of assembly language programming techniques for the 8086/8088, 8089 and debugging with ICE-86 emulator.

PREREQUISITE: MCS-86/88 System Workshop.

LENGTH: 5 days

TUITION: $675

COURSE OUTLINE:

Day 1

Review of the 8086

Advanced Programming Topics

a. LINK86, LOC86, LIB86
b. PL/M-86 Parameter Passing and Linkage
c. Segmentation
d. CREDIT — Advanced Editor

Laboratory

Day 2

Execution Vehicle Considerations

a. SDK-86
b. iSBC 86/12™ Board
c. Debugging with Monitor

Peripheral Chip Programming

a. 8251A
b. 8253
c. 8255A
d. 8259A

Laboratory

Introduction to ICE-86™ Emulator

Day 3

Advanced ICE-86™ Features

Laboratory — ICE-86™

Interrupt Structures

Multiprocessor Topics

Day 4

Laboratory

Component Family Review

a. CPU, 8282, 8284, 8286, 8288
b. Bus Interface
c. Multi-bus Arbitration Logic

Introduction to Input/Output Processors

a. Device Considerations
b. Programming the 8089

Day 5

Advanced 8089 Topics

PL/M-86

Application Topics

Laboratory

MCS-48™ System Workshop

This workshop will prepare the student to design and develop a system using the Intel® MCS-48 family of single chip microcomputers through the use of lecture, demonstration and laboratory "hands-on" experience with the Intellec® Development System, PROMPT-48™, and In-Circuit Emulator.

ATTENDEES: The design engineer, programmer, or one who is familiar with the binary numbers system and basic logic functions.

LENGTH: 5 days

TUITION: $625

COURSE OUTLINE:

Day 1

Orientation

Introduction
- a. Microprocessor System
  - 1. Function
  - 2. Organization
  - 3. Programming
- b. 8048 Overview
  - 1. Functional Sections
  - 2. Programming Model
  - 3. Execution Sequence

Assembly Language Instructions
- a. I/O Instructions
- b. Data Move Instructions
- c. Increment/Decrement Instructions
- d. Branch Instructions
- e. Worksession No. 1
- f. Accumulator Group Instructions
  - 1 . ADD/ADDC
  - 2. Logicals

PROMPT-48™
- a. Function
- b. Operation

Laboratory Exercise
- a. Program Entry and Execution Using PROMPT-48™

Day 2

Assembly Language Instructions
- a. Accumulator Group Instructions
  - 1. Flags
  - 2. Rotates
- b. Specials (XCH, DA, SWAP)
- c. Worksession No. 2
- d. Subroutines
  - 1. Invocation
  - 2. Stack Operation
- e. Interrupt System
  - 1. Description
  - 2. Service Subroutines
  - 3. Multiple Source Systems

Development System
- a. Function
- b. Disk Operating System

Text Editor and Macro Assembler
- a. Function
- b. Operation

Laboratory Exercise
- a. Bootstrap Procedures
- b. Create, Edit, and Assemble Source Program
- c. Execute Program

Day 3

System Timing
- a. Basic Timing and Timer
- b. Bus Timing for Peripheral Devices

Peripherals and Design
- a. Expanding Memory
  - 1. Program Memory (1, 2K ROMs)
  - 2. Data Memory (RAMs)
- b. Expanding Ports (8243)
  - 1. Device Characteristics
  - 2. Software Control of Ports
- c. Combination Chips
  - 1. 8155 RAM and I/O Chip
  - 2. 8355, 8755 ROM and I/O Chip
- d. Peripheral Interfacing (Parallel)
  - 1. 8255 Parallel I/O
  - 2. 8279 Keyboard and Display Interface
    - —Keyboard Scanning Techniques
    - —Display Refresh

Laboratory Exercise
- a. Edit and Assemble Using DOS
- b. Execute Using PROMPT-48™

Day 4

Peripherals and Design
- a. Peripheral Interfacing (Serial)
  - 1. Transmission Formats
  - 2. Asynchronous Operation
  - 3. RS232C Interface

In-Circuit Emulator
- a. Prototype Development
- b. Resource Sharing
- c. Commands
  - 1. Mapping
  - 2. Utility
  - 3. Interrogation
  - 4. Emulation

Laboratory Exercise
- a. Use of the In-Circuit Emulator for System Debugging

Day 5

8048 Family
- a. 8049
- b. 8041
  - 1. 8041/8048 Difference
  - 2. 8041 Slave/Master Protocol
- c. 8021
- d. 8022

Analog Interfacing
- a. Successive Approximation A/D
- b. A/D, D/A Chips
- c. A/D Design

Laboratory

RMX/80^{TM} Real-Time Multi-Tasking Executive System Workshop

This workshop will cover the concepts of multi-tasking, i.e., what a task is, concurrency of tasks, asynchronous events, priorities and scheduling, resource sharing, interrupts and inter-task communication, as well as actual task writing, system generation and debugging utilizing the Intellec® Microcomputer Development System and iSBC-80/20^{TM} Board.

ATTENDEE: The design engineer or programmer who will be using RMX/80^{TM} in an iSBC^{TM} system application. The student must be familiar with the PL/M-80 Language and Compiler, ISIS-II utility facilities, ISIS-II relocation and linkage facilities, and modular systems programming.

PREREQUISITE: PL/M-80 Language/Software Design Workshop or equivalent knowledge.

LENGTH: 5 days **TUITION:** $675

COURSE OUTLINE:

Day 1

Introduction

What is RMX/80^{TM}

- **a. Constituent Parts of the RMX/80^{TM} Product**
- **b. Overview of the RMX/80^{TM} Development Process**

Review of the Development Process

- a. Intel 8080/8085 Translators
    - 1. Assembler
    - 2. PL/M-80 Compiler
- b. ISIS-II Commands
- c. LINKing Task Modules with the RMX/80^{TM} Nucleus and Intel Provided Tasks
- d. LOCATEing the Final Module in an End Product Environment (Single Board Computer Modules)
- e. Debugging the Task Environment

Real Time Asynchronous Event Processing

- a. Definition of Terminology
- b. Recognition of Asynchronous Events
    - 1. Polling (Status Loop)
    - 2. Preemption (Interrupt)
- c. The Single Unit Program
    - 1. Status Environment
    - 2. Interrupt Environment
- d. Program Execution
    - 1. Sequential Processing
    - 2. Concurrent Processing

Day 2

RMX/80^{TM} Model

- a. Task
    - 1. Single Unit Program
- b. Exchanges and Messages
    - 1. SEND Function
    - 2. WAIT Function
- c. Context Switching and Dispatching of Tasks
- d. A Sequential Model
- e. A Concurrent Model
- f. The Interrupt Exchange/Message

RMX/80^{TM} Terminal Handler

- a. Message Formats
- b. Service Request Exchanges
    - 1. Terminal Input (Line Edited)
    - 2. Terminal Output
- c. Service Response Exchanges

Implementing an RMX^{TM} Task(s) Module

- a. Translator INCLUDE option
- b. Creating a Task(s) Module
- c. RMX/80^{TM} System Creation
- d. Configuration Module
- e. System Generation

Laboratory

- a. Implementation of Two Modules

Day 3

Laboratory

- a. Implement Configuration Module and System Generation

Use of In-Circuit Emulator to Emulate Task System

Terminal Handler

- a. Line Edit Input
- b. Control Character Table
- c. Alarm Exchange — Alarm Message Type
- d. DEBUGGER and Wakeup Exchange

DEBUGGER Task

- a. Configuration
- b. Invoking the DEBUGGER
- c. DEBUGGER Commands

Day 4

RMX/80^{TM} Interrupt Processing

- a. Interrupt Exchanges
- b. Enabling and Disabling Interrupt Levels
- c. Software Priorities and Interrupt Masking
- d. User Defined Interrupt Handling

Line Printer Driver Task Example

- a. Interrupt Handling
    - 1. Using RMX/80^{TM} Model
    - 2. User Defined Handler

Laboratory

- a. Interrupt Handling

Day 5

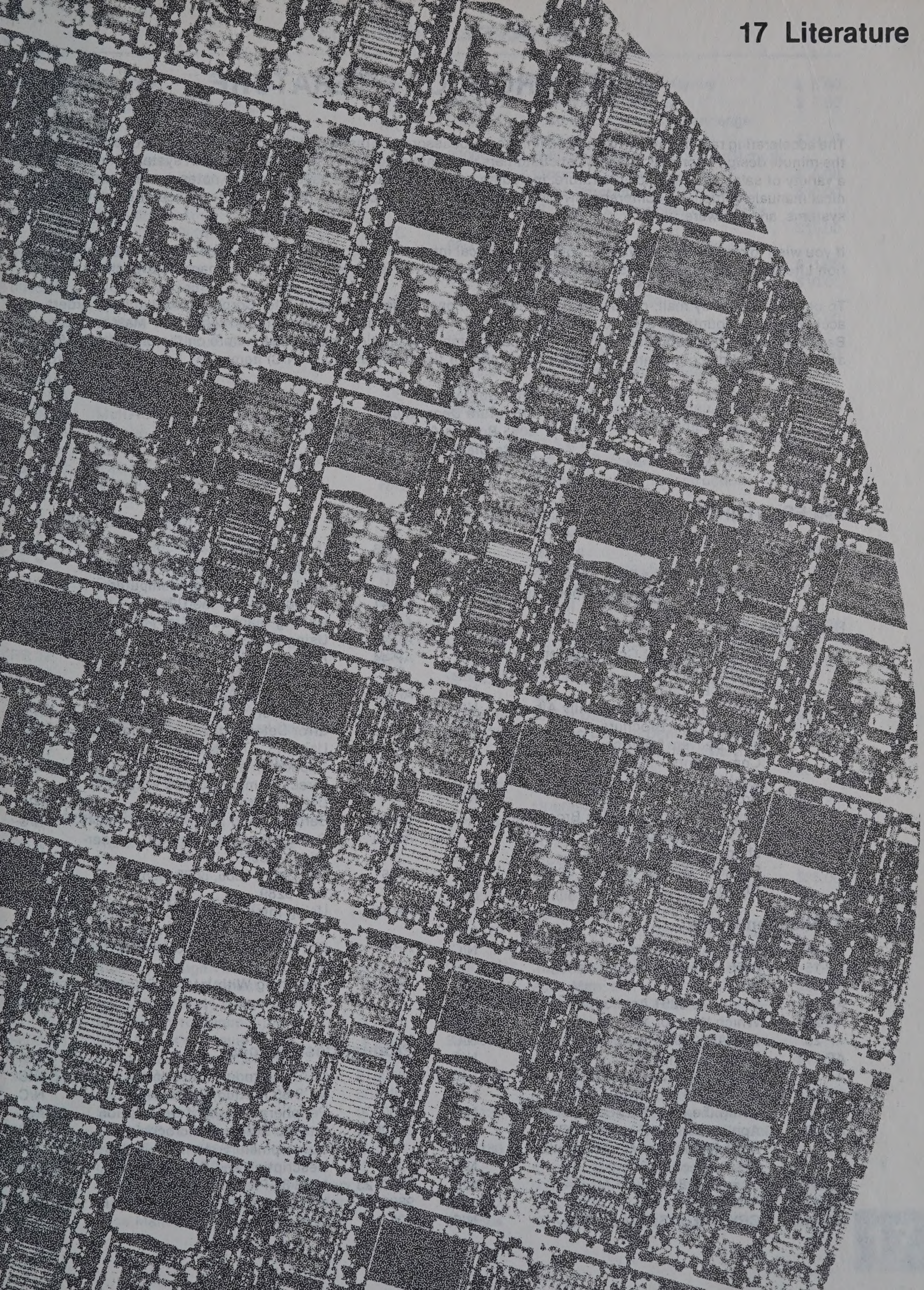
Disk File System

- a. Disk File system Services
- b. Add-on ISIS-II Services
- c. Configuration
    - 1. Free Space Manager
    - 2. Concurrent Operation
- d. File system Structure
    - 1. Directory Format
    - 2. File Data Format

Laboratory

- a. Disk File system

17 Literature



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The accelerating rate of new developments in microprocessors and memories has created the need for concise, up-to-the-minute design information. To assist customers in maintaining expertise in state of the art systems, Intel provides a variety of sales and technical literature, including brochures, data sheets, application notes, handbooks, and technical manuals containing comprehensive information on microprocessors, microcomputers, memories, development systems, and software.

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SALES LITERATURE

Catalogs

1978/79 Systems Data Catalog	$ 2.00
1979 Data Catalog—Components	$ 5.00

Brochures

iSBC 8-Bit/16-Bit Configuration Folder—FULL	N/C
ICE-85 Brochure	N/C
Growing Static RAM Family Album	N/C
2115A/2125A Brochure	N/C
Intel Delivers Microcomputer Components—8086	N/C
Intel Marches On—Military Brochure	N/C
Industrial Control Series Brochure	N/C
1979 Intel Microcomputer Workshops Brochure	N/C
Success Manual for 8086 Users Brochure	N/C

Application Notes

AP-4	2107A Application Note	N/C
AP-15	8255 Programmable Peripheral Interface	N/C
AP-16	Using the 8251 Application Note	N/C
AP-22	Which Way for 16K	N/C
AP-23	2104A 4K RAM	N/C
AP-24	MCS-48 Family	N/C
AP-26	SBC 80/10 & System 80/10	N/C
AP-28A	MULTIBUS Interfacing	N/C
AP-29	Using the Intel 8085 Serial I/O Lines	N/C
AP-30	Applications of 5-Volt EPROM & ROM Family for Microcomputer Systems	N/C
AP-31	Using the 8259	N/C
AP-33	RMX/80	N/C
AP-35	CRYSTALS: Specifications	N/C
AP-36	Using the 8273	N/C
AP-40	Keyboard/Display Scanning With Intel's MCS-48 Microcomputers	N/C
AP-41	Introduction to the UPI-41A	N/C
AP-42	Writing Diagnostics for μScope	N/C
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AP-49	Serial I/O and Math Utilities—8049	N/C
AP-50	Debugging Strategies & Considerations—8089	N/C
AP-51	Designing 8086, 8088, 8089—with 8289	N/C
AP-52	Using Intel's Industrial Control Series in Control Applications	N/C
AP-54	Dot Matrix Printer Controllerl Using 8295	N/C
AP-56	Designing With Intel's 8022 Microcomputer	N/C

Product Descriptions

9800615	MCS-48 Product Description	N/C
9800365	MCS-85 Product Description	N/C
9800600	Peripherals Product Description	N/C
9800606	Intellec Series II Microcomputer Development Systems Functional Description and Specifications	N/C
9800723	MCS-86 Product Description	N/C
9800881	Industrial Control Series Product Description	N/C

Reference Cards

9800774	BASIC-80 Pocket Reference	N/C
9800547	FORTRAN-80 Reference Card	N/C
9800871	UPI-41 Assembly Language Reference Card	N/C
9800412	MCS-48 Assembly Language Reference Card	N/C
May 1979	MCS-48 Assembly Language Reference Card (8021/8022)	N/C
9800438	8085/8080 Assembly Language Reference Card	N/C
9800749	MCS-86 Assembly Language Reference Guide	N/C
9800404	PROMPT-48 Reference Cardlet	$ 1.50
9800653	MCS-48 In-Circuit Emulator Reference Card	N/C
9800976	ICE-85 Pocket Reference	N/C
9800838	ICE-86 Pocket Reference	N/C
9800810	Multi-ICE Reference Card	N/C
9800582	μScope 820 8080A Operator's Reference Card	N/C
9800929	ICIS-COBOL Pocket Reference	N/C
9800841	ISIS II Reference Card	N/C

Reliability Reports

RR 6	1702 Silicon Gate MOS	N/C
RR 7	2107A/2107B 4K Dynamic RAM	N/C
RR 8	Polysilicon Fuse Bipolar PROM	N/C
RR 9	MOS Static RAMs	N/C
RR 10	8080/8080A Microcomputer	N/C
RR 11	2146 16K CCD Memory	N/C
RR 12	2708 8K Erasable PROM	N/C
RR 14	2115/2125 MOS Static RAMs	N/C
RR 15	2104A 4K Dynamic RAM	N/C
RR 16	2116 16K Dynamic RAM	N/C
RR 17	iSBC 80/10 Single Board Computer	N/C
RR 18	HMOS Reliability	N/C
RR 20	2117 N-Channel Silicon Gate 16K Dynamic RAM	N/C

Engineering Reports

ER 4	Hermetic CerDip Packaging	N/C

TECHNICAL LITERATURE

User's Manuals & Guides

111100	Memory Design Handbook	$ 5.00
9800270	MCS-48 User's Manual	$ 7.50
9800255	MCS-48 & UPI-41 Assembly Language Programming Manual	$10.00
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9800676	Peripheral Design Handbook	$ 7.50
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9800203	SDK-80 User's Guide	$ 5.00
9800758	BASIC-80 Reference Manual	$15.00
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9800672	Multi-ICE Operating Instructions for ISIS II Users	$20.00
9800016	Paper Tape Reader Guide	$ 2.50
9800526	μScope-820 Operator's Handbook	$15.00
9800592	μScope 8080A Probe Service Manual	$15.00
9800425	μScope 8085 Probe Service Manual	$15.00
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9800230F	SBC 80/10 & 80/10A Reference Manual	$10.00
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9800317D	SBC 80/20 & 80/20-4 Reference Manual	$10.00
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9800611B	iSBC 80/30 Hardware Reference Manual	$10.00
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9800683	Intel MULTIBUS Specifications	$10.00
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in-5770 Technical Manual	$25.00
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